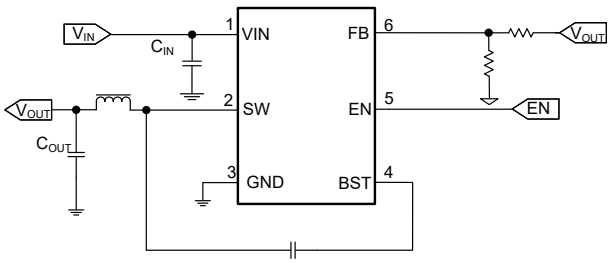
TPS56124x 4.2V to 17V Input, 1A, Synchronous Buck Converter in SOT563

1 Features

- Configured for a wide range of applications
  - Input voltage range: 4.2V to 17V
  - Output voltage range: 0.6V to 7V
  - Reference voltage: 0.6V
  - ±1.5% reference voltage accuracy
  - Integrated FETs: 100mΩ and 55mΩ
  - Low quiescent current for TPS561243: 110µA
  - Switching frequency: 1280kHz
  - Maximum 95% large duty cycle operation
  - Fixed soft-start time: 1.4ms
- Easy of use and small design size
  - TPS561243 Eco-mode and TPS561246 FCCM mode at light load
  - D-CAP3™ control mode with fast transient response
  - Support start-up with prebiased output
  - Non-latch for OV, OT, and UVLO protection
  - Cycle-by-cycle over current limit
  - Hiccup mode for UV protection
  - Operating junction temperature range: –40°C to 125°C
  - SOT563 package: 1.6mm × 1.6mm
- Create a custom design using the TPS56124x with the WEBENCH® Power Designer

2 Applications

- WLAN/Wi-Fi access point
- Modem (cable/DSL/GFAST)
- Small business router
- Electricity meter
- STV and DVR
- Appliances



Simplified Schematic

3 Description

The TPS56124x is a simple, easy-to-use, synchronous buck converter with input voltage ranging from 4.2V to 17V and supports up to 1A continuous current.

The device is designed to operate with minimum external component counts and low standby current.

This switch mode power supply (SMPS) device employs D-CAP3 control mode providing a fast transient response and supporting both low equivalent series resistance (ESR) output capacitors such as specialty polymer and ultra-low ESR ceramic capacitors with no external compensation components.

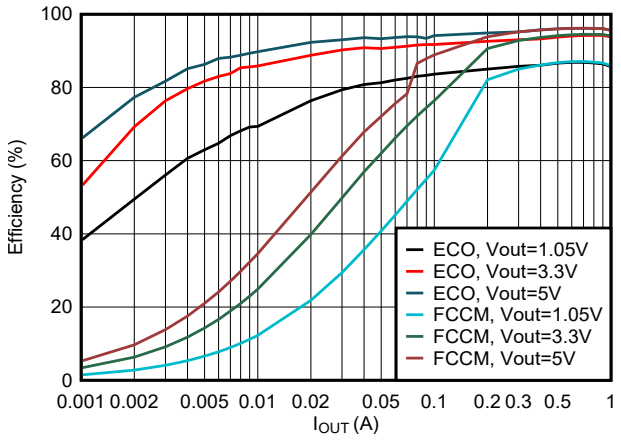
The TPS561243 operates in Eco-mode, which maintains high efficiency during light load operation. The TPS561246 operates in FCCM mode, which keeps the same frequency and lower output ripple during all load conditions. The TPS56124x integrates complete protection including OCP, UVLO, OTP, and UVP with hiccup.

The TPS56224x is available in a 6-pin, 1.6mm × 1.6mm SOT563 (DRL) package. The junction temperature is specified from –40°C to 125°C.

Device Information

PART NUMBER	MODE	PACKAGE(1)	PACKAGE SIZE(2)
TPS561243	Eco-mode	DRL (SOT563, 6)	1.60mm × 1.60mm
TPS561246	FCCM mode		

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



TPS56124x Efficiency at Vin = 12V

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4 Pin Configuration and Functions

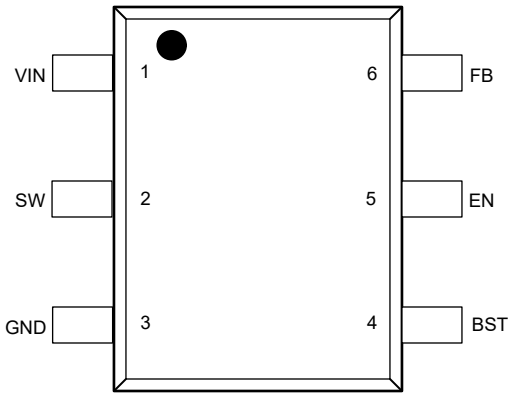

Figure 4-1. 6-Pin SOT563 DRL Package (Top View)

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
VIN	1	I	Input voltage supply pin
SW	2	O	Switch node connection between high-side NFET and low-side NFET
GND	3	—	Ground pin source terminal of low-side power NFET, as well as the ground terminal for the control circuit. Connect sensitive FB to this GND at a single point.
BST	4	O	Supply input for the high-side NFET gate drive circuit. Connect a 0.1µF capacitor between the BST and SW pin.
EN	5	I	Enable input control. Active high and must be pulled up to enable the device.
FB	6	I	Converter feedback input. Connect to the output voltage with feedback resistor divider.

(1) I = input, O = output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	19	V
Input voltage	FB, EN	–0.3	6	V
Input voltage	GND	–0.3	0.3	V
Output voltage	BST	–0.3	25	V
Output voltage	BST (< 20ns)	–0.3	27	V
Output voltage	SW	–2	19	V
Output voltage	SW (< 20ns)	–6.5	21	V
Operating junction temperature range, T_J		–40	150	°C
Storage temperature, T_{stg}	Storage temperature, Tstg	–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage	VIN	4.2		17	V
Input voltage	FB, EN	–0.1		5.5	V
Input voltage	GND	–0.1		0.1	V
Output voltage	BST	–0.1		23	V
Output voltage	BST (< 20ns)	–0.1		25	V
Output voltage	SW	–1		17	V
Output voltage	SW (< 20ns)	–6		19	V
Output Current	IO	0		1	A
T_J	Operating junction temperature	–40		125	°C
T_{stg}	Storage temperature	–40		150	°C

5.4 Thermal Information

THERMAL METRIC(1)		DRL (SOT-563) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	147.4	°C/W
$R_{\theta JA\_effective}$	Junction-to-ambient thermal resistance on EVM board	73(2)	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	75.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.1	°C/W
Y_{JB}	Junction-to-board characterization parameter	31.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.
(2) This $R_{\theta JA\_effective}$ is tested on TPS562243EVM board (2 layer, copper thickness of top and bottom layer are 2oz) at TA = 25ºC.

5.5 Electrical Characteristics

Over operating T_J = –40°C – 125°C, V_{IN} = 12V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY VOLTAGE						
VIN	Input voltage range		4.2		17	V
I_{VIN}	VIN supply current	No load, V_{EN} = 1.5V, non-switching, ECO version		110		µA
		No load, V_{EN} = 1.5V, VFB = 0.9V, FCCM version (1)		350		µA
I_{INSDN}	VIN shutdown current	V_{EN} = 0V		7		µA
UVLO						
UVLO	VIN undervoltage lockout	Wake up VIN voltage	3.6	3.8	4	V
UVLO	VIN undervoltage lockout	Shut down VIN voltage	3.2	3.4	3.6	V
UVLO	VIN undervoltage lockout	Hysteresis VIN voltage		400		mV
FEEDBACK VOLTAGE						
V_{FB}	FB voltage	T_J = 25°C, Vin = 4.2 – 17V	591	600	609	mV
V_{FB}	FB voltage	T_J = –40°C to 125°C, Vin = 4.2 – 17V	588	600	612	mV
MOSFET						
$R_{DS(ON)HI}$	High-side MOSFET Rds(on)	T_J = 25°C		100		mΩ
$R_{DS(ON)LO}$	Low-side MOSFET Rds(on)	T_J = 25°C		55		mΩ
DUTY CYCLE and FREQUENCY CONTROL						
F_{SW}	Switching frequency	V_{OUT} = 3.3V		1280		kHz
$T_{OFF(MIN)}$	Minimum off-time (1)	V_{FB} = 0.5V		100		ns
$T_{ON(MIN)}$	Minimum on-time (1)			55		ns
CURRENT LIMIT						
I_{OCL_LS}	Over current threshold	Valley current set point	1.2	2.8	3.6	A
I_{NOCL}	Negative over current threshold	Valley current set point	1	1.8	2.5	A
LOGIC THRESHOLD						
$V_{EN(ON)}$	EN threshold high-level		1.15	1.2	1.28	V
$V_{EN(OFF)}$	EN threshold low-level		0.93	1	1.05	V
V_{ENHYS}	EN hysteresis			200		mV
OUTPUT DISCHARGE and SOFT START						

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5.5 Electrical Characteristics (continued)

Over operating T_J = –40^{0}C – 125^{0}C, V_{IN} = 12V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{EN}	EN pulldown current	V_{EN} = 1.5V		1		uA
t_{SS}	Internal soft-start time	V_{OUT} from 0 to target value.		1.4		ms
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{UVP}	UVP trip threshold		55	60	65	%
t_{UVPDLY}	UVP prop deglitch			256		us
t_{UVPON}	In continuous hiccup mode, the switching time	Hard short, UVP detect		1.5		ms
t_{UVPOFF}	In continuous hiccup mode, non switching time	Hard short, UVP detect		13		ms
THERMAL PROTECTION						
T_{OTP}	OTP trip threshold			155		°C
T_{OTPHSY}	OTP hysteresis			20		°C

(1) Specified by design

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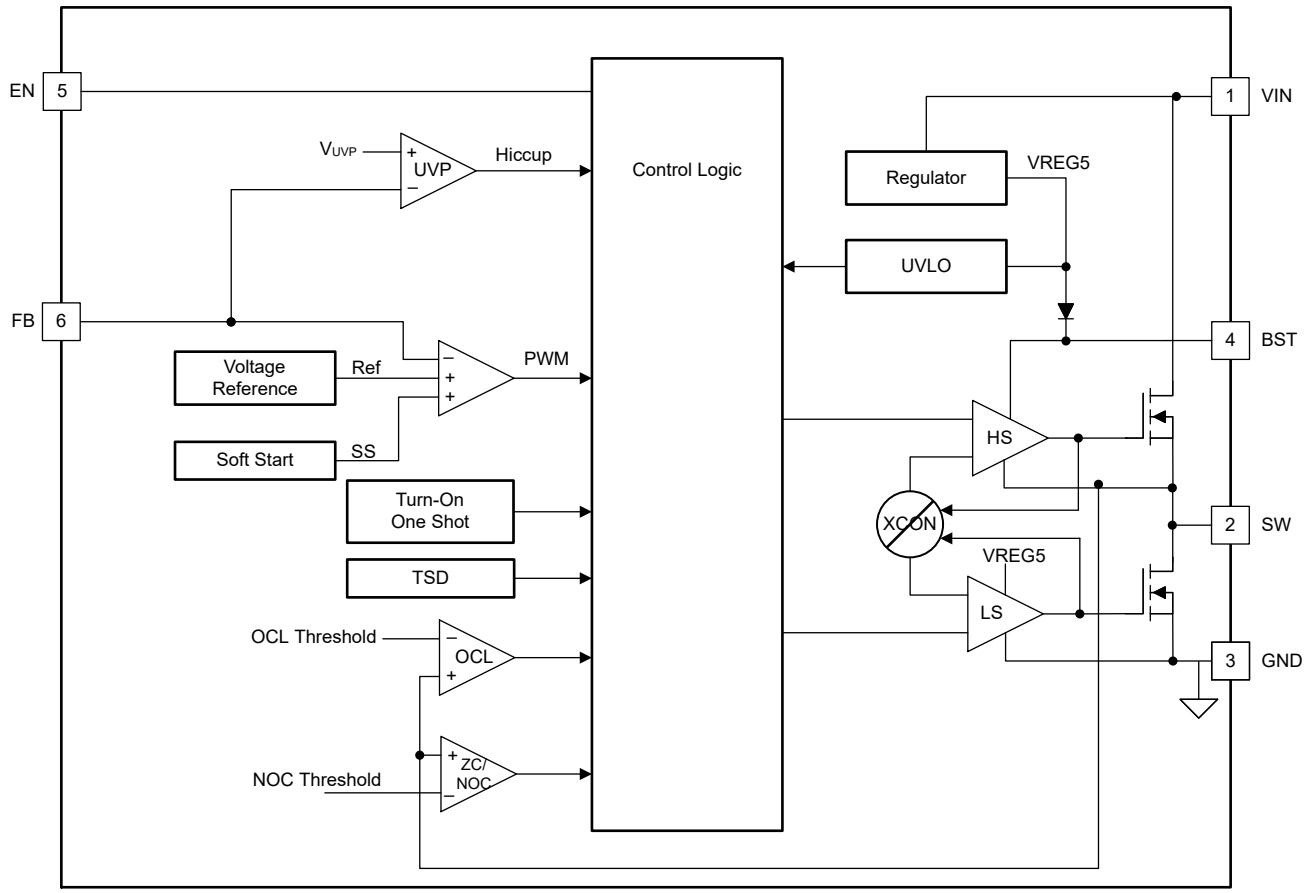
6 Detailed Description

6.1 Overview

The TPS56124x is a 1A, integrated FETs, synchronous step-down buck converter that can operate from 4.2V to 17V input voltage and 0.6V to 7V output voltage. The device employs D-CAP3 control mode that provides an accurate feedback voltage and a fast transient response with no external compensation components. The proprietary D-CAP3 control mode enables low external component count, ease of design, and optimization of the power design for cost, size and efficiency. The topology provides a seamless transition between CCM operating mode at higher load condition and DCM operation at lighter load condition.

The Eco-mode version allows the TPS561243 to maintain high efficiency at light load. The FCCM mode version allows the TPS561246 to maintain a fixed switching frequency and lower output voltage ripple. The TPS56124x is able to adapt to both low equivalent series resistance (ESR) output capacitors such as POSCAP or SP-CAP and ultra-low ESR ceramic capacitors.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Adaptive On-Time Control and PWM Operation

The TPS56124x implements D-CAP3 control scheme that supports adaptive on-time pulse width modulation (PWM) control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration, with both low-ESR and ceramic output capacitors. The D-CAP3 control scheme is stable even with virtually no ripple at the output. The TPS56124x also includes an error amplifier that makes the output voltage very accurate.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after the internal one shot timer expires. This one shot duration is set proportional to the output voltage, V_O, and inversely

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proportional to the converter input voltage, V_{IN}, to maintain a pseudo-fixed frequency over the input voltage range, hence called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP3 control scheme.

6.3.2 Eco-mode Control

The TPS561243 is designed with advanced Eco-mode to maintain high light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to a point that the ripple valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode. The on-time is kept almost the same as in the continuous conduction mode so that discharging the output capacitor with smaller load current to the level of the reference voltage takes a longer time. This action makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. Use Equation 1 to calculate the transition point to the light load operation $I_{OUT(LL)}$ current.

$$I_{out(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (1)$$

6.3.3 Soft Start and Prebiased Soft Start

The TPS56124x has an internal 1.4ms soft start. When the EN pin becomes high, the internal soft start function begins ramping up the reference voltage to the PWM comparator.

If the output capacitor is prebiased at start-up, the device initiates switching and start ramping up only after the internal reference voltage becomes greater than the feedback voltage V_{FB}. This scheme makes sure that the converters ramp up smoothly into the regulation point.

6.3.4 Large Duty Operation

The TPS56124x can support large duty operations up to 95% by smoothly dropping down the switching frequency. When input voltage V_{IN} < 7V and V_{FB} is lower than internal reference voltage, the switching frequency is allowed to smoothly drop to make T_{ON} extended to keep output voltage and improve the load transient performance. The minimum switching frequency is limited to about 400kHz.

6.3.5 Current Protection

The output overcurrent limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the OFF state by measuring the low side FET drain to source voltage. This voltage is proportional to the switch current. To improve the accuracy, the voltage sensing is temperature compensated.

During the on time of the high side FET switch, the switch current increases with a linear rate determined by V_{IN}, V_{OUT}, the on-time and the output inductor value. During the on time of the low side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{out}. If the monitored current is above the OCL level, the converter maintains low side FET on and delays the creation of a new set pulse, even the voltage feedback loop requires one, until the current level becomes OCL level or lower. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of overcurrent protection. The load current is higher than the overcurrent threshold by one half of the peak-to-peak inductor ripple current. Also, when the current is being limited, the output voltage tends to fall as the demanded load current can be higher than the current available from the converter. This event can even cause the output voltage to fall. When the FB voltage falls below the UVP threshold voltage, the UVP comparator detects the fall. Then, the device shuts down after the UVP delay time and re-starts after the hiccup time.

When the overcurrent condition is removed, the output voltage returns to the regulated value.

The TPS561246 is an FCCM mode part. In this mode, the device has negative inductor current at light load. The device has NOC (negative overcurrent) protection to avoid too large negative current. NOC protection detects the valley of inductor current. When the valley value of inductor current exceeds the NOC threshold, the IC turns off the low side then turns on the high side. When NOC protection is triggered eight times continuously, IC turns off both high side FET and low side FET. When the NOC condition is removed and output voltage returns to the target value, the device returns to normal switching.

Because the TPS561246 is an FCCM mode part, if the inductance is so small that the device triggers NOC, the output voltage becomes higher than the target value. The minimum inductance is identified as Equation 2.

$$L = \frac{V_{out} \times \left(1 - \frac{V_{out}}{V_{in}}\right)}{2 \times Frequency \times NOC_{min}} \quad (2)$$

6.3.6 Enable Circuit

The EN pin controls the turn-on and turn-off of the device. When the EN pin voltage is above the turn-on threshold, the device starts switching. When the EN pin voltage falls below the turn-off threshold, the device stops switching. The default status is low because there is a 1uA pulldown current in internal IC.

EN can be controlled by a typical resistor divider circuit from Vin or by a voltage of lower than 5.5V.

The TPS56124x also allows EN to connect to Vin with a pullup resistor only. TI suggests the value of the pullup resistor be 100kohm as EN voltage is clamped by a Zener diode and this Zener diode is not allowed to go through large current. The pullup resistor R1 is not allowed to be smaller than 80kohm, and TI suggests R1 also not be too large to avoid EN not being able to turn on. The recommended value range for the pullup resistor R1 is 80kohm to 3Mohm and 100kohm is the best recommended choice.

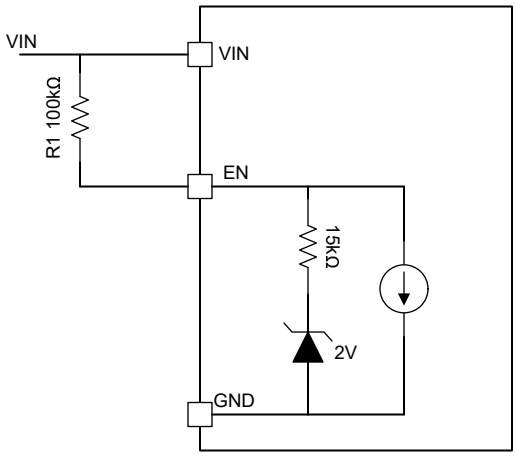

Figure 6-1. EN Block Circuit

6.3.7 Undervoltage Lockout (UVLO) Protection

UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. This protection is non-latching.

6.3.8 Thermal Shutdown

The device monitors the temperature of the device. If the temperature exceeds the threshold value (typically 155°C), the device is shut off. This protection is a non-latch protection.

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6.4 Device Functional Modes

6.4.1 Eco-mode Operation

The TPS561243 operates in Eco-mode, which maintains high efficiency at light load. As the output current decreases from heavy load conditions, the inductor current is also reduced and eventually comes to a point where the rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode. The on time is kept almost the same as in continuous conduction mode so that discharging the output capacitor with smaller load current to the level of the reference voltage takes longer. This fact makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high.

6.4.2 FCCM Mode Operation

The TPS561246 operates in forced CCM (FCCM) mode, which keeps the converter operating in continuous current mode during light load condition and allows the inductor current to become negative. During FCCM mode, the switching frequency (F_{SW}) is maintained at an almost constant level over the entire load range, which is designed for applications requiring tight control of the switching frequency and output voltage ripple at the cost of lower efficiency under light load.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The TPS56124x device is a typical buck DC/DC converter to convert a higher DC voltage to a lower DC voltage with a maximum available output current of 1A. The following design procedure can be used to select component values for TPS56124x. Alternately, the WEBENCH® software can be used to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

7.2 Typical Application

The TPS56124x application schematic in Figure 7-1 was developed to meet the requirements in Table 7-1. This section provides the design procedure.

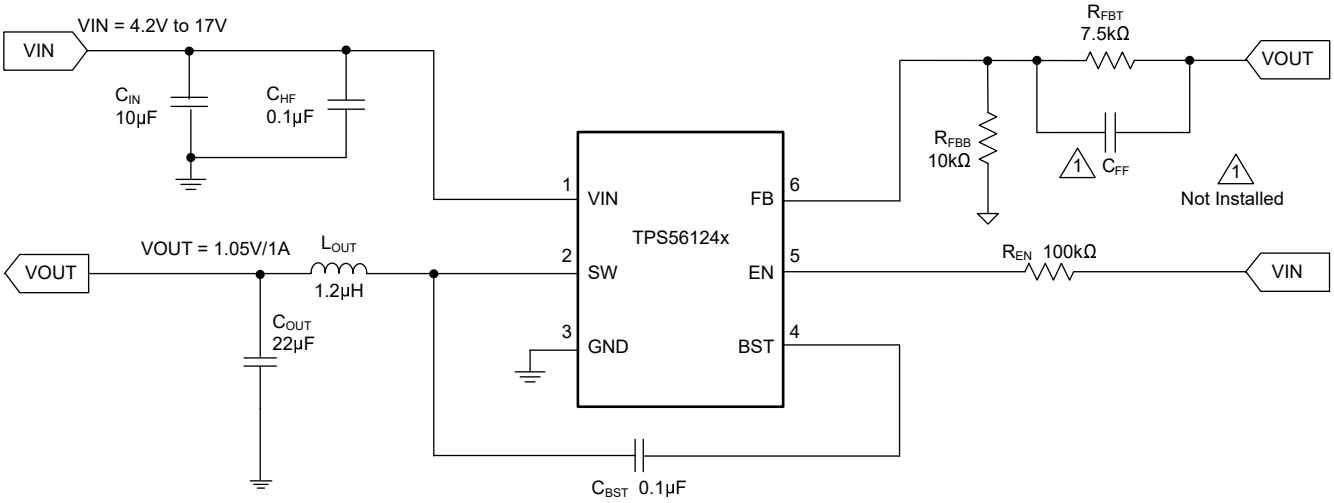

Figure 7-1. TPS56124x 1.05V/1A Reference Design

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7.2.1 Design Requirements

Table 7-1 shows the design parameters for this application.

Table 7-1. Design Parameters

	Parameter	Conditions	MIN	TYP	MAX	Unit
V_{OUT}	Output voltage			1.05		V
I_{OUT}	Output current			1		A
ΔV_{OUT}	Transient response	0.1A – 0.9A load step, 0.8A/µs slew rate		±2% × V_{OUT}		V
V_{IN}	Input voltage		4.2	12	17	V
$V_{OUT(ripple)}$	Output voltage ripple	CCM condition		8		mV
F_{SW}	Switching frequency			1.2		MHz
T_A	Ambient temperature			25		°C

7.2.2 Detailed Design Procedure

7.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS56124x device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

7.2.2.2 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the FB pin. TI recommends to use 1% tolerance or better divider resistors. Start by using Equation 3 to calculate V_{OUT}.

To improve the efficiency at very light loads, consider using larger value resistors. Too high of the resistance can make the circuit more susceptible to noise and voltage errors introduced from the FB input current are more noticeable.

$$V_{OUT} = 0.6 \times \left(1 + \frac{RFBT}{RFBB}\right) \quad (3)$$

7.2.2.3 Output Filter Selection

The LC filter used as the output filter has a double pole at Equation 4. In this equation, C_{OUT} must use effective value after derating, not nominal value.

$$Frequency_{doublepole} = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} \quad (4)$$

For any control topology that is compensated internally, there is a range of the output filter that the control topology can support. At low frequency, the overall loop gain is set by the output set point resistor divider network and the internal gain of the device. The low frequency phase is 180°. At the output filter pole frequency, the gain rolls off with a rate of –40dB per decade and the phase has a 180 degree drop. The internal ripple generation network introduces a high-frequency zero that reduces the gain roll off from –40dB to –20dB per

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decade and leads to the 90 degree phase boost. The high frequency zero brought by the internal ripple injection circuit is about 160kHz. TI recommends the double pole frequency brought by the selected inductor and capacitor to be located at about 40kHz, so that the phase boost provided by this high frequency zero provides adequate phase margin for the stability requirement. For output voltage higher than 2V, TI suggests to add a C_{FF} capacitor to increase the bandwidth and the phase margin. The C_{FF} range suggested is from 10pF to 100pF. The crossover frequency of the overall system must usually be targeted to be less than one-third of the switching frequency.

Table 7-2. Recommended Component Values

OUTPUT VOLTAGE (V)	L_{OUT} (uH)	C_{OUT}(uF)	C_{OUT}(uF) (1) Range	R_{FBT} (kΩ)	R_{FBB} (kΩ)	C_{FF}(pF)
0.6	1	22	22-88	0	10.0	-
1.05	1.2	22	22-44	7.5	10.0	-
2.5	2.2	22	22-44	95.0	30.0	33
3.3	3.3	22	22-44	135.0	30.0	33
5	4.7	22	22-44	220.0	30.0	47
7	4.7	22	22-66	320.0	30.0	47

(1) A ceramic capacitor is used in this table. All the C_{OUT} values are after derating.

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using Equation 5, Equation 6, and Equation 7. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

$$I_{P-P} = \frac{V_{OUT}}{V_{IN(Max)}} \times \frac{V_{IN(Max)} - V_{OUT}}{L_{OUT} \times f_{SW}} \quad (5)$$

$$I_{PEAK} = I_O + \frac{I_{P-P}}{2} \quad (6)$$

$$I_{LO(RMS)} = \sqrt{I_O^2 + \frac{1}{12} \times I_{P-P}^2} \quad (7)$$

For this design example, the calculated peak current is 1.34A and the calculated RMS current is 1.02A. The inductor used is WE 74438357012.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS561243 is intended for use with ceramic or other low ESR capacitors. TI recommends to use 1× 22µF output cap. Use Equation 8 to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_{OUT} \times f_{SW}} \quad (8)$$

For this design, one MuRata GRM21BR61A226ME44L 22µF output capacitor can be used. The typical ESR is 2mΩ each. The calculated RMS current is 0.2A and each output capacitor is rated for 4A.

7.2.2.4 Input Capacitor Selection

The TPS561243 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. TI recommends a ceramic capacitor over 10µF for the decoupling capacitor. An additional 0.1µF capacitor CHF from pin 1 V_{IN} to ground is optional to provide additional high frequency filtering. The capacitor voltage rating must be greater than the maximum input voltage.

7.2.2.5 Bootstrap Capacitor Selection

A 0.1µF ceramic capacitor must be connected between the BST to SW pin for proper operation. TI recommends to use a ceramic capacitor.

ADVANCE INFORMATION

ADVANCE INFORMATION

7.2.3 Application Curves

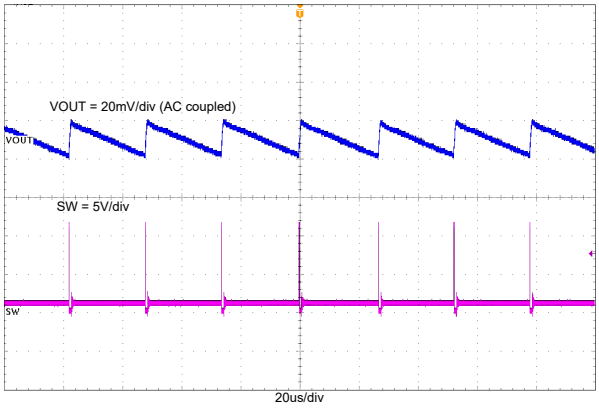

Figure 7-2. TPS561243 Output Voltage Ripple With 0.01A Loading

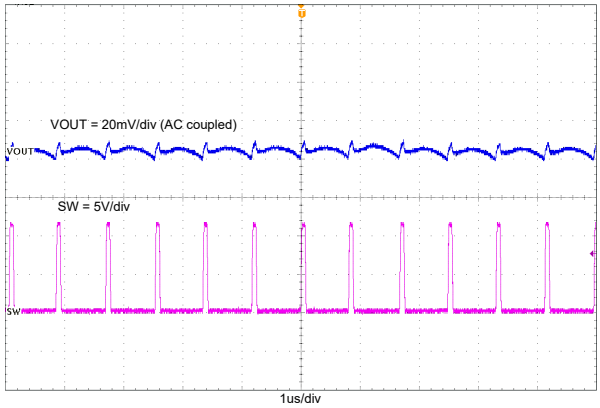

Figure 7-3. TPS561246 Output Voltage Ripple With 0.01A Loading

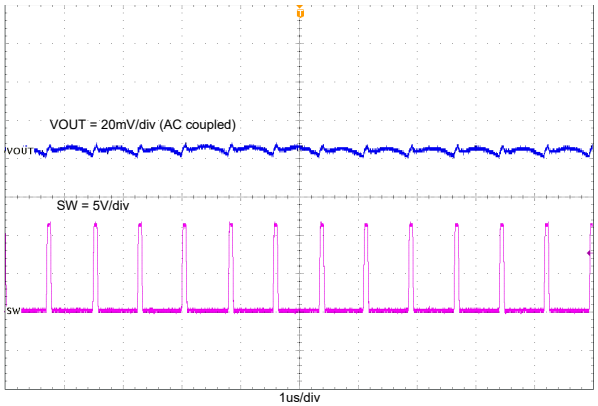

Figure 7-4. TPS561243 Output Voltage Ripple With 1A Loading

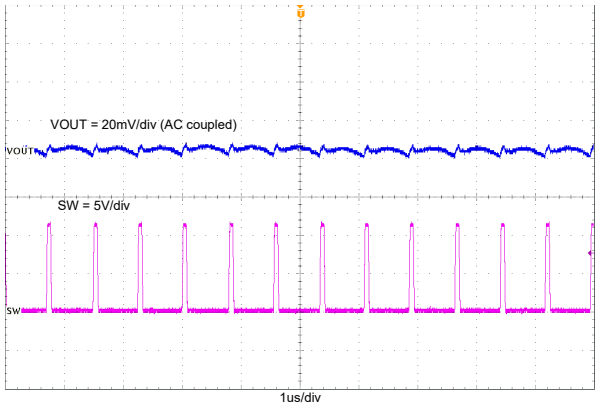

Figure 7-5. TPS561246 Output Voltage Ripple With 1A Loading

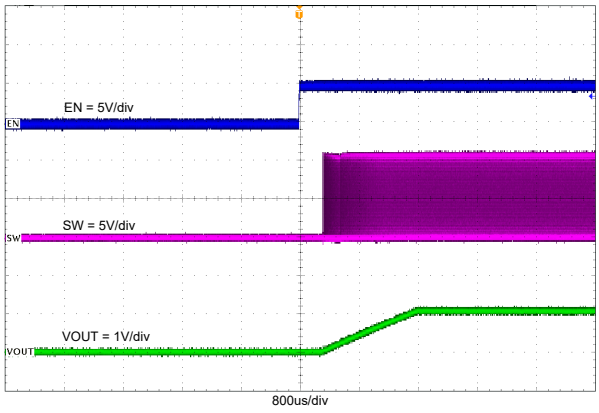

Figure 7-6. TPS561243 Enable On With 1A Loading

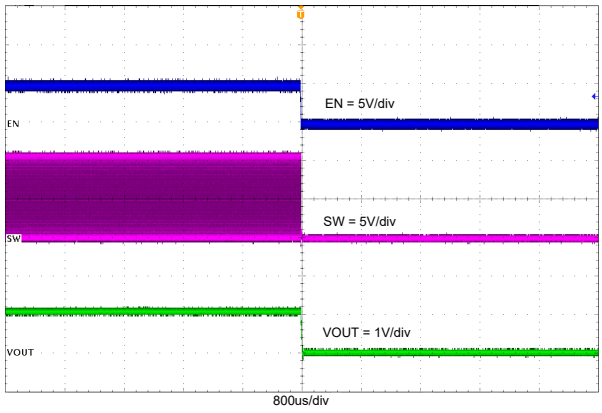

Figure 7-7. TPS561243 Enable Off With 1A Loading

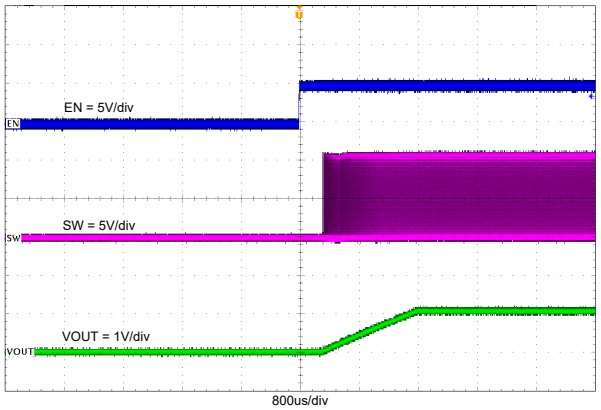

Figure 7-8. TPS561246 Enable On With 1A Loading

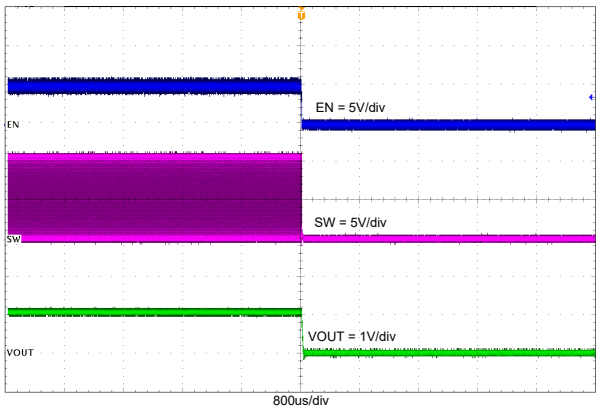

Figure 7-9. TPS561246 Enable Off With 1A Loading

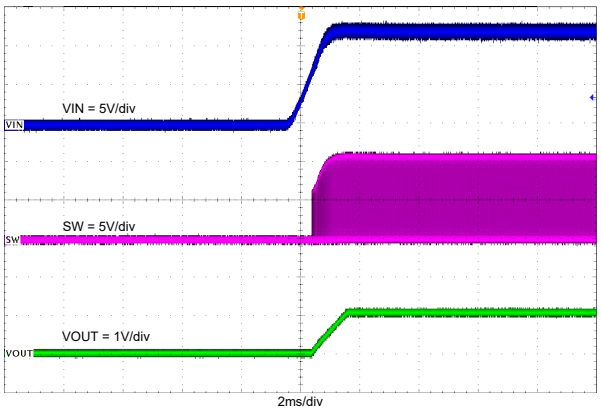

Figure 7-10. TPS561243 Power On With 1A Loading

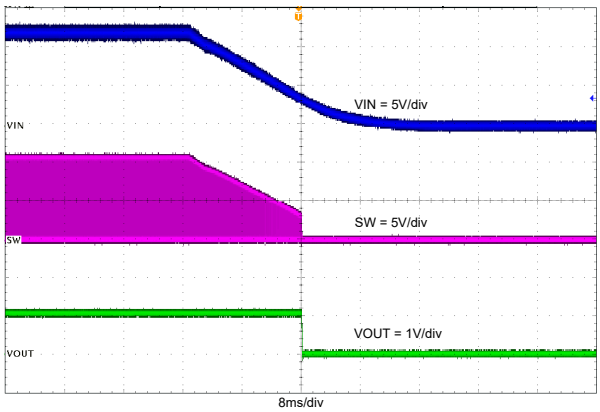

Figure 7-11. TPS561243 Power Off With 1A Loading

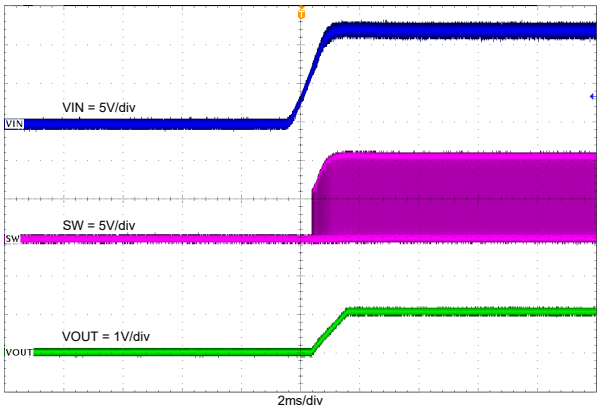

Figure 7-12. TPS561246 Power On With 1A Loading

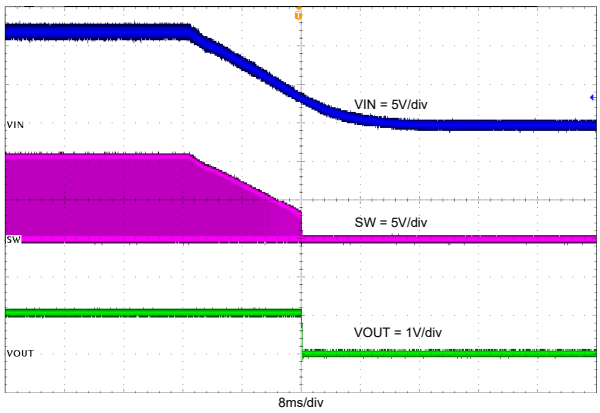

Figure 7-13. TPS561246 Power Off With 1A Loading

ADVANCE INFORMATION

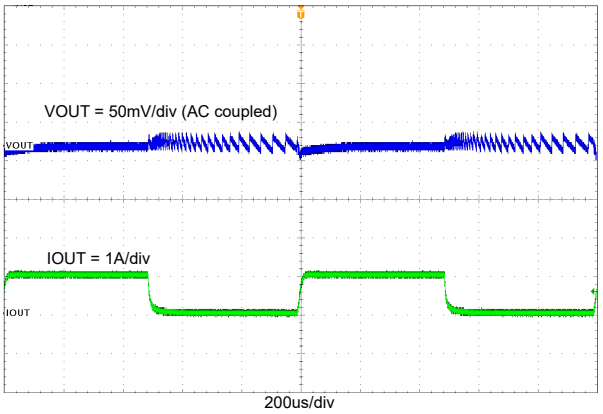

Figure 7-14. TPS561243 Load Transient With 0A to 1A

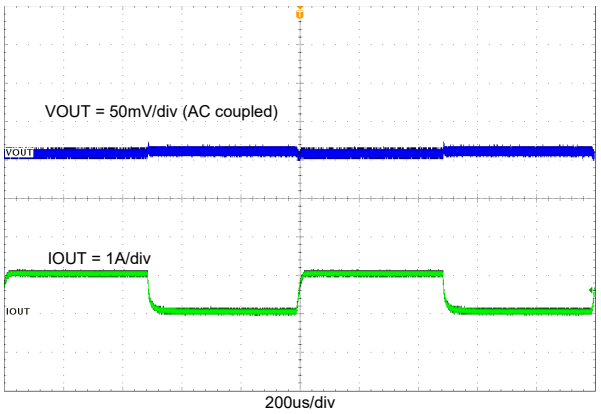

Figure 7-15. TPS561246 Load Transient With 0A to 1A

7.3 Power Supply Recommendations

The TPS56124x is designed to operate from input supply voltages in the range of 4.2V to 17V. Buck converters require the input voltage to be higher than the output voltage for proper operation. The maximum duty is 95%.

7.4 Layout

7.4.1 Layout Guidelines

1. Make V_{IN} and GND traces as wide as possible to reduce trace impedance. The wide areas can also benefit for heat dissipation.
2. Place the input capacitor and output capacitor as close to the device as possible to minimize trace impedance.
3. Provide sufficient vias for the input capacitor and output capacitor.
4. Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
5. Do not allow switching current to flow under the device.
6. Connect a separate VOUT path to the upper feedback resistor.
7. Make a Kelvin connection to the GND pin for the feedback path.
8. Place a voltage feedback loop away from the high voltage switching trace, and preferably with ground shield.
9. Make the trace of the FB node as small as possible to avoid noise coupling.
10. Make the GND trace between the output capacitor and the GND pin as wide as possible to minimize trace impedance.

ADVANCE INFORMATION

7.4.2 Layout Example

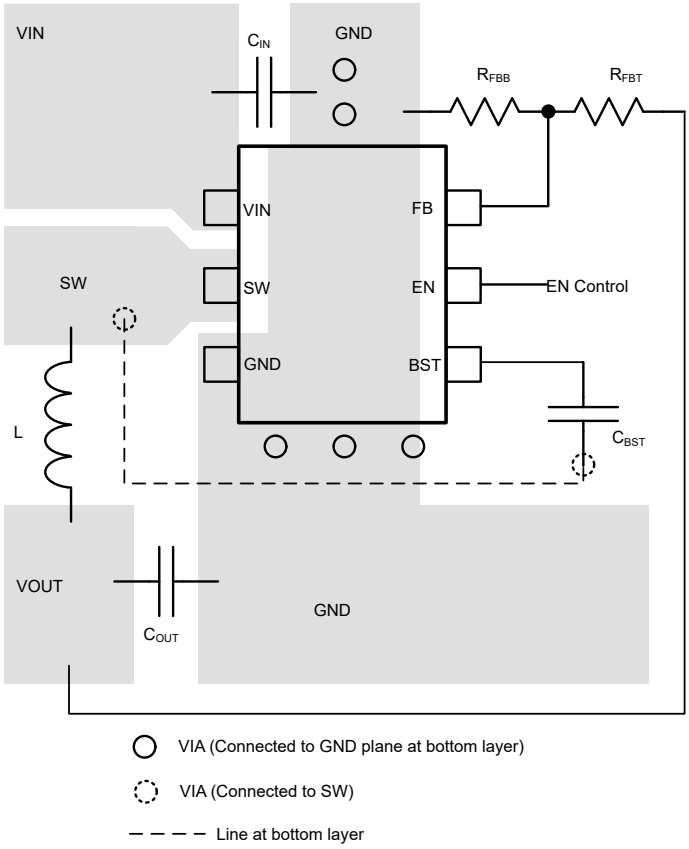

Figure 7-16. TPS56124x Layout

ADVANCE INFORMATION

ADVANCE INFORMATION

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS56124x device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.4 Trademarks

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WEBENCH® is a registered trademark of Texas Instruments.
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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

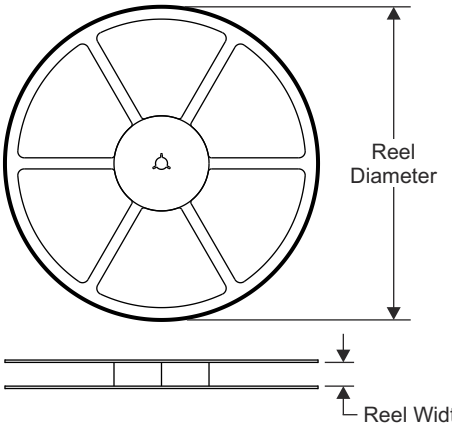
DATE	REVISION	NOTES
April 2024	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

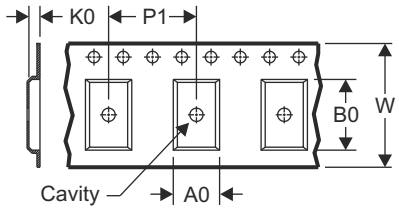
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10.1 Tape and Reel Information

REEL DIMENSIONS

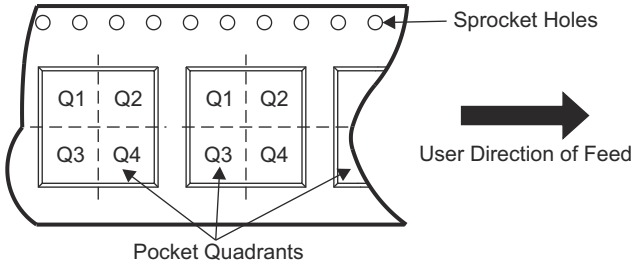


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

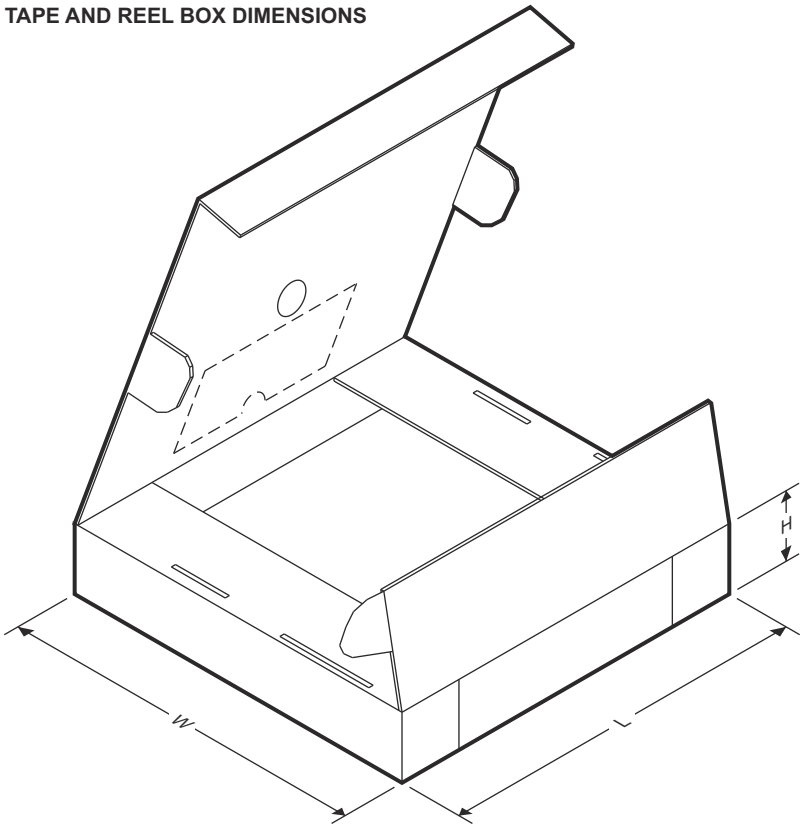


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS561243DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TPS561246DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3

ADVANCE INFORMATION

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



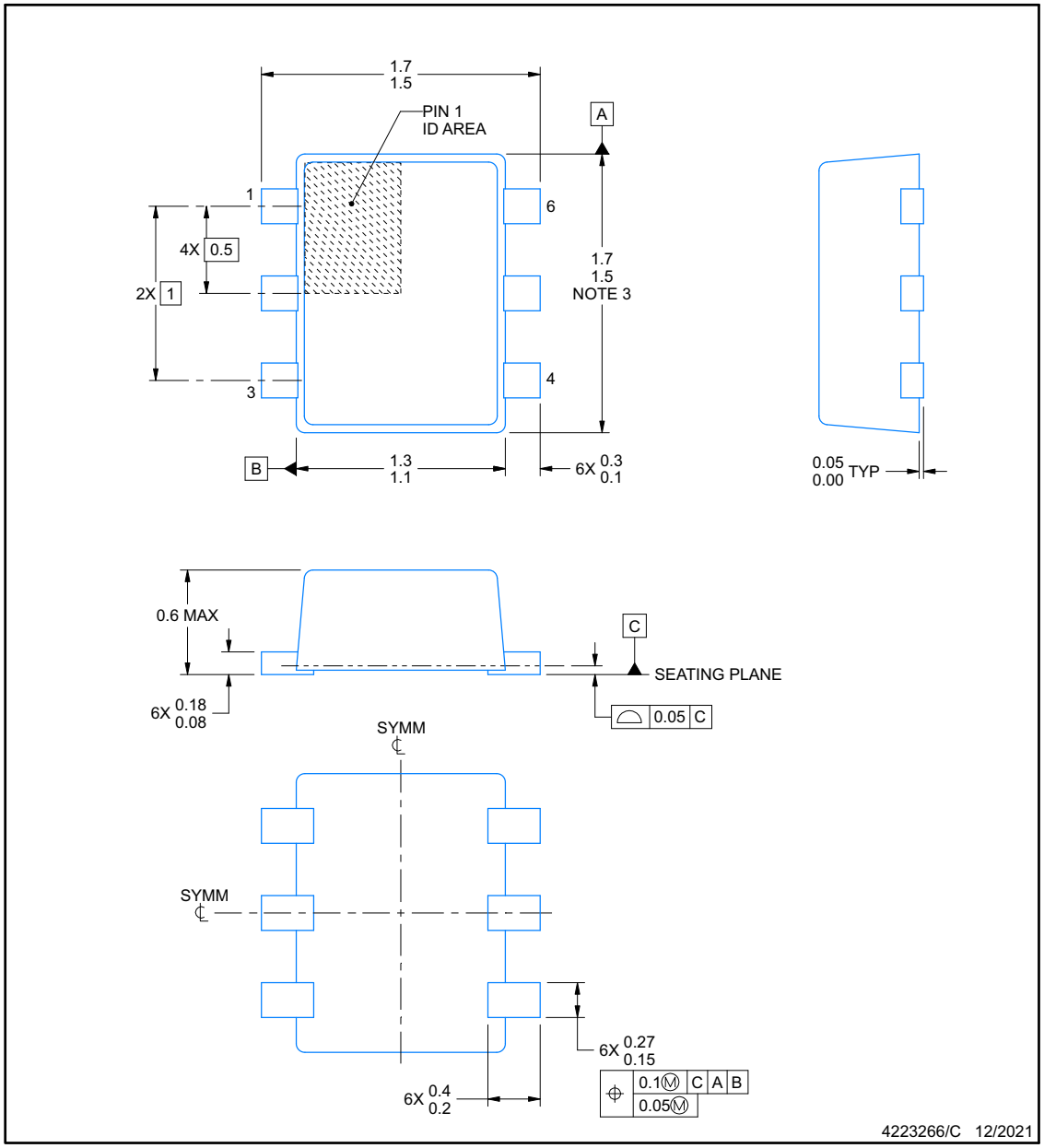
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS561243DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
TPS561246DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0

PACKAGE OUTLINE

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

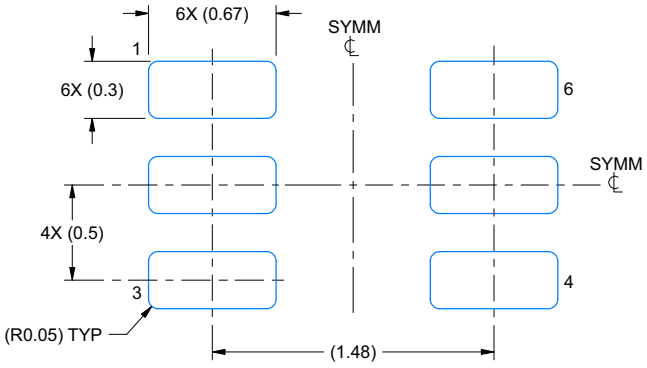
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

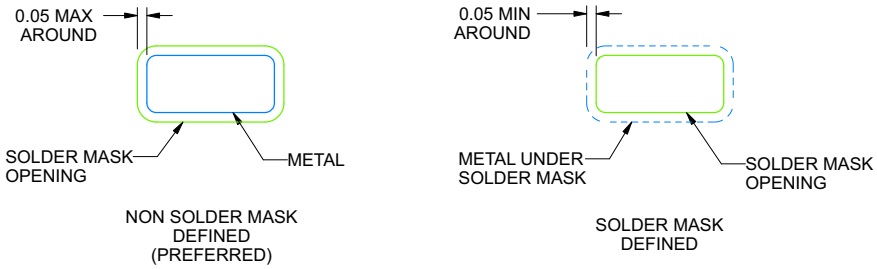
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4223266/C 12/2021

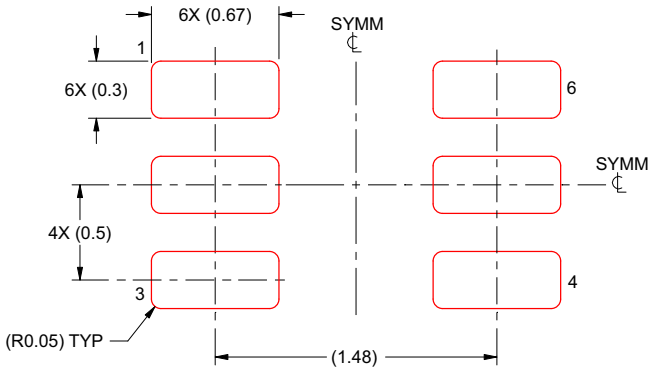
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A — **SOT - 0.6 mm max height**

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/C 12/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPS561243DRLR	ACTIVE	SOT-5X3	DRL	6	4000	TBD	Call TI	Call TI	-40 to 125		Samples
PTPS561246DRLR	ACTIVE	SOT-5X3	DRL	6	4000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

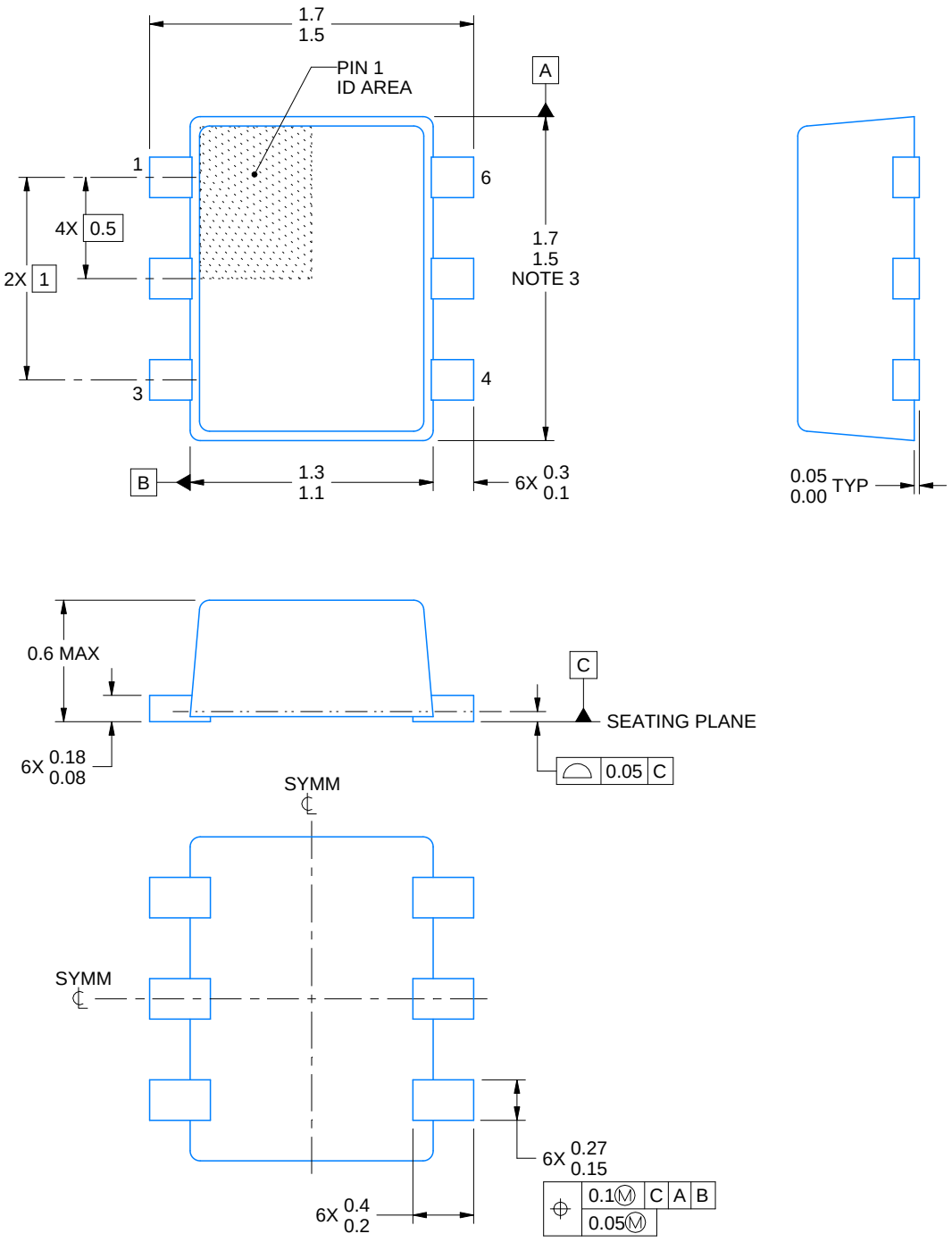
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



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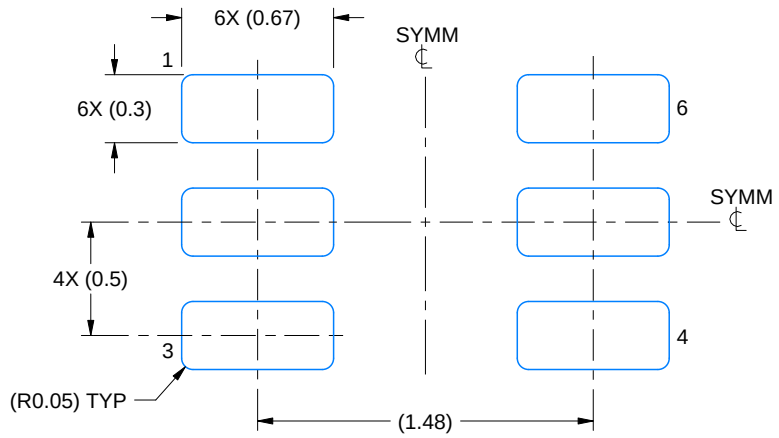
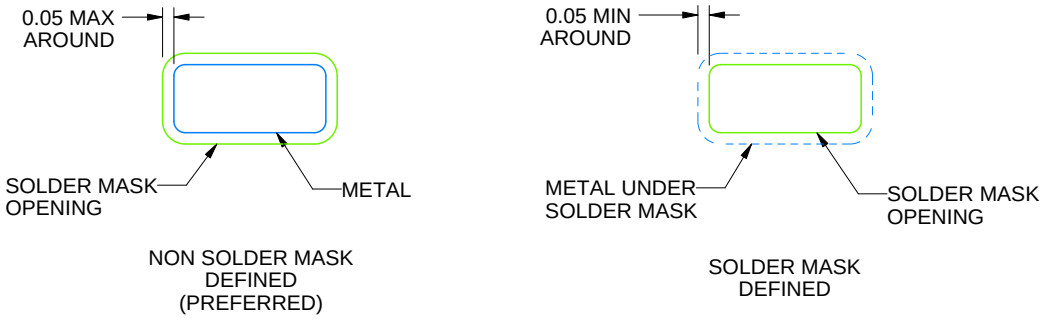


LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4223266/C 12/2021

NOTES: (continued)

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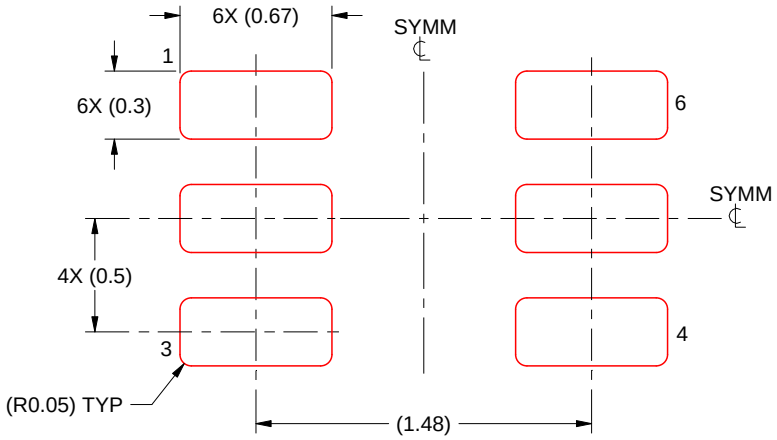
EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/C 12/2021

NOTES: (continued)

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9. Board assembly site may have different recommendations for stencil design.

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