TEXAS INSTRUMENTS

Modeling the ADS41XX family of components through IBIS

Texas Instruments

Date – September 18th, 2009

3-state CMOS buffer

The structure of the CMOS buffer in ADS41XX family of products is shown in Figure 1.1. The structure can be directly mapped to the structure of a 3-state output buffer as specified by the IBIS standard. So its model shall consist of

1. I-V characteristics of Power and Ground clamp as well as the pull-up and pull-down circuits.
2. V-t characteristics of output pin

Voltage levels of 0 Volts and 1.8 Volts correspond to logic levels of '0' and '1' at HI and LO at the input of the buffer.

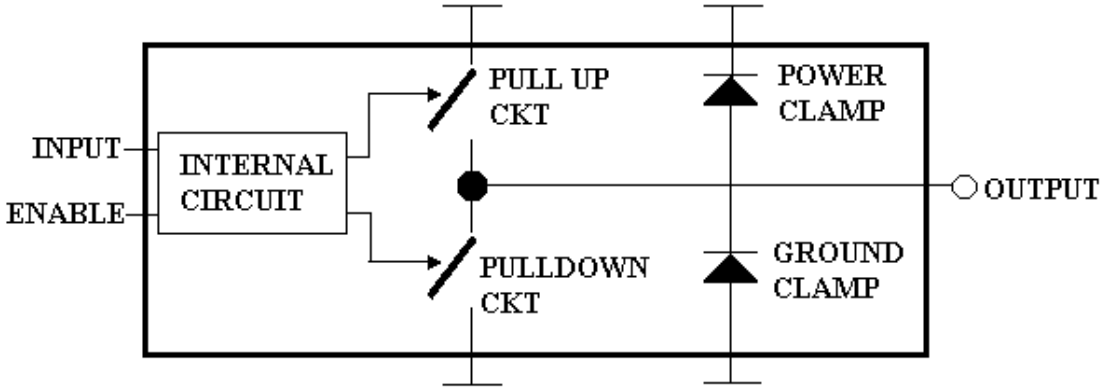

Figure 1.1 3-state CMOS output buffer structure

1.1 V-I tables for Pull-up and Power clamp

The Circuit setup used to extract the pull-up and power clamp data is shown in Fig. 1.2 Two sets of measurements are taken.

1 Measurement (a)
- Input is at HI
- Enable pin is at LO to deactivate output
- The voltage source VPIN is swept from -VDD to 2*VDD (as VSS = 0), where VDD = 1.8V, 1.7V or 1.9V (for typ, min and max corners). done by first giving a LO at the output enable pin
- The current flowing through VPIN is tabulated

2 Measurement (b)
- Input is at HI
- Enable pin is at HI to activate output
- The voltage source VPIN is swept from -VDD to 2*VDD (as VSS = 0), where VDD = 1.8V, 1.7V or 1.9V (for typ, min and max corners).
- The current flowing through VPIN is tabulated

The current measurements in (a) (for VPIN = VDD to 2VDD) are the Power clamp data, as only clamp circuits are active. The current measurement in (b) is sum of clamp circuit current and pull-up circuit current. So (b) - (a) gives the pull-up data.

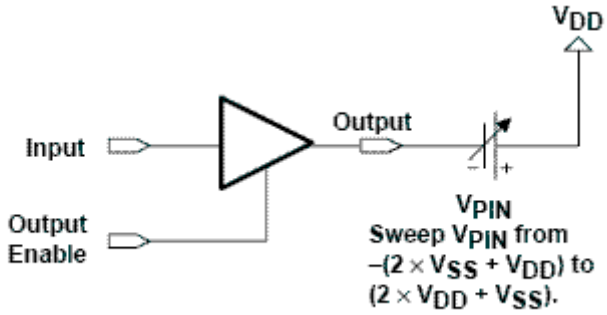

Figure 1.2 Circuit setup to extract Pull-up and Power clamp data

1.2 V-I tables for Pull-down and Ground clamp

The Circuit setup used to extract the pull-down and ground clamp data is shown in Fig. 1.3. Two sets of measurements are taken.

1. Measurement (a)
    - Input is at LO
    - Enable pin is at LO to deactivate output
    - The voltage source VPIN is swept from -VDD to 2*VDD (as VSS = 0), where VDD = 1.8V, 1.7V or 1.9V (for typ, min and max corners). done by first giving a LO at the output enable pin
    - The current flowing through VPIN is tabulated
2. Measurement (b)
    - Input is at LO
    - Enable pin is at HI to activate output
    - The voltage source VPIN is swept from -VDD to 2*VDD (as VSS = 0), where VDD = 1.8V, 1.7V or 1.9V (for typ, min and max corners).
    - The current flowing through VPIN is tabulated

The current measurements in (a) (for VPIN = -VDD to VDD) are tabulated as the Ground clamp data, as only clamp circuits are active. The current measurement in (b) is sum of clamp circuit current and pull-down circuit current. So (b) - (a) gives the pull-dow n data.

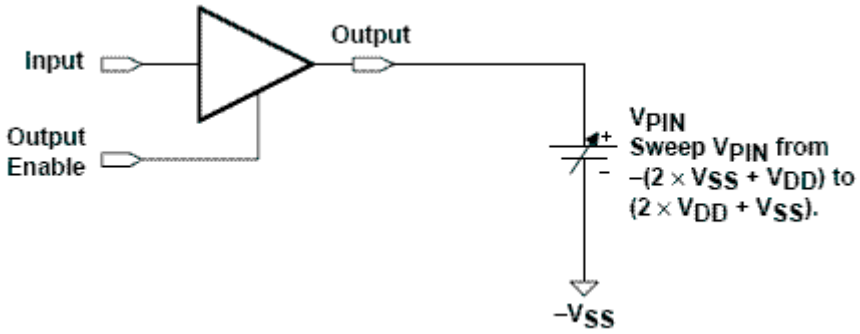

Figure 1.3 Circuit setup to extract Pull-down and Ground clamp data

1.3 Generating the V-t Data

Four V-t tables are generated using the setup shown in Figure 1.4. A step signal is given at input at voltage waveform at output is tabulated

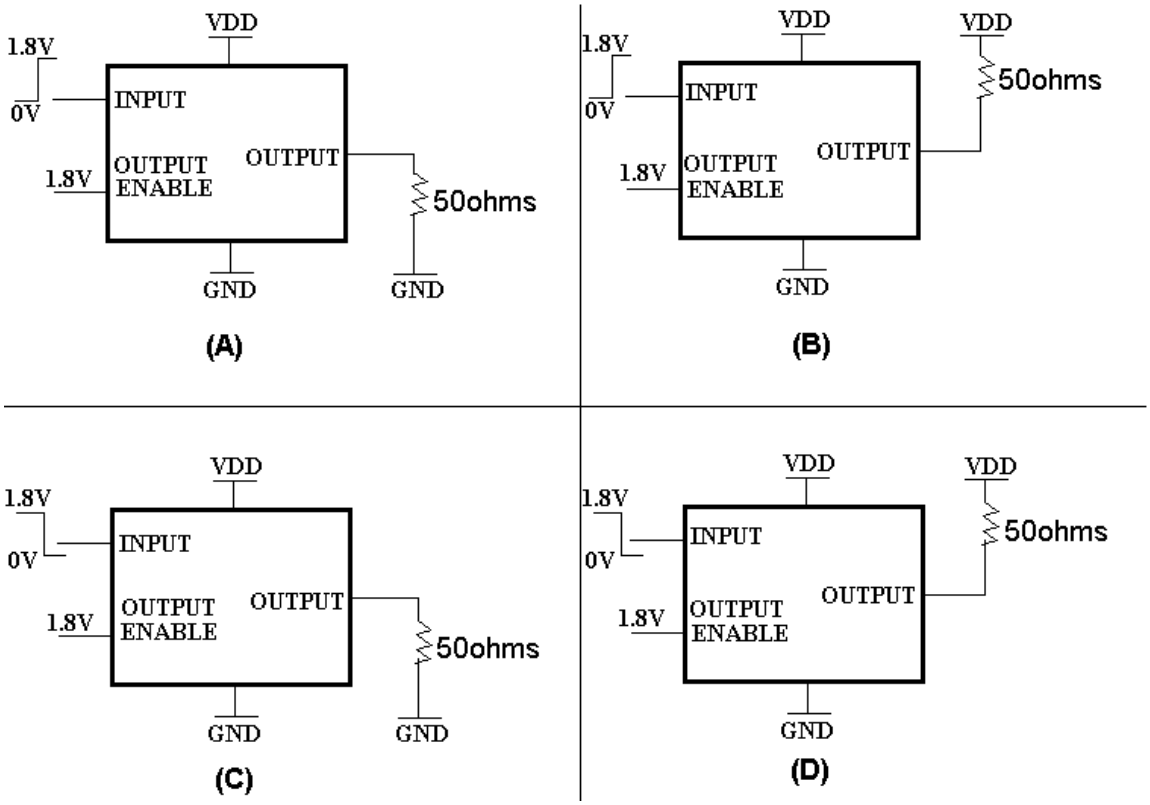

Figure 1.4 Circuit setup to extract the four V-t tables

1.4 Comparison of IBIS model with the actual circuit

To check how well the IBIS models shall model the actual circuit, the following SPICE simulations were done. The circuit set up is shown in Figure 1.5. In the first simulation the SPICE netlist of the buffer is used and in the second simulation the IBIS model of the buffer is used.

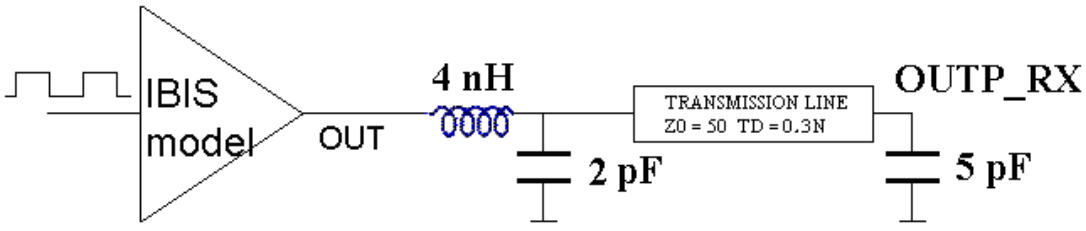

Figure 1.5 Circuit set up used in simulations for validation of the model

Simulations were also done with different values of the delay for the transmission line and load capacitance.

Figure 1.6 shows a comparison of the HSPICE simulation results obtained from the IBIS model with those from the actual circuit.

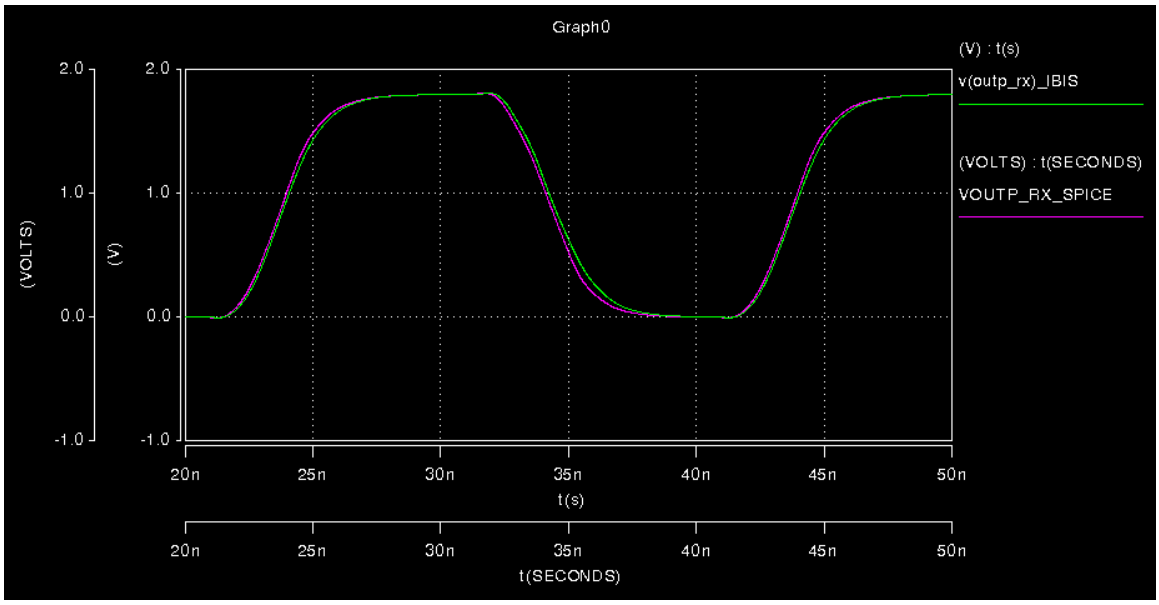

Figure 1.6 Output waveforms of simulation with IBIS model Vs. full-transistor netlist

As can be observed, there is a close match between the actual circuit and its IBIS model.

2. LVDS BUFFER

Method of modeling the LVDS buffer through IBIS

Since the LVDS buffer has differential inputs and differential outputs, some additional considerations are involved while modeling it through IBIS.

ADS41XX LVDS buffer architecture

The internal structure of the LVDS buffer in ADS41XX family of products is shown in Figure 2.1. For simplicity, the enable pin has not been shown. HI and LO refer to the differential input to the buffer. VH and VL are internally regulated voltages of values 1.45V and 0.75V respectively. LOUTP and LOUTM form the differential output.
The buffer consists of 4 MOS switches that connect or disconnect the appropriate regulated voltages VH and VL to the output through the equivalent on-resistance of the switch.

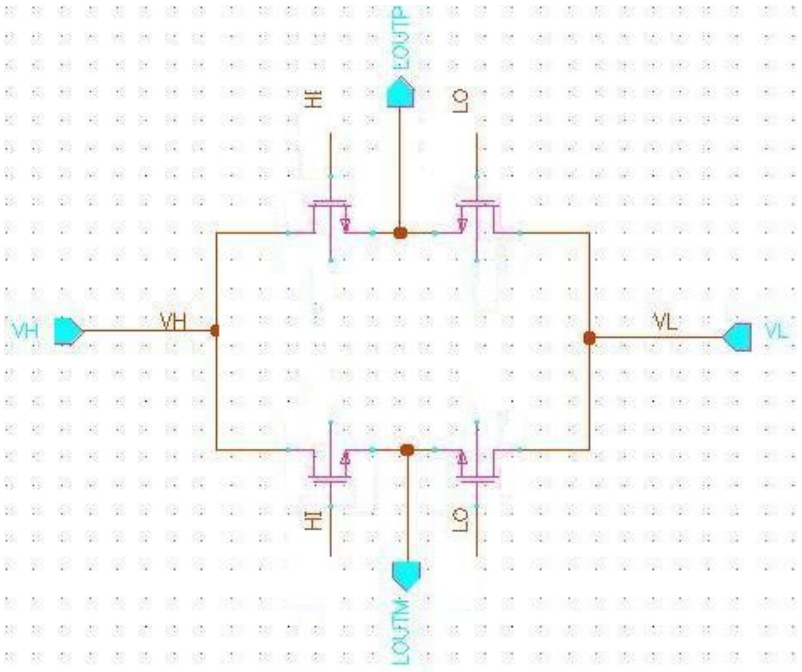

Figure 2.1. LVDS buffer architecture

Comparison of IBIS model with the actual circuit

The IBIS models were generated and compared with the actual circuit through SPICE simulations. Figure 2.2 shows the simulation environment for the actual LVDS buffer, while Figure 2.3 shows the identical environment used for the IBIS model.

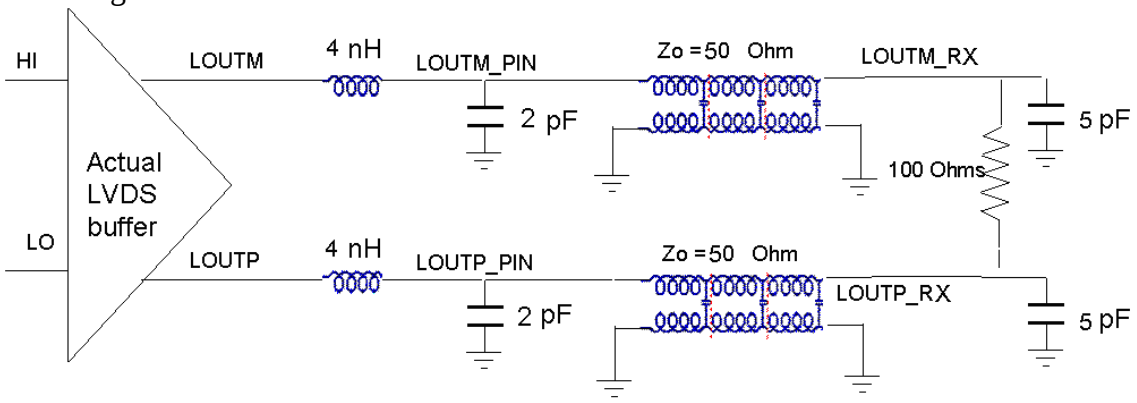

Figure 2.2. Simulation environment for the actual LVDS buffer

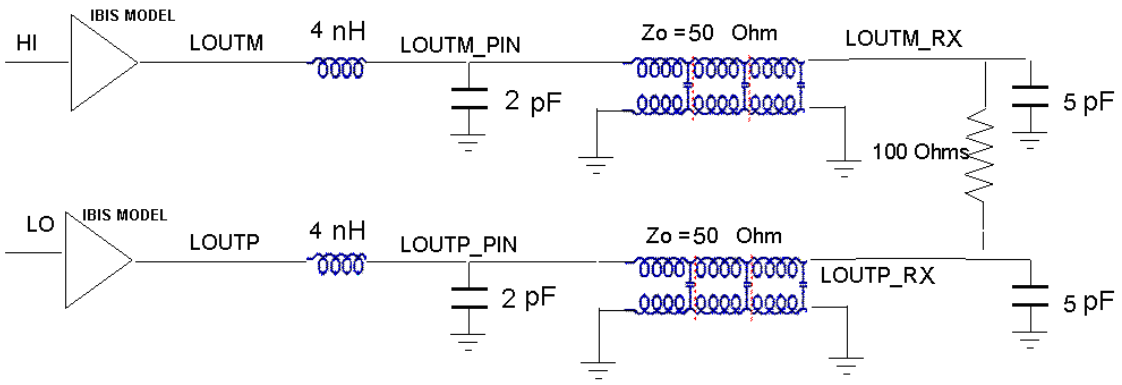

Figure 2.3. Simulation environment for the IBIS model of the LVDS buffer

Simulations were done with different values of the delay for the transmission line.

1. Figure 2.4 shows a comparison of the SPICE simulation results obtained from the IBIS model with those from the actual circuit. The delay of the transmission line was set to 0.50ns

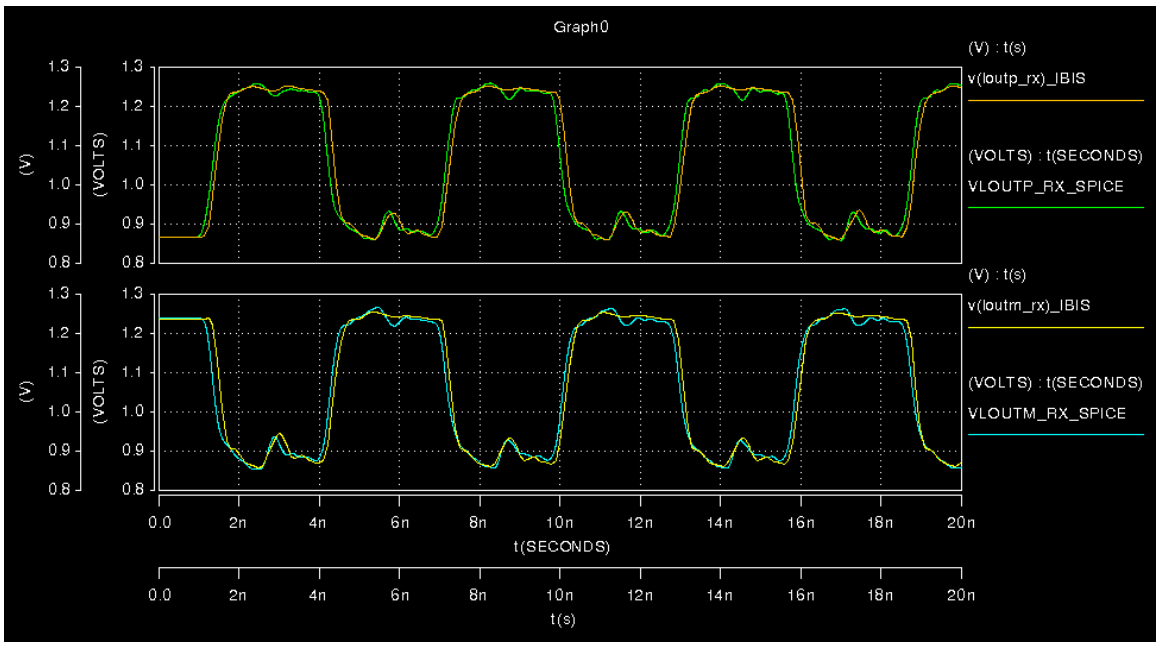

Figure 2.4. Comparison of results between full-transistor spice simulation and simulation using IBIS model for buffer.

As can be observed, there is a close match between the actual circuit and its IBIS model.

3. Input buffer for clock

The structure of the input buffer in ADS41XX family of products is shown in Figure 3.1. The inputs to the buffer are differential and internally it consists of clamping circuits and pull-up/pull-down circuits (as in any input buffer). In addition to them, there is a termination consisting of a capacitance C and 2 equal resistances R1 and R2 from each input to a common mode voltage of 0.9V.

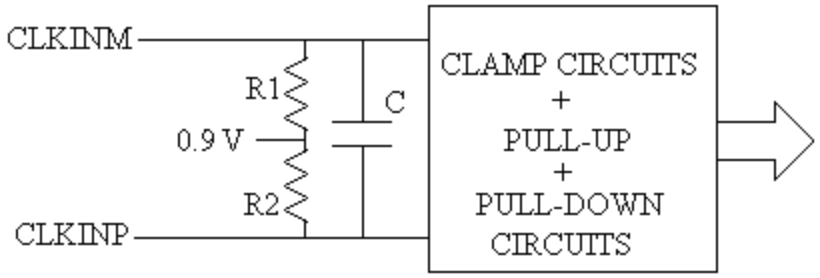

Figure 3.1 Structure of the input buffer in ADS41XX family

As it is an input buffer the pull-up/pull-down circuits shall not be characterized in the IBIS model. The differential input buffer plus R1 and R2 is modeled as combination of 2 single-input buffers and termination capacitance C is modeled as a series element. So the IBIS model file consists of:

1. A model for characterizing clamp circuits + termination resistance. Model type us ed is Terminator
2. A model for the termination capacitance. Model type used is Series

The input file to the simulator shall consist of 2 instances of the 1st model to represent the differential input and 1 instance of 2nd model to represent the capacitive termination between the differential inputs

3.1 Model for characterizing clamp circuits and termination resistance

The clamp circuit together with termination resistance (R1 or R2) shall be modeled using buffer type Terminator. The model name in the ibis file is ‘input’.

3.1.1 Extracting power clamp and ground clamp data

The setup for the CLAMP data extraction is as shown in Figure 3.2.

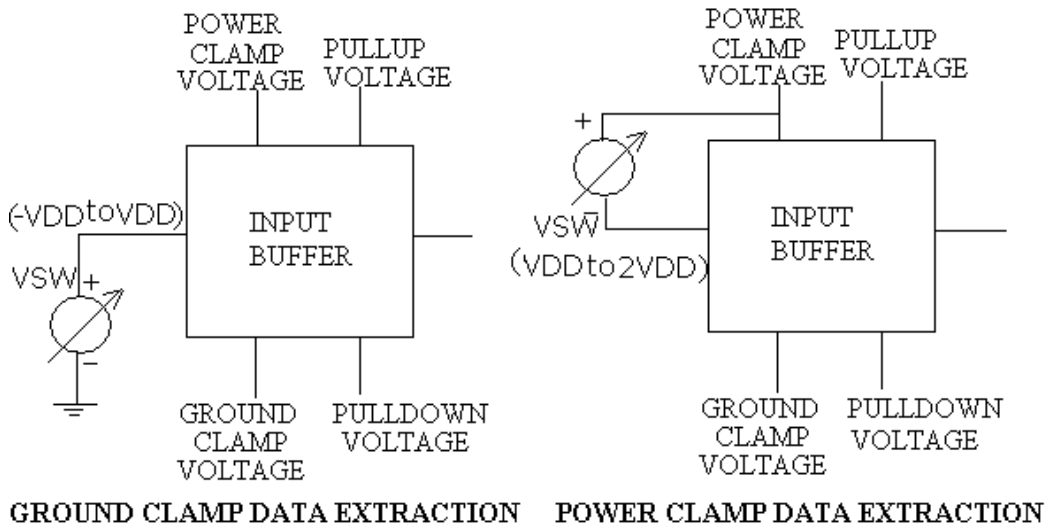

Figure 3.2 Circuit setup used to extract V-I tables

3.1.2 Termination resistance

As shown in Figure 3.1 the termination resistance is connected between input pin and a constant voltage of 0.9V. The Terminator buffer model has keywords [Rpower] and [Rgnd] to specify resistance between the pin to supply voltage and ground respectively. So we split the termination resistance into 2 parts ; one each to the supply and to the ground. The values of Rpower and Rgnd are obtained by solving

VDD*Rgnd / (Rpower + Rgnd) = 0.9

Rpower*Rgnd / (Rpower + Rgnd) = R1 (= R2)

This calculation is done for ‘typ’, ‘min’ as well as ‘max’ values of R1 (=R2) to get the Rpower and Rgnd at the 3 corners.

From the above discussion, it follows that the ‘Terminator’ model can be represented diagrammatically as in Figure 3.3

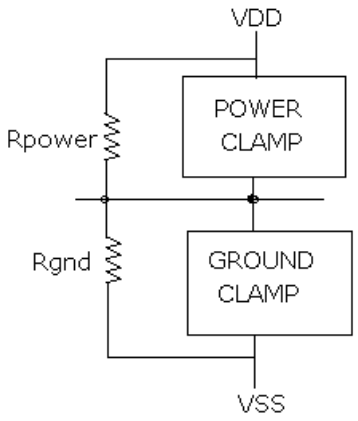

Figure 3.3 Equivalent Terminator model of the termination resistance

3.2 Termination Capacitance

The termination capacitance (C) between the pins of the differential input is captured in the IBIS model as ‘Series’ buffer type. The [C Series] keyword is used to specify its value at the 3 corners.

3.3 Comparison of IBIS model with the actual circuit

The IBIS models were generated and compared with the actual circuit through SPICE simulations. Figure 3.4 shows the simulation environment.

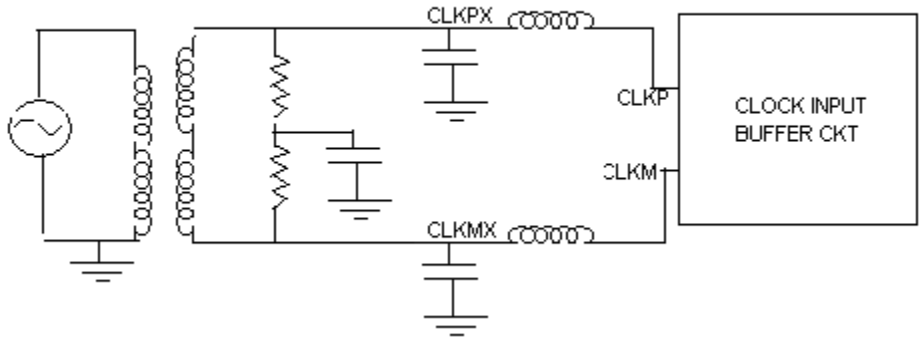

Figure 3.4 Circuit set up used in simulations to validate the IBIS model

Two simulations are performed. The first one uses the full transistor spice netlist of the input buffer circuit. The second simulation uses the IBIS model representation of the buffer as shown in Figure 3.5. A sample spice deck for this configuration is given in section 7.4 of this document.

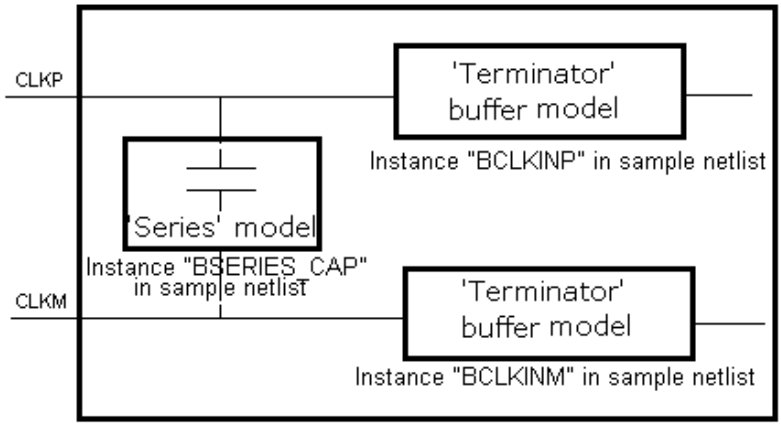

Figure 3.5 The “clock input buffer” block in Fig 3.4 was replaced with this setup of model instances for simulation with IBIS model

Figure 3.6 shows a comparison of the SPICE simulation results obtained from the IBIS model with those from the actual circuit.

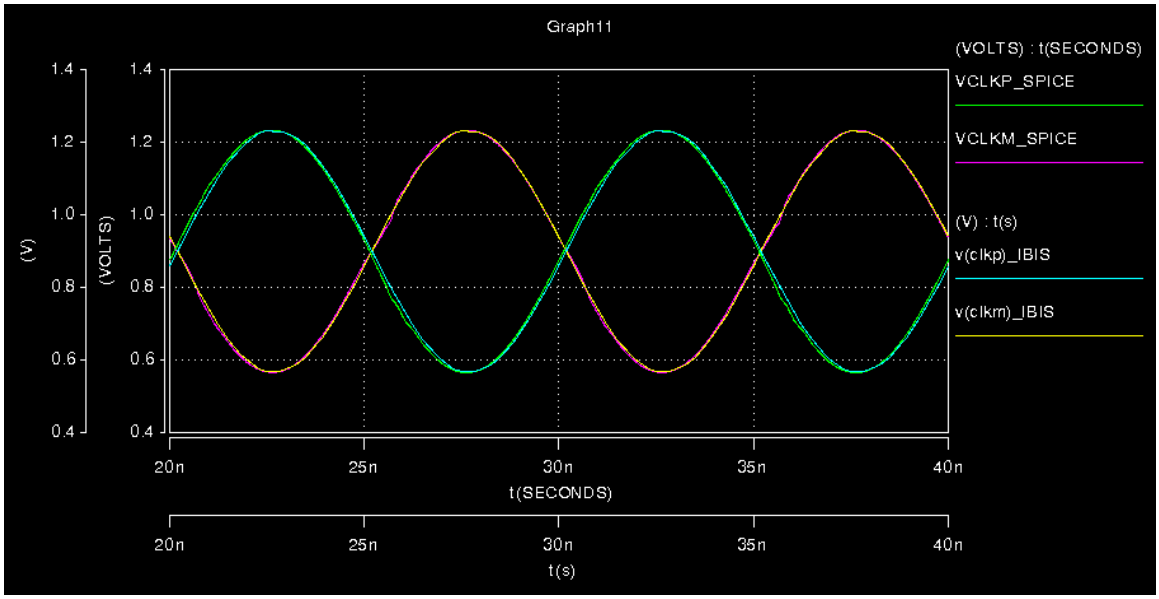

Figure 3.6 Waveforms of simulation with IBIS model Vs full transistor net list

There is a close match between the output waveforms of simulation using actual circuit netlist and its IBIS model.

4. MODEL SUMMARY

Component name - ADS41XX
Model types - Tristate, Terminator, series switch, series cap
Filename - ads41xx.ibs

Modeling conditions:

Condition	typ/ min/ max
DRVDD	1.8 V/ 1.7 V/ 1.9 V
VBG (Common mode reference)	1.065 V/ 1.045 V/ 1.1 V
Junction temperature (Tj)	25/ 125/ -40 (degree C)
Process setting	nominal/ weak/ strong

Package Characteristics:

Characteristics	typ/ min/ max
R_pkg:	0.16Ω/0.144Ω/0.176Ω
L_pkg	4nH/3.6 nH /4.4 nH
C_pkg	2.0pF / 1.8 pF /2.2 pF

5. Quality Verification:

The created IBIS models are verified as follows:

1. Visual check of each characteristics using the s2iplt tool
2. Syntax check by IBISCHK4
3. Behavior of IBIS models and actual circuit compared using SPICE

6. Simulation using IBIS models for the buffer

6.1 Sample instantiation of the IBIS models for the lvds buffer in HSPICE:

```
BOUTPUTP PU 0 LOUTP INP EN_LVDS
+FILE = 'ads41xx.ibs' MODEL = 'LVDS'
+TYP = TYP POWER=ON
+BUFFER = 3-state
+RAMP_RWF = 1
+RAMP_FWF = 1
+INTERPOL = 1

BOUTPUTM PU 0 LOUTM INM EN_LVDS
+FILE = 'ads41xx.ibs' MODEL = 'LVDS'
+TYP = TYP POWER=ON
+BUFFER = 3-state
+RAMP_RWF = 1
+RAMP_FWF = 1
+INTERPOL = 1
```

6.2 CMOS DATA OUTPUT BUFFER

```
BOUTPUTP PU PD OUTP INP EN_CMOS
+FILE = 'ads41xx.ibs' MODEL = 'cmos_data_low'
+TYP = TYP POWER=ON
+BUFFER = 3-state
+RAMP_RWF = 2
+RAMP_FWF = 2
+INTERPOL = 1

*ENABLE SIGNAL FOR THE BUFFER
VEN_CMOS EN_CMOS 0 1.8
```

6.3 CMOS CLOCK OUTPUT BUFFER

```
BOUTPUTP PU PD OUTP INP EN_CMOS
+FILE = 'ads41xx.ibs' MODEL = 'cmos_clk_low'
+TYP = TYP POWER=ON
+BUFFER = 3-state
+RAMP_RWF = 2
+RAMP_FWF = 2
+INTERPOL = 1

*ENABLE SIGNAL FOR THE BUFFER
VEN_CMOS EN_CMOS 0 1.8
```

6.4 INPUT BUFFER FOR CLOCK ALONG WITH TERMINATION CAPACITANCE

BCLKINP AVDD AVSS CLKP
+FILE ='ads41xx.ibs' MODEL = 'input'
+TYP = TYP POWER=ON
+BUFFER = Terminator
+INTERPOL = 1

BCLKINM AVDD AVSS CLKM
+FILE ='ads41xx.ibs' MODEL = 'input'
+TYP = TYP POWER=ON
+BUFFER = Terminator
+INTERPOL = 1

*The following line may also be replaced with a capacitance
*of value as specified against the [C Series] keyword in IBIS model
BSERIES_CAP CLKP CLKM
+FILE ='ads41xx.ibs' MODEL = 'series_cap'
+TYP = TYP
+BUFFER = SERIES
+INTERPOL = 1

7.1 Sample SPICE deck for simulation of buffer

```
.TEMP 27

* INPUT TO THE BUFFER
VINP INP 0 PULSE (0 1.8 0N 0.2N 0.2N 2.7N 5.8N)
VINM INM 0 PULSE (1.8 0 0N 0.2N 0.2N 2.7N 5.8N)

BOUTPUTP PU 0 LOUTP INP EN_LVDS
+FILE = 'ads41xx.ibs' MODEL = 'LVDS'
+TYP = TYP POWER=ON
+BUFFER = 3-state
+RAMP_RWF = 1
+RAMP_FWF = 1
+INTERPOL = 1

BOUTPUTM PU 0 LOUTM INM EN_LVDS
+FILE = 'ads41xx.ibs' MODEL = 'LVDS'
+TYP = TYP POWER=ON
+BUFFER = 3-state
+RAMP_RWF = 1
+RAMP_FWF = 1
+INTERPOL = 1


*ENABLE SIGNAL FOR THE BUFFER
VEN_LVDS EN_LVDS 0 0.0

* PIN INDUCTANCE
LOUTP LOUTP_EXT LOUTP 4N
LOUTM LOUTM_EXT LOUTM 4N
** PIN CAPACITANCE
COUTP LOUTP_EXT 0 2PF
COUTM LOUTM_EXT 0 2PF

** TRANSMISSION LINE LOAD
TDATALINKP LOUTP_EXT 0 LOUTP_RX 0 Z0=50 TD=0.5N
TDATALINKM LOUTM_EXT 0 LOUTM_RX 0 Z0=50 TD=0.5N

** LVDS TERMINATION AT RECEIVER END
RLOAD LOUTP_RX LOUTM_RX 100

** CAPACITANCE AT RECEIVER END
COUTP_RX LOUTP_RX 0 5PF
COUTM_RX LOUTM_RX 0 5PF

.OPTION POST
```

```
.TRAN 10PS 20NS
.PLOT TRAN V(LOUTP) V(LOUTM)
+ V(LOUTP_EXT) V(LOUTM_EXT)
+ V(LOUTP_RX) V(LOUTM_RX)
+ V(LOUTP_RX,LOUTM_RX)

.END
```

7.2 Sample deck with instantiation of the IBIS models for the cmos data buffer in HSPICE:

```
.TEMP 27
* INPUT TO THE BUFFER
VINP INP 0 PULSE (0 1.8 0N 0.2N 0.2N 10N 20N)

BOUTPUTP PU PD OUTP INP EN_CMOS
+FILE = 'ads41xx.ibs' MODEL = 'cmos_data_low'
+TYP = TYP POWER=ON
+BUFFER = 3-state
+RAMP_RWF = 2
+RAMP_FWF = 2
+INTERPOL = 1

*ENABLE SIGNAL FOR THE BUFFER
VEN_CMOS EN_CMOS 0 1.8

** PIN INDUCTANCE
LOUTP OUTP_EXT OUTP 4N
** PIN CAPACITANCE
COUTP OUTP_EXT 0 2.4PF
*
** TRANSMISSION LINE LOAD
TDATALINKP OUTP_EXT 0 OUTP_RX 0 Z0=50 TD=0.3N
*
* CAPACITANCE AT RECEIVER END
COUTP_RX OUTP_RX 0 5PF

.OPTION POST
.OPTION DELMAX=1PS
.TRAN 10PS 50NS
.PLOT TRAN V(OUTP_RX)
.END
```

7.3 Sample instantiation of the IBIS models for the cmos clock buffer in HSPICE:

```
.TEMP 27
* INPUT TO THE BUFFER
```

```
VINP INP 0 PULSE (0 1.8 0N 0.2N 0.2N 10N 20N)

BOUTPUTP PU PD OUTP INP EN_CMOS
+FILE = 'ads41xx.ibs' MODEL = 'cmos_clk_low'
+TYP = TYP POWER=ON
+BUFFER = 3-state
+RAMP_RWF = 2
+RAMP_FWF = 2
+INTERPOL = 1

*ENABLE SIGNAL FOR THE BUFFER
VEN_CMOS EN_CMOS 0 1.8

** PIN INDUCTANCE
LOUTP OUTP_EXT OUTP 4N
** PIN CAPACITANCE
COUTP OUTP_EXT 0 2.4PF
*
** TRANSMISSION LINE LOAD
TDATALINKP OUTP_EXT 0 OUTP_RX 0 Z0=50 TD=0.3N
*
* CAPACITANCE AT RECEIVER END
COUTP_RX OUTP_RX 0 5PF

.OPTION POST
.OPTION DELMAX=1PS
.TRAN 10PS 50NS
.PLOT TRAN V(OUTP_RX)
.END
```

7.4 INPUT BUFFER FOR CLOCK ALONG WITH TERMINATION CAPACITANCE

```
.TEMP 27
VAVDD AVDD 0 1.8
VAVSS AVSS 0 0

BCLKINP AVDD AVSS CLKP
+FILE ='ads41xx.ibs' MODEL = 'input'
+TYP = TYP POWER=ON
+BUFFER = Terminator
+INTERPOL = 1

BCLKINM AVDD AVSS CLKM
+FILE ='ads41xx.ibs' MODEL = 'input'
+TYP = TYP POWER=ON
+BUFFER = Terminator
```

```
+INTERPOL = 1

*The following line may also be replaced with a capacitance
*of value as specified against the [C Series] keyword in IBIS model
BSERIES_CAP CLKP CLKM
+FILE ='ads41xx.ibs' MODEL = 'series_cap'
+TYP = TYP
+BUFFER = SERIES
+INTERPOL = 1

.subckt BALUN1  in  out1  out2 ct
Lin    in    gnd   L=1
Lo1    out1  ct   L=0.25
Lo2    ct   out2  L=0.25
K12    Lin  Lo1    IDEAL
K13    Lin  Lo2    IDEAL
K23    Lo1  Lo2    IDEAL
.ends
VIN SRCA AVSS SIN (0 1 100MEG)
RSRC SRCA SRC R=50
XTRFM SRC CLKP_IN CLKM_IN n1 BALUN1
RTERM_SRC_M NET024 CLKM_IN R=50
RTERM_SRC_P CLKP_IN NET024 R=50
CACGND NET024 AVSS C=1e-6

LPINP CLKP_IN CLKP L=4e-9
LPINM CLKM_IN CLKM L=4e-9
CPINM CLKM_IN AVSS C=2e-12
CPINP CLKP_IN AVSS C=2e-12

.TRAN 0.01n 40n
.OPTIONS POST
.plot tran V(CLKP CLKM)
.END
```