Modeling the ADS61XX_HS family through IBIS

Applies to devices: ADS6149, ADS6148, ADS6129, ADS6128

Version 1.3
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3-state CMOS buffer

The structure of the CMOS buffer in ADS61XX_HS family of products is shown in Figure 1.1. The structure can be directly mapped to the structure of a 3-state output buffer as specified by the IBIS standard. So its model shall consist of

1. I-V characteristics of Power and Ground clamp as well as the pull-up and pull-down circuits.
2. V-t characteristics of output pin

Voltage levels of 0 Volts and 1.8 Volts correspond to logic levels of '0' and '1' at HI and LO at the input of the buffer.

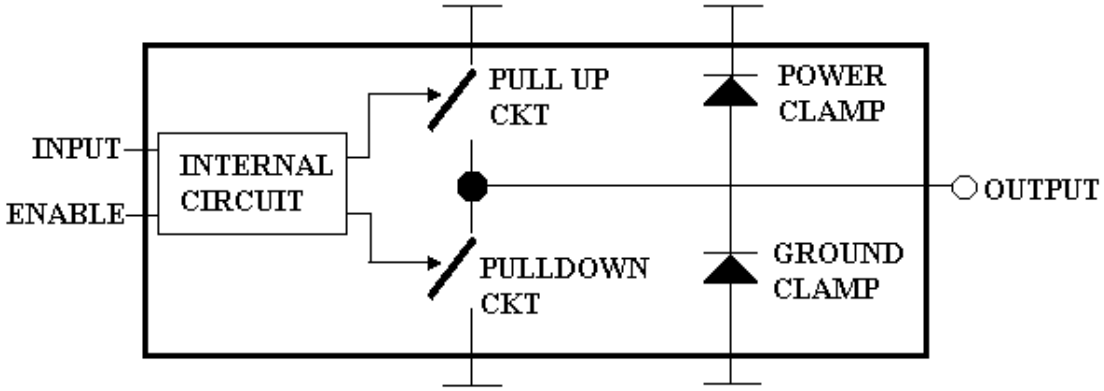


Figure 1.1 3-state CMOS output buffer structure

1.1 V-I tables for Pull-up and Power clamp

The Circuit setup used to extract the pull-up and power clamp data is shown in Fig. 1.2 Two sets of measurements are taken.

1 Measurement (a)
- Input is at HI
- Enable pin is at LO to deactivate output
- The voltage source VPIN is swept from -VDD to 2*VDD (as VSS = 0), where VDD = 1.8V, 1.7V or 1.9V (for typ, min and max corners). done by first giving a LO at the output enable pin
- The current flowing through VPIN is tabulated

2 Measurement (b)
- Input is at HI
- Enable pin is at HI to activate output
- The voltage source VPIN is swept from -VDD to 2*VDD (as VSS = 0), where VDD = 1.8V, 1.7V or 1.9V (for typ, min and max corners).
- The current flowing through VPIN is tabulated

The current measurements in (a) (for VPIN = VDD to 2VDD) are the Power clamp data, as only clamp circuits are active. The current measurement in (b) is sum of clamp circuit current and pull-up circuit current. So (b) - (a) gives the pull-up data.

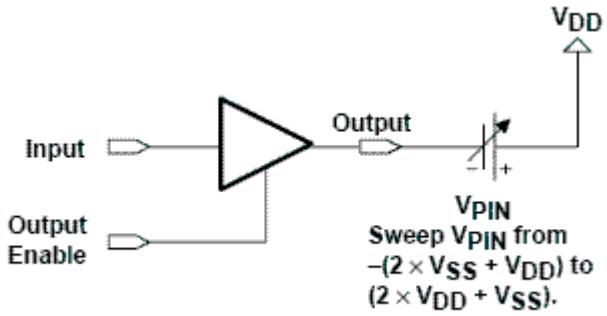


Figure 1.2 Circuit setup to extract Pull-up and Power clamp data

1.2 V-I tables for Pull-down and Ground clamp

The Circuit setup used to extract the pull-down and ground clamp data is shown in Fig. 1.3. Two sets of measurements are taken.

1. Measurement (a)
    - Input is at LO
    - Enable pin is at LO to deactivate output
    - The voltage source VPIN is swept from -VDD to 2*VDD (as VSS = 0), where VDD = 3.3V, 3.0V or 3.6V (for typ, min and max corners). done by first giving a LO at the output enable pin
    - The current flowing through VPIN is tabulated
2. Measurement (b)
    - Input is at LO
    - Enable pin is at HI to activate output
    - The voltage source VPIN is swept from -VDD to 2*VDD (as VSS = 0), where VDD = 3.3V, 3.0V or 3.6V (for typ, min and max corners).
    - The current flowing through VPIN is tabulated

The current measurements in (a) (for VPIN = -VDD to VDD) are tabulated as the Ground clamp data, as only clamp circuits are active. The current measurement in (b) is sum of clamp circuit current and pull-down circuit current. So (b) - (a) gives the pull-down data.

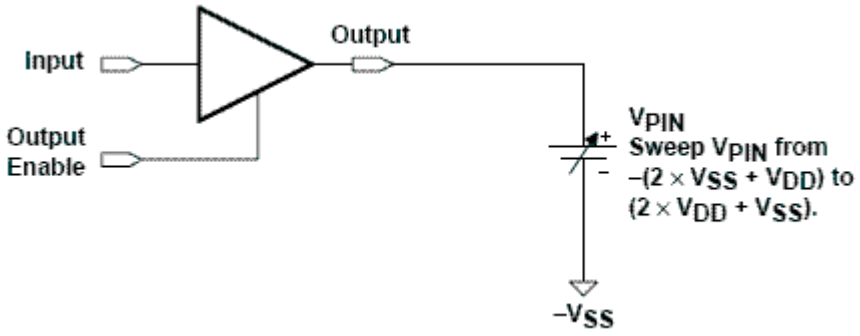


Figure 1.3 Circuit setup to extract Pull-down and Ground clamp data

1.3 Generating the V-t Data

Four V-t tables are generated using the setup shown in Figure 1.4. A step signal is given at input at voltage waveform at output is tabulated

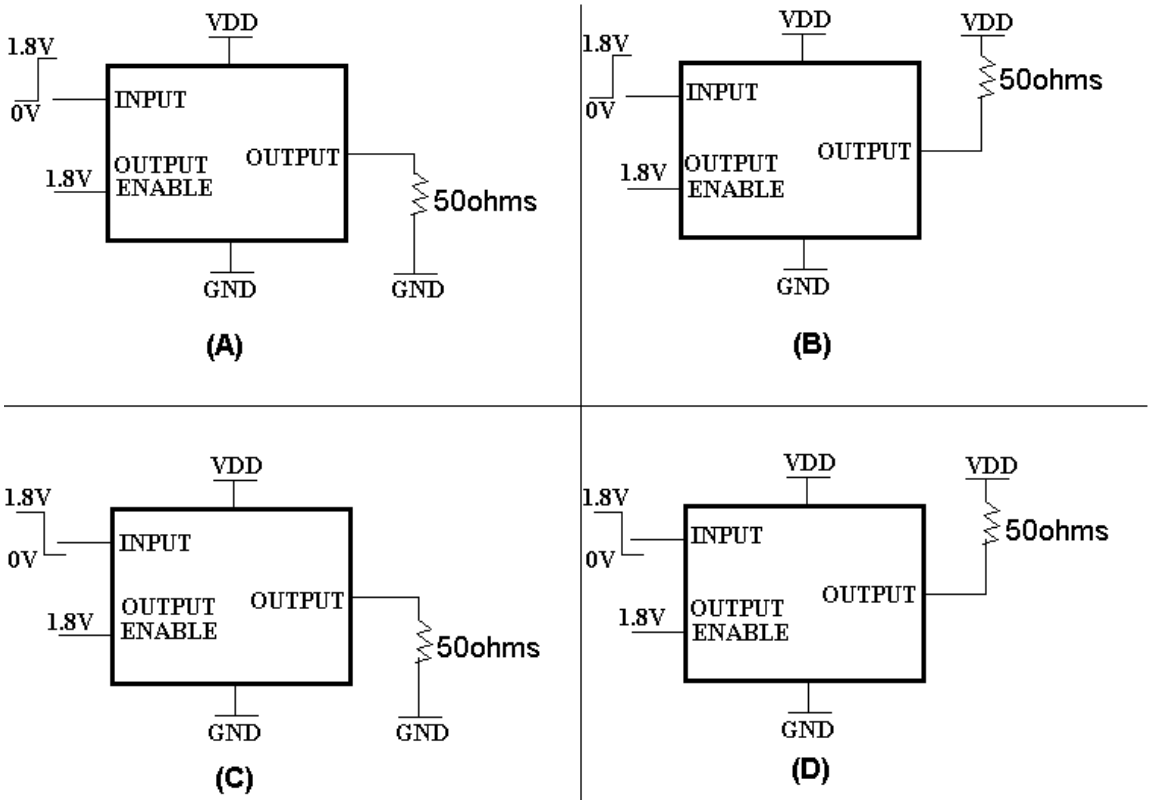


Figure 1.4 Circuit setup to extract the four V-t tables

1.4 Comparison of IBIS model with the actual circuit

To check how well the IBIS models shall model the actual circuit, the following SPICE simulations were done. The circuit set up is shown in Figure 1.5. In the first simulation the SPICE netlist of the buffer is used and in the second simulation the IBIS model of the buffer is used. (Refer section on sample spice decks)

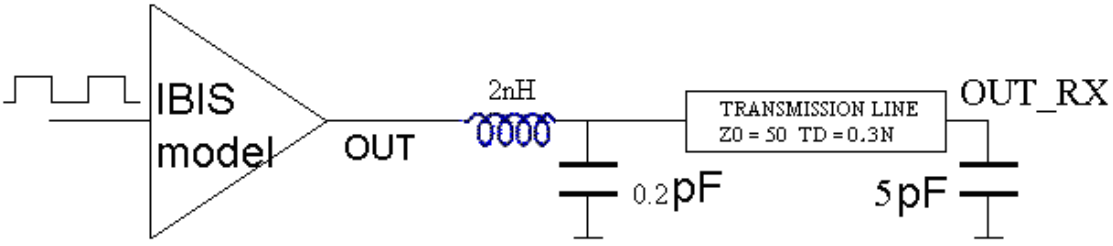


Figure 1.5 Circuit set up used in simulations for validation of the model

Simulations were also done with different values of the delay for the transmission line and load capacitance.

Figure 1.6 shows a comparison of the HSPICE simulation results obtained from the IBIS model with those from the actual circuit at the typ corner.

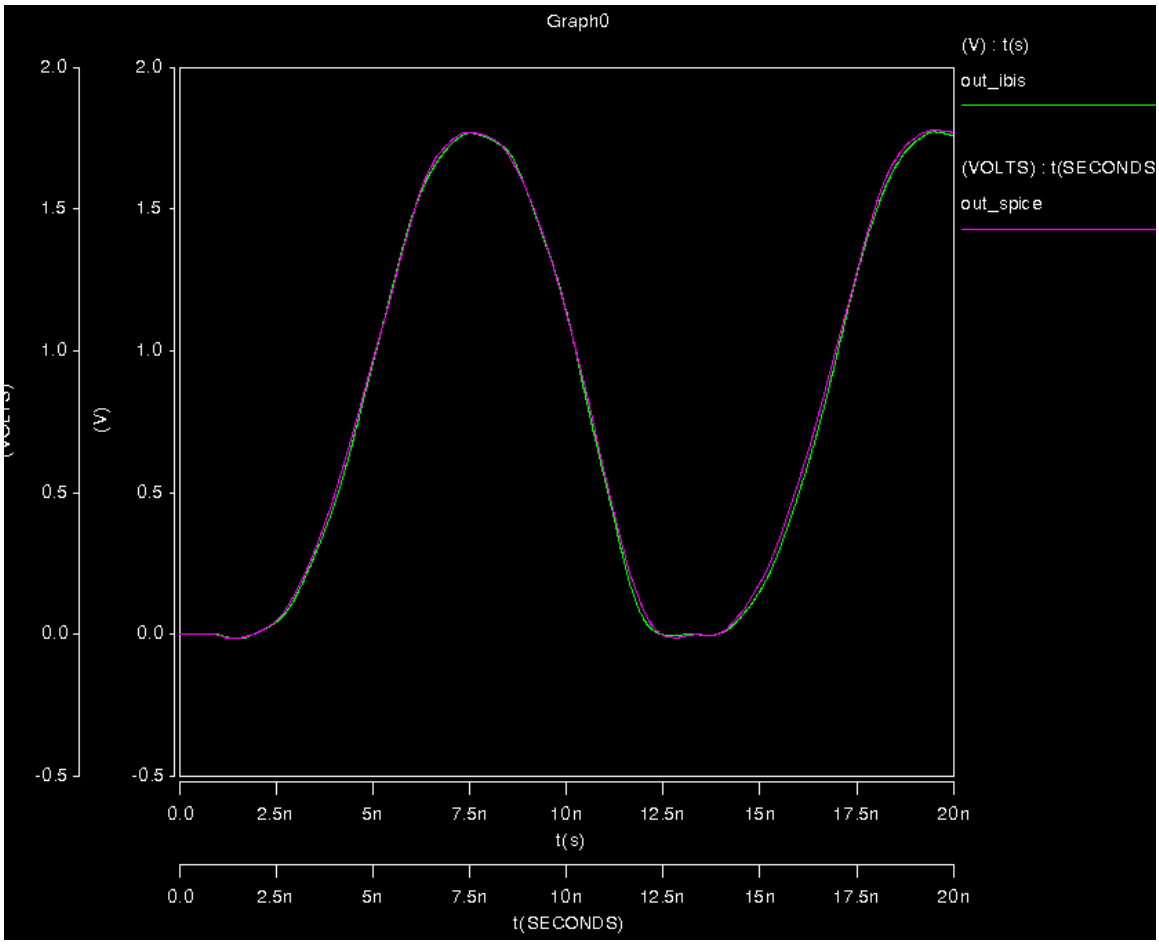


Figure 1.6.a Output waveforms of simulation with IBIS model Vs. full-transistor netlist for data output buffer

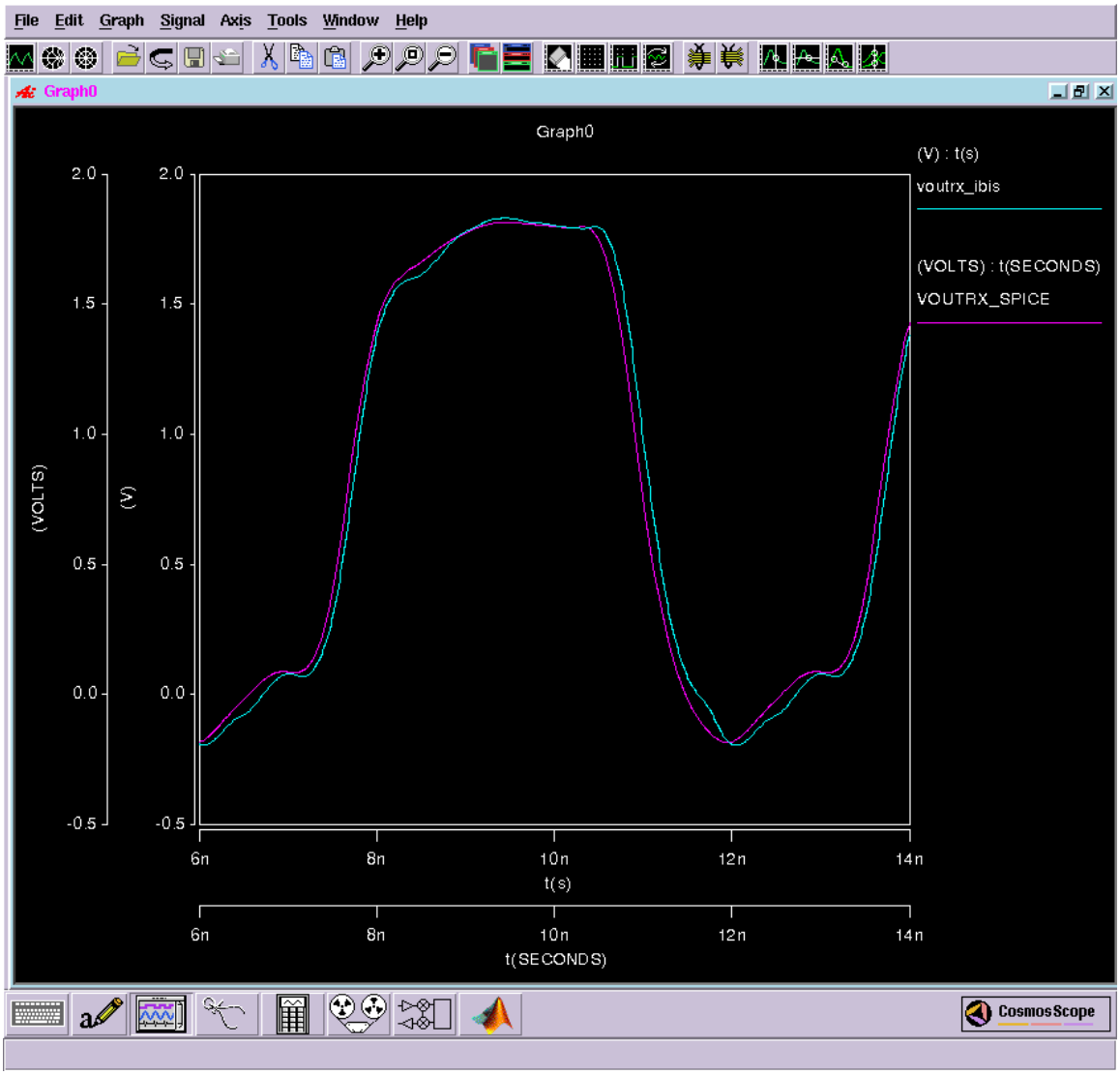


Figure 1.6.b Output waveforms of simulation with IBIS model Vs. full-transistor netlist for clock output buffer

The only difference in test bench circuit for clock and data buffer was the input frequency. The highest operation frequency for clock is double of that of data buffer. As can be observed, there is a close match between the actual circuit and its IBIS model.

2. LVDS BUFFER

Method of modeling the LVDS buffer through IBIS

IBIS is basically defined for single ended buffers. Since the LVDS buffer has differential inputs and differential outputs, some additional considerations are involved while modeling it through IBIS.

ADS61XX_HS LVDS buffer architecture

The internal structure of the LVDS buffer in ADS61XX_HS family of products is shown in Figure 1. For simplicity, the enable pin has not been shown. HI and LO refer to the differential input to the buffer. VH and VL are internally regulated voltages of values 1.5V and 0.84V respectively. LOUTP and LOUTM form the differential output.
The buffer consists of 4 MOS switches that connect or disconnect the appropriate regulated voltages VH and VL to the output through the equivalent on-resistance of the switch.

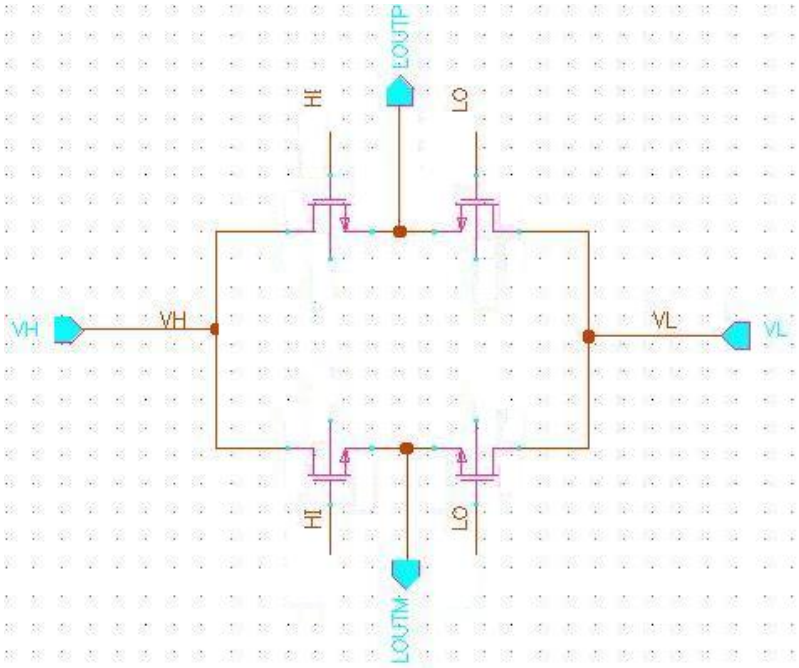


Figure 1. LVDS buffer architecture

Comparison of IBIS model with the actual circuit

The IBIS models were generated and compared with the actual circuit through SPICE simulations. Figure 6 shows the simulation environment for the actual LVDS buffer, while Figure 7 shows the identical environment used for the IBIS model.

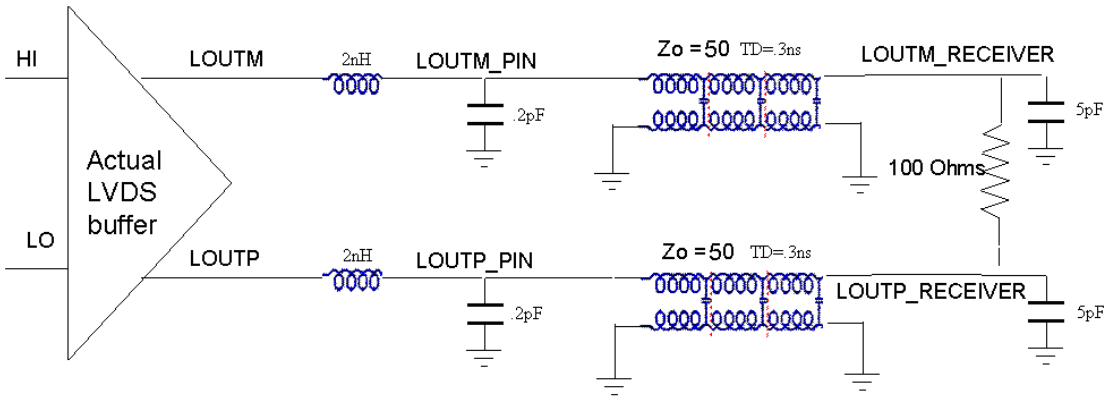


Figure 6. Simulation environment for the actual LVDS buffer

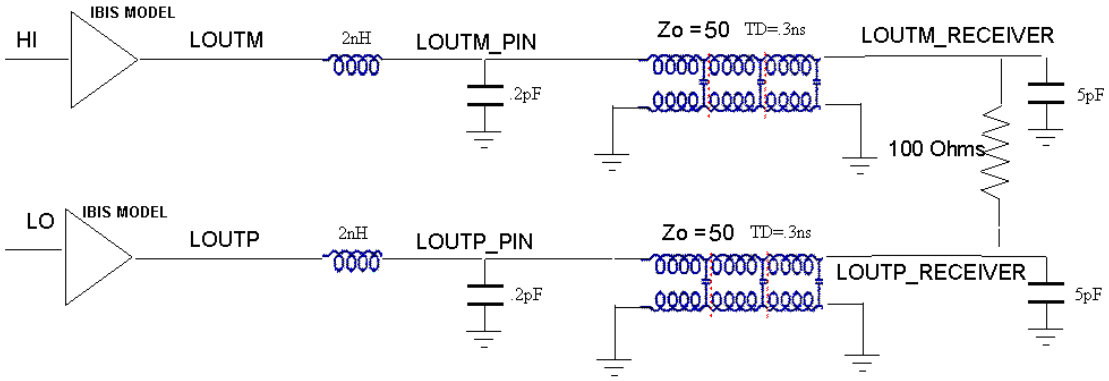


Figure 7. Simulation environment for the IBIS model of the LVDS buffer

Simulations were done with different values of the delay for the transmission line.

Figure 8 shows a comparison of the SPICE simulation results obtained from the IBIS model with those from the actual circuit. The signals DIFF_IBIS and DIFF_SPICE are the differential signal appearing across the resistor at receiver end and DATAOPRX_IBIS/SPICE are signals at receiver end of one of the pins LOUTP.

As can be observed, there is a close match between the actual circuit and its IBIS model.

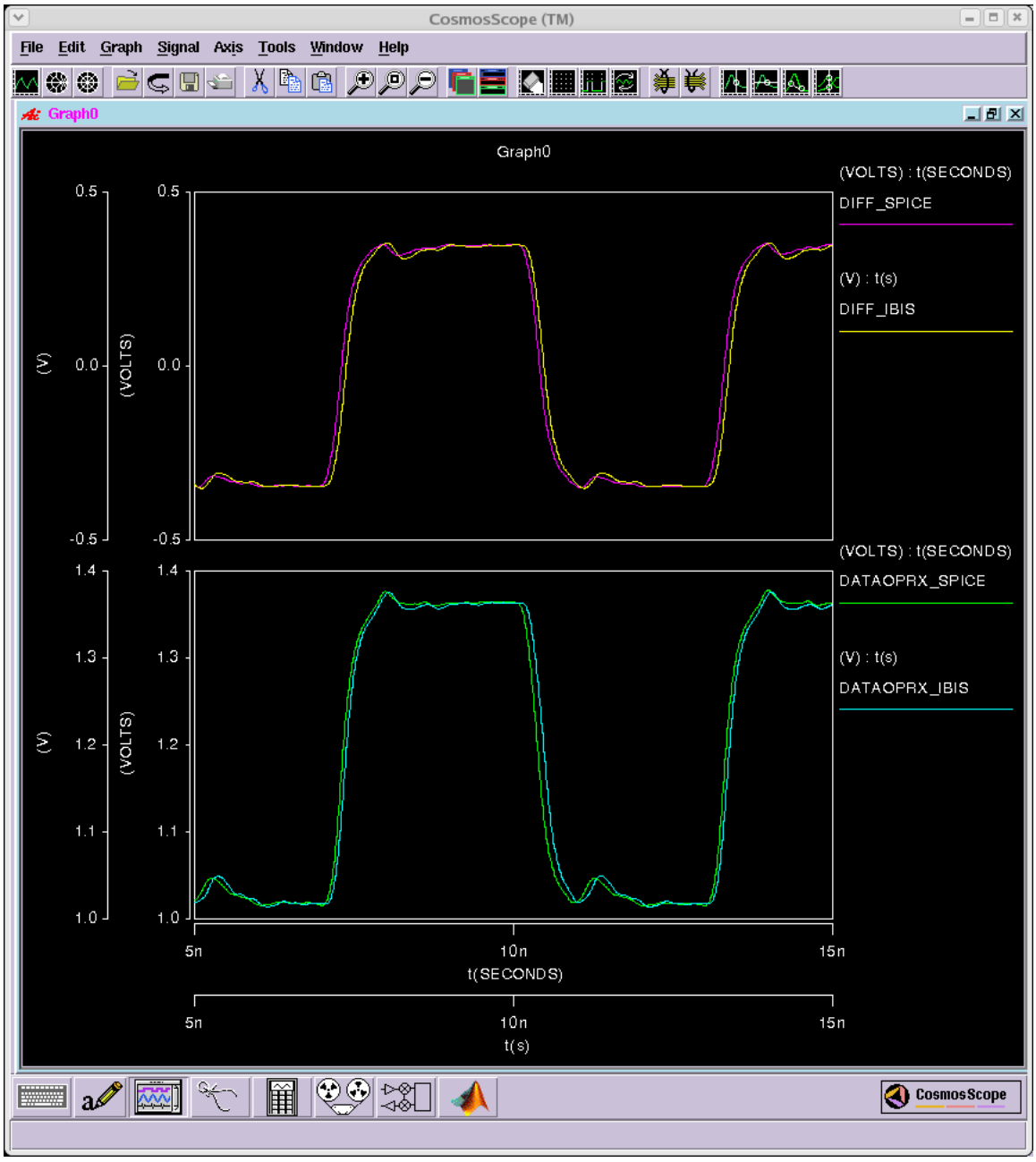


Figure 8 : Comparison of results between full-transistor spice simulation vs. simulation using IBIS model for buffer.

3. INPUT BUFFER

The CMOS input buffers can be approximated to the equivalent circuit of termination elements (R or RC), clamp circuits and other receiver circuitry which can be represented by an equivalent cap when looking into the pin as illustrated in Figure 9(a) – (d).

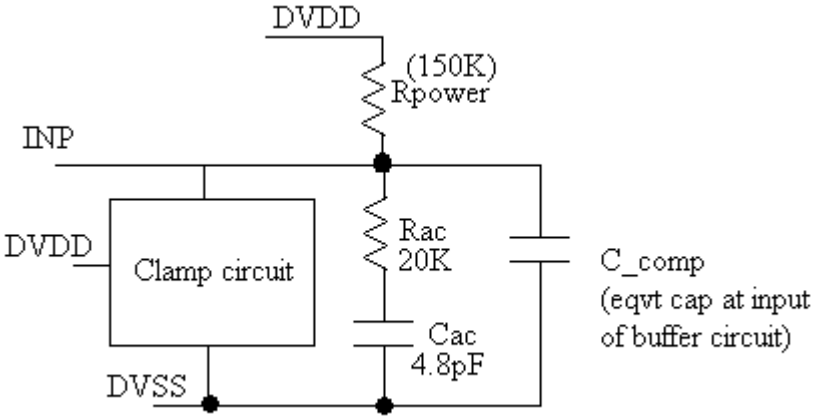


Figure 9(a) Input Buffer equivalent for OE

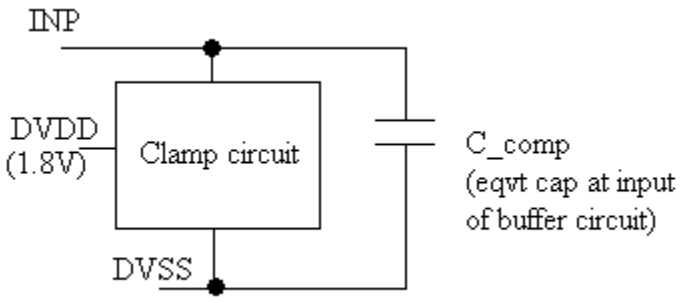


Figure 9(b) Input Buffer equivalent for RESET

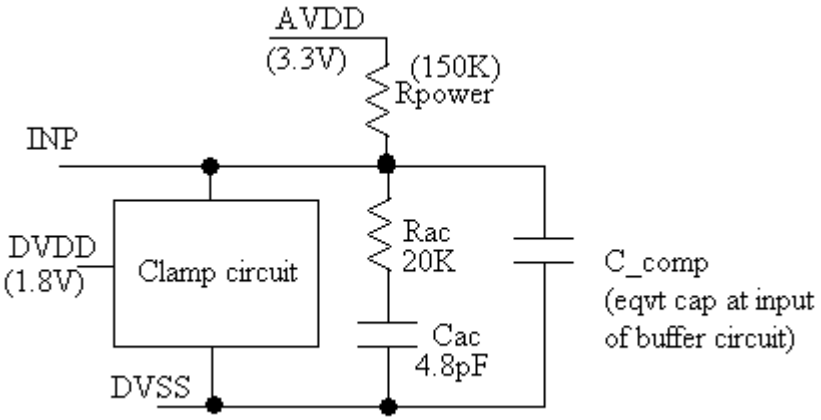


Figure 9(c) Input Buffer equivalent for SEN

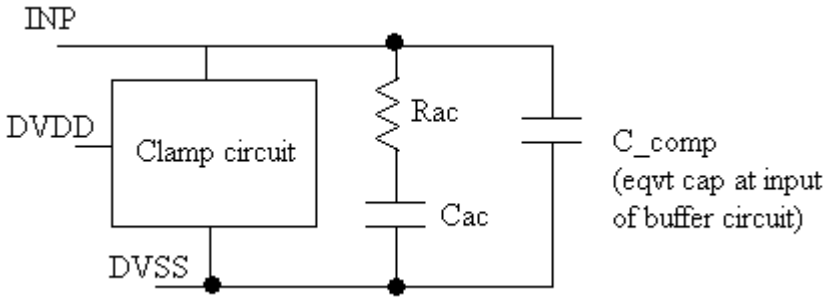


Figure 9(c) Input Buffer equivalent for SCLK (and SDATA)

As there are termination elements, the buffer is modeled as a [Terminator] model type. The C_comp is measured by applying a voltage ramp at input of buffer (without the termination elements) and measuring the current.

Model correlation

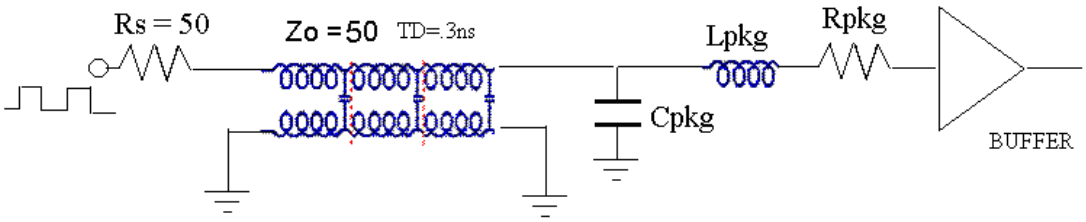
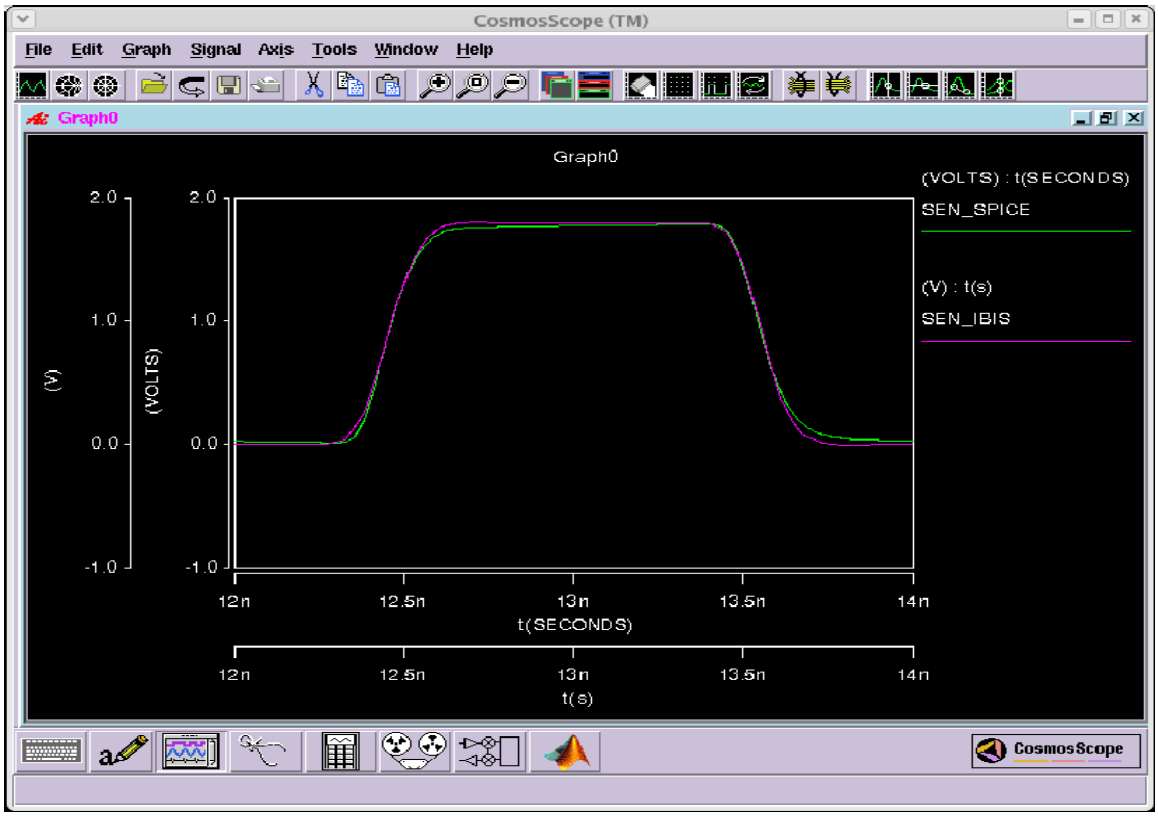
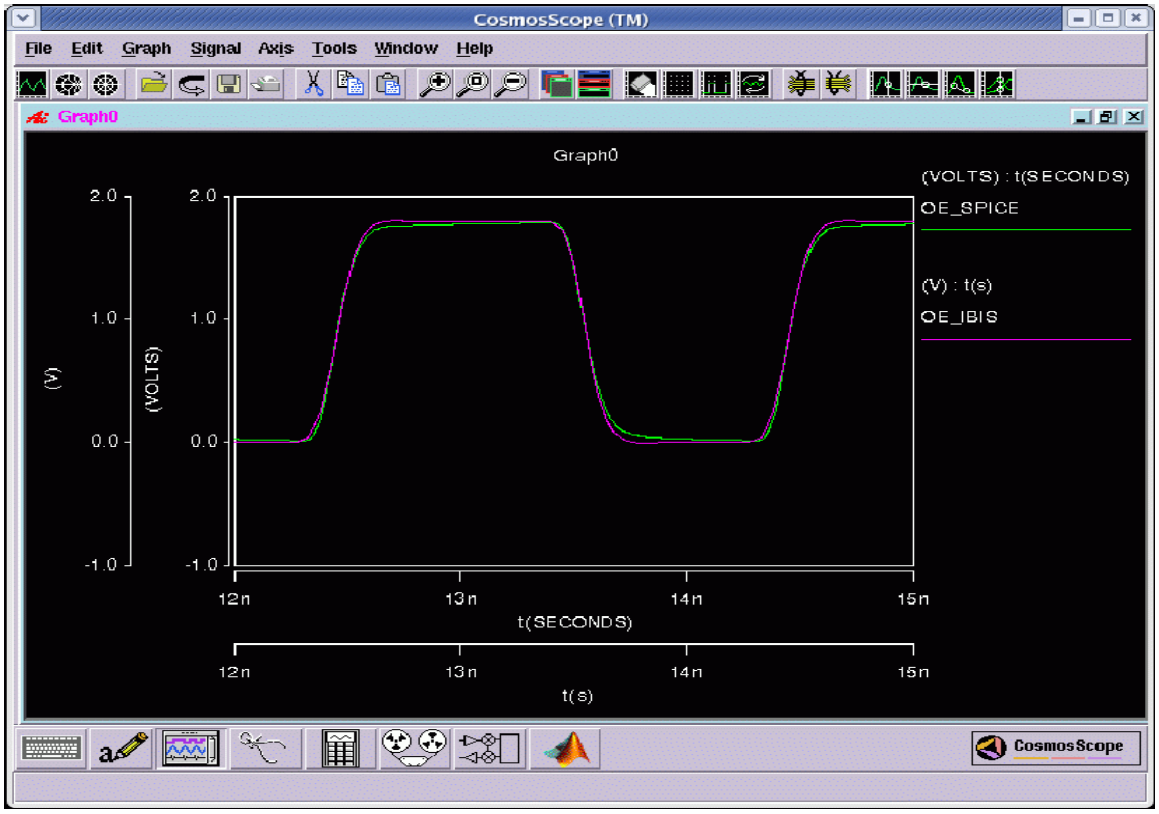
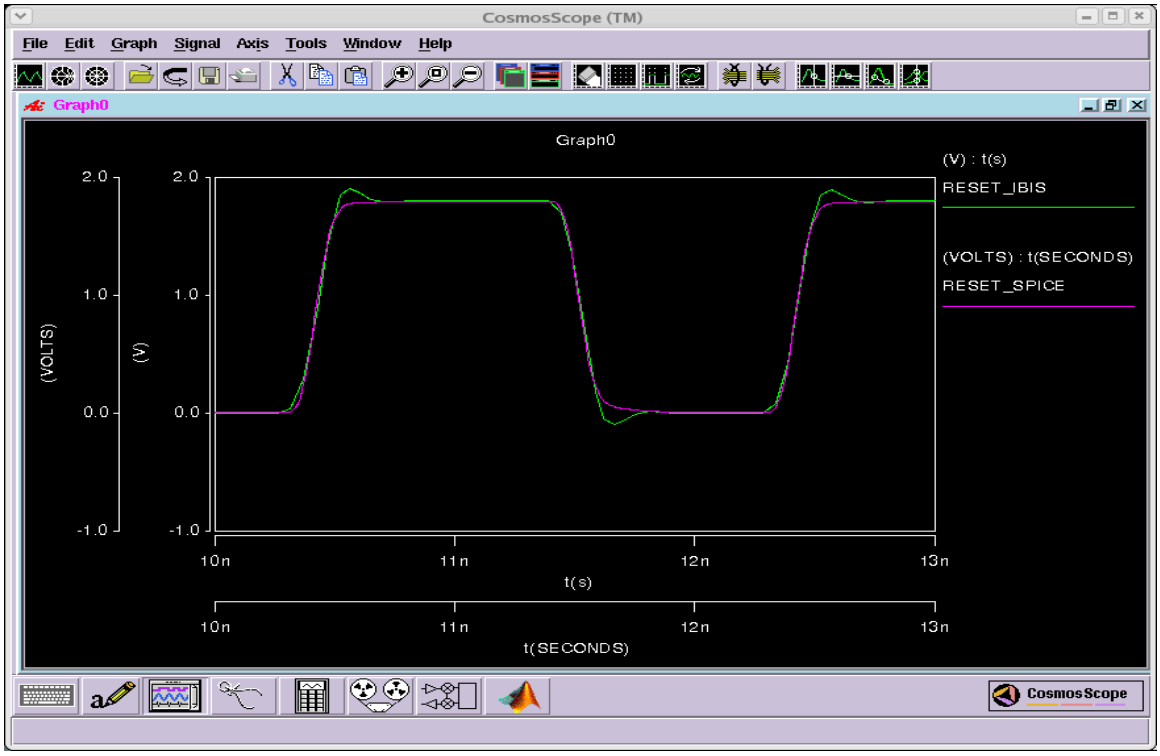


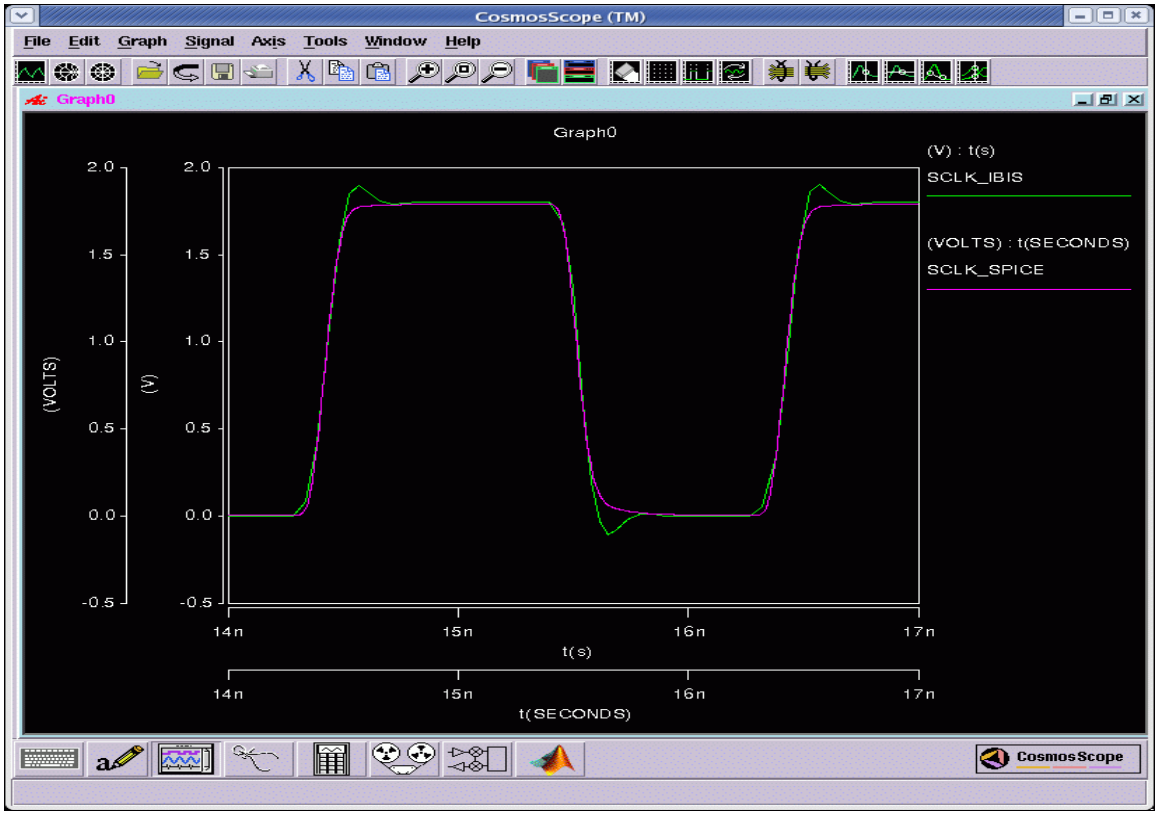
Figure 10 Circuit setup used to validate the input buffer.

The waveforms at the input of the buffer were compared amongst IBIS and spice model simulation results. The results for SEN, OE,RESET and SCLK are captured below.


CosmosScope (TM)
File Edit Graph Signal Axis Tools Window Help
Graph0
Graph0
(VOLTS) : t(SECONDS)
SEN_SPICE
(V) : t(s)
SEN_IBIS
2.0
1.0
0.0
-1.0
(V)
(VOLTS)
12n
12.5n
13n
13.5n
14n
t(SECONDS)
t(s)
CosmosScope


CosmosScope (TM)
File Edit Graph Signal Axis Tools Window Help
Graph0
Graph0
(VOLTS) : t(SECONDS)
OE_SPICE
(V) : t(s)
OE_IBIS
2.0
1.0
0.0
-1.0
(V)
(VOLTS)
12n
13n
14n
15n
t(SECONDS)
t(s)
CosmosScope


CosmosScope (TM)
File Edit Graph Signal Axis Tools Window Help
Graph0
Graph0
(V) : t(s)
RESET_IBIS
(VOLTS) : t(SECONDS)
RESET_SPICE
2.0
1.0
0.0
-1.0
(VOLTS)
(V)
10n
11n
12n
13n
t(s)
t(SECONDS)
CosmosScope



MODEL SUMMARY

Component name - ADS61XX_HS
Model types – CMOS Output (3-state), LVDS output(3-state), input (Terminator)
Filename - ads61xx_hs.ibs

Modeling conditions:

Condition	typ/ min/ max
DRVDD	1.8 V/ 1.65 V/ 1.95 V
VBG (Common mode reference)	1.2 V/ 1.1 V/ 1.25 V
Junction temperature (Tj)	25/ 125/ -40 (degree C)
Process setting	nominal/ weak/ strong

Package Characteristics:

Characteristics	typ/ min/ max
R_pkg	0.13119Ω/0.067130Ω/0.17310Ω
L_pkg	2.1610nH/ 1.7017nH / 2.7362nH
C_pkg	0.23pF / 0.20pF / 0.30pF

Quality Verification:

The created IBIS models are verified as follows:

1. Visual check of each characteristics using the s2iplt tool
2. Syntax check by IBISCHK4
3. Behavior of IBIS models and actual circuit compared using SPICE

Sample HSPICE deck for simulation of buffer LVDS

```
VINS2IP IN_LVDSP_IBSVALIDATE 0 PULSE 0.0 1.8
+ 0 1.0E-10 1.0E-10 3E-9 6e-9
VINS2IM IN_LVDSM_IBSVALIDATE 0 PULSE 1.8 0.0
+ 0 1.0E-10 1.0E-10 3E-9 6e-9
VFIXS2I dum17854 0 DC 1.2
BoutputP PUP_IBSVALIDATE PDP_IBSVALIDATE DATAOP
+ IN_LVDSP_IBSVALIDATE TRI_OUT FILE="ads61xx_hs.ibs"
+ MODEL = "LVDS" TYP=typ POWER=ON BUFFER = THREE_STATE
BoutputM PUM_IBSVALIDATE PDM_IBSVALIDATE DATAOM
+ IN_LVDSM_IBSVALIDATE TRI_OUT FILE="ads61xx_hs.ibs"
+ MODEL = "LVDS" TYP=typ POWER=ON BUFFER = THREE_STATE
VENAS2I TRI_OUT 0 DC 0.0
VRPKGOUTP_IBISVALIDATE DATAOP DUMMY1OUTP_IBISVALIDATE 0
VRPKGOUTM_IBISVALIDATE DATAOM DUMMY1OUTM_IBISVALIDATE 0

LPKGOUTP_IBISVALIDATE DUMMY1OUTP_IBISVALIDATE
+ DUMMY2OUTP_IBISVALIDATE 2n
LPKGOUTM_IBISVALIDATE DUMMY1OUTM_IBISVALIDATE
+ DUMMY2OUTM_IBISVALIDATE 2n

CPKGOUTP_IBISVALIDATE DUMMY2OUTP_IBISVALIDATE 0 .2p
CPKGOUTM_IBISVALIDATE DUMMY2OUTM_IBISVALIDATE 0 .2p

TXNOUTP_IBISVALIDATE DUMMY2OUTP_IBISVALIDATE 0
+ DATAOPRX_IBISVALIDATE 0 Z0=50 TD=.3n
TXNOUTM_IBISVALIDATE DUMMY2OUTM_IBISVALIDATE 0
+ DATAOMRX_IBISVALIDATE 0 Z0=50 TD=.3n

CLOADOUTP_IBISVALIDATE DATAOPRX_IBISVALIDATE 0 5p
CLOADOUTM_IBISVALIDATE DATAOMRX_IBISVALIDATE 0 5p

RLOADOUTP_IBISVALIDATE DATAOPRX_IBISVALIDATE dum17854 50
RLOADOUTM_IBISVALIDATE DATAOMRX_IBISVALIDATE dum17854 50

.TRAN 1.25e-11 20n
.option delmax=1.25e-11
.PLOT TRAN V( DATAOPRX_IBISVALIDATE)
+ V( DATAOMRX_IBISVALIDATE) V( DATAOP ) V( DATAOM )
.PLOT TRAN V( DATAOP, DATAOM )
+ V( DATAOPRX_IBISVALIDATE,DATAOMRX_IBISVALIDATE)

.option post
.END
```

CMOS clock buffer

```
BoutputP PUP_IBSVALIDATE PDP_IBSVALIDATE OUTCLK
+ IN_CLKP_IBSVALIDATE TRI_OUT FILE="ads61xx_hs.ibs"
+ MODEL = "cmos_clk" TYP=typ POWER=ON BUFFER = THREE_STATE

VINS2IP IN_CLKP_IBSVALIDATE 0 PULSE 0.0 1.8 0 1.000E-10
+ 1.000E-10 3.0E-9 6.0E-9
VENAS2I TRI_OUT 0 DC 1.8
VRPKGOUTP_IBISVALIDATE OUTCLK DUMMY1OUTP_IBISVALIDATE 0
LPKGOUTP_IBISVALIDATE DUMMY1OUTP_IBISVALIDATE
+ DUMMY2OUTP_IBISVALIDATE 2n
CPKGOUTP_IBISVALIDATE DUMMY2OUTP_IBISVALIDATE 0 .2p
TXNOUTP_IBISVALIDATE DUMMY2OUTP_IBISVALIDATE 0
+ OUTCLKRX_IBISVALIDATE 0 Z0=50 TD=.3n
CLOADOUTP_IBISVALIDATE OUTCLKRX_IBISVALIDATE 0 5p

.TRAN 1.25e-11 20n
.option delmax=1.25e-11
.PLOT TRAN V( OUTCLKRX_IBISVALIDATE ) V( OUTCLK )
.option post
.END
```

CMOS data buffer

```
BoutputP PUP_IBSVALIDATE PDP_IBSVALIDATE DOUT IN_IBSVALIDATE
+ TRI_OUT FILE="ads61xx_hs.ibs" MODEL = "cmos_data" TYP=typ
+ POWER=ON BUFFER = THREE_STATE

VINS2IP IN_IBSVALIDATE 0 PULSE 0.0 1.8 0 1.000E-10
+ 1.000E-10 6.0E-9 12.0E-9
VENAS2I TRI_OUT 0 DC 1.8
VRPKGOUTP_IBISVALIDATE DOUT DUMMY1OUTP_IBISVALIDATE 0
LPKGOUTP_IBISVALIDATE DUMMY1OUTP_IBISVALIDATE
+ DUMMY2OUTP_IBISVALIDATE 2n
CPKGOUTP_IBISVALIDATE DUMMY2OUTP_IBISVALIDATE 0 .2p
TXNOUTP_IBISVALIDATE DUMMY2OUTP_IBISVALIDATE 0
+ DOUTRX_IBISVALIDATE 0 Z0=50 TD=.3n
CLOADOUTP_IBISVALIDATE DOUTRX_IBISVALIDATE 0 5p

.TRAN 1.25e-11 20n
.option delmax=1.25e-11
.PLOT TRAN V( DOUTRX_IBISVALIDATE ) V( DOUT )
.option post
.END
```

Input Buffer (SEN)

```
BSEN AVDD AVSS SEN FILE ='ads61xx_hs.ibs' MODEL = 'inp_sen'
+TYP = TYP POWER=ON  BUFFER = TERMINATOR

RPKG SEN N1 0.13697
LPKG N1 N2 2.13329nH
Cpkg N2 0 0.20917pF
TXN N3 0 N2 0 Z0=50 TD=.3n
RIN INP N3 50
VINP INP 0 DC 0.0
+ PULSE( 0.0 1.8 0 1.000E-10 1.000E-10 1E-9 2E-9 )

.TR 10ps 30n
.PLOT TR V(INP OE)
.option post
.END
```

Input Buffer (OE)

```
BOE AVDD AVSS OE FILE ='ads61xx_hs.ibs' MODEL = 'inp_oe'
+TYP = TYP POWER=ON BUFFER = TERMINATOR

RPKG OE N1 0.13697
LPKG N1 N2 2.13329nH
Cpkg N2 0 0.20917pF
TXN N3 0 N2 0 Z0=50 TD=.3n
RIN INP N3 50
VINP INP 0 DC 0.0
+ PULSE( 0.0 1.8 0 1.000E-10 1.000E-10 1E-9 2E-9 )

.TR 10ps 30n
.PLOT TR V(INP OE)
.option post
.END
```

Input Buffer (RESET)

```
BRESET AVDD AVSS RESET FILE ='ads61xx_hs.ibs'
+ MODEL = 'inp_reset' TYP = TYP POWER=ON BUFFER = TERMINATOR

RPKG RESET N1 0.13320
LPKG N1 N2 2.05999n
Cpkg N2 0 0.20700p
TXN N2 0 INP1 0 Z0=50 TD=.3n
Rin INP INP1 50
VOUTS2I INP 0 DC 0.0
+ PULSE( 0.0 1.8 0 1.000E-10 1.000E-10 1E-9 2E-9 )

.TR 10ps 30n
.PLOT TR V(INP RESET)
.option post
.END
```

Input Buffer (SCLK and SDATA)

```
BSCLK AVDD AVSS SCLK FILE ='ads61xx_hs.ibs' MODEL = 'inp_sclk'
+ TYP = TYP POWER=ON BUFFER = TERMINATOR

RPKG SCLK_B N1 0.13320
LPKG N1 N2 2.05999n
Cpkg N2 0 0.20700p
TXN N2 0 INP1 0 Z0=50 TD=.3n
Rin INP INP1 50
VOUTS2I INP 0 DC 0.0 PULSE( 0.0 1.8 0 1.000E-10 1.000E-10 1E-9 2E-9 )

.TR 10ps 30n
.PLOT TR V(INP SCLK)
.option post
.END
```