REVISIONS			
REV	DESCRIPTION	APPRVD	DATE
A	INITIAL RELEASE		02-25-11

NOTES: UNLESS OTHERWISE SPECIFIED

1. MATERIAL: PER IPC-4101/24.

A. LAMINATE: TYPE GFN, GRADE A, CLASS 2, AND TYPE FR-4

B. FINISHED BOARD: PER SHEET 3

C. ALL COPPER LAYERS MUST BE SPACED PER DETAIL "A".

D. BOARD THICKNESS IS MEASURED INCLUDING TOP AND BOTTOM SIDES FINISHED COPPER. TIN, TIN/LEAD, OR GOLD PLATING. SOLDERMASK, AND SILKSCREEN LEGEND MUST NOT BE INCLUDED IN FINSHED BOARD THICKNESS.

E. ALL INNER LAYERS MUST BE OXIDE COATED.

2. THE CONDUCTOR PATTERN MUST BE ETCHED USING XXX.ART FILES 880600582-001 REV A SUPPLIED.
3. ALL CONDUCTOR LAYERS MUST BE REGISTERED WITHIN +/-.005 INCH FROM TRUE POSITION.
4. ALL EXTERNAL LAYERS CONDUCTOR WIDTH MUST BE WITHIN +/-.0015 INCH OR 15% OF ARTWORK OR WHICHEVER IS SMALLER.
   ALL INTERNAL LAYERS CONDUCTOR WIDTH MUST BE WITHIN +/-.0010 INCH OR 15% OF ARTWORK OR WHICHEVER IS SMALLER.
5. BOARD MUST BE NC DRILLED USING DRILL DATA: NCDRILL.DAT AND NCDRILL.BIT SUPPLIED.
6. DRILL TOLERANCES AND HOLES SIZE ARE FOR FINISHED BOARD.
7. ALL HOLES MUST BE REGISTERED WITHIN +/-.003 INCH FROM TRUE POSITION.
8. MINIMUM ANNULAR RING MUST BE .002 INCH.
9. PLATING:
   A. PER MIL-C-14550, PLATED THROUGH HOLES MUST BE PLATED WITH .0008 MIN. TO .0015 MAX INCH THICK COPPER.

B. PER MIL-G-45204, IMMERSION GOLD .000002 TO .000007 INCHES OVER .000150 TO .000200 INCHES OF ELECTROLESS NICKEL.
   NO INTERNAL LAYERS ARE TO BE GOLD PLATED.

10. IMPEDANCE PER SHEET 3:
    TRACE WIDTH AND LAYER SPACING MAY BE CHANGED TO ACCOMMODATE FABRICATION PROCESS BUT PRIOR APPROVAL IS REQUIRED BEFORE TRACE WIDTH OR LAYER SPACING CHANGES ARE MADE.
11. NO SPACING GAUGE AT BOARD EDGE.
12. WARP AND TWIST OF FINISHED BOARDS MUST NOT EXCEED .007 INCH PER INCH.
13. SOLDERMASK: PER IPC-SM-840
    A. SOLDERMASK BOTH TOP AND BOTTOM SIDES.
    B. SOLDERMASK MUST CLEAR ALL LANDS SHOWN ON GERBER SOLDERMASK LAYERS.
    C. COLOR GREEN AND SOLVENT FREE.
    D. LIQUID PHOTO-IMAGEABLE MUST BE .0002 MIN. TO .0008 MAX. INCH THICK.
14. SILKSCREEN TOP AND BOTTOM SIDES USING A GLOSSY WHITE, NONCONDUCTIVE, EPOXY BASED INK. NO SILKSCREEN ALLOWED ON GOLD PLATED AREAS OR IN HOLES.
15. ROUTE BOARD OUTLINE, PER DRAWING DIMENSIONS.
16. VENDOR MUST ENTER VENDOR'S IDENTITY, DATE CODE, AND ALL OTHER ID ON BOTTOM SIDE ETCH APPROXIMATELY WHERE SHOWN.
17. OTHER VENDOR NOMENCLATURE OR MARKINGS SHOULD NOT BE ETCHED OR SILKSCREENED ON BOARD WITHOUT PRIOR PERMISSION.
18. ALL VENDOR IN-PROCESS MARKINGS, QA STAMPS, ETC., MUST BE PLACED ON THE BOTTOM SIDE OF BOARD.
19. FINISHED BOARD MUST MEET UL94V-0 RATING.
20. BOARDS MUST BE NETLIST TESTED FOR OPENS AND SHORTS USING: NETLIST.TXT
21. DOCUMENTATION THAT MUST BE DELIVERED WITH FABRICATED BOARDS.
    CROSS SECTION REPORT (SPACING BETWEEN COPPER LAYERS AND COPPER THICKNESS)
    ELECTRICAL TEST CERTIFICATION OF COMPLIANCE(ACCORDANCE WITH IPC-ET-652 CLASS II)
    CERTIFICATION OF COMPLIANCE(BOARD HAS BEEN MANUFACTURED TO DRAWING REQUIREMENTS)
    IMPEDANCE REPORT (REQUIRED IMPEDANCE TRACES PER NOTE 10)
    RoHS CERTIFICATE OF COMPLIANCE
    MICROSECTION CROSS SECTION
    IONIC CONTAMINATION REPORT (IF APPLICABLE)
22. MUST DELIVER SOLDER SAMPLE BOARD FOR MECHANICAL CHECKING.

BOARD FABRICATION INFORMATION	
	NOMINAL SMALLEST
AIR GAP	.005
TRACE SIZE	.008
HOLE SIZE	.013
PAD SIZE	.020x.025 RECT
SUFRACE MOUNT TOP AND BOTTOM	

UNLESS OTHERWISE SPECIFIED
DO NOT SCALE DRAWING
DIMENSIONS ARE IN INCHES
TOLERANCES ON:
2 PL DECIMALS ± .01
3 PL DECIMALS ± .005
ANGLES 1°
MATERIAL: SEE NOTES
FINISH: SEE NOTES

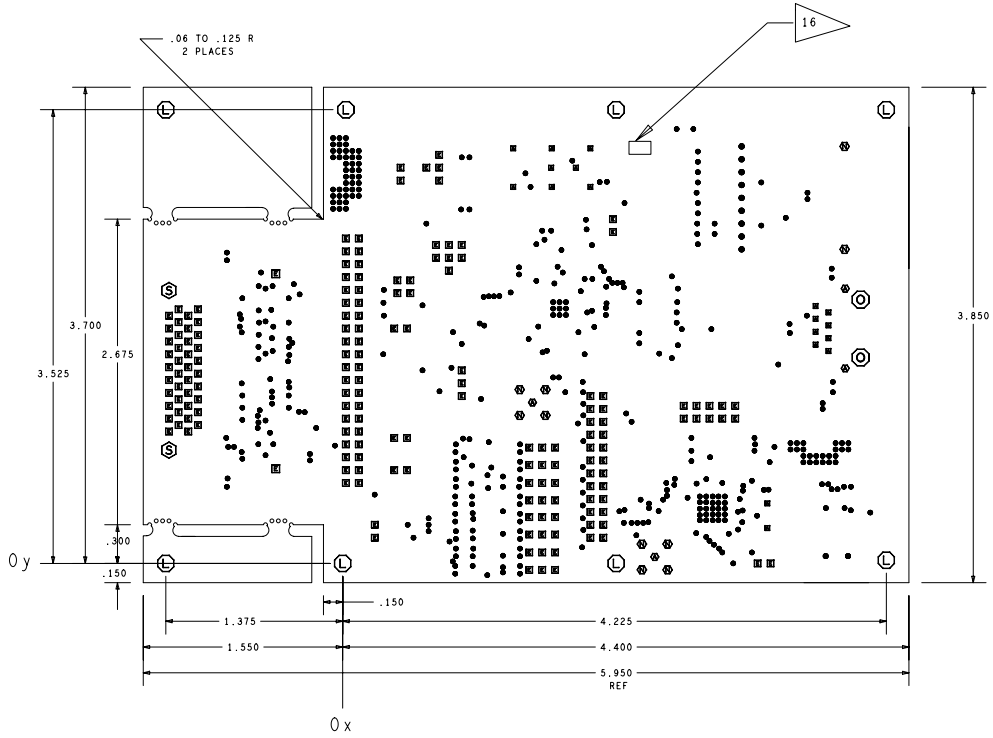
SIGNATURES	DATE
DRAWN BY:	
CHECKED BY:	
APPRVD BY:	
APPRVD BY:	

National Semiconductor
INTERFACE DIVISION

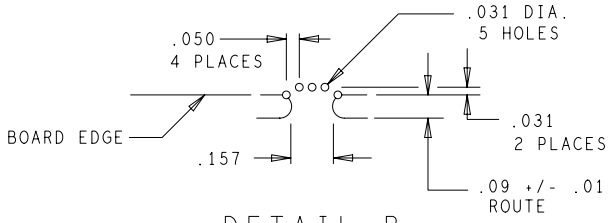
PCB FABRICATION DRAWING
DP83620 SQ48A
PHYTER HP TP/FX DEMO

B | DWG 551600596-001 | A

SCALE: NONE | SHEET 1 OF 3 | REV



VIEWED FROM TOP SIDE



DETAIL B
SCALE: NONE
4 RAIL CUT-OUTS

6

FINISHED HOLE CHART				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
•	13.0	+3.0/-3.0	PLATED	421
•	17.72	+3.0/-3.0	PLATED	2
•	32.0	+3.0/-3.0	PLATED	9
▪	36.0	+3.0/-3.0	PLATED	18
▪	40.0	+3.0/-3.0	PLATED	170
◈	62.0	+3.0/-3.0	PLATED	4
◈	75.0	+3.0/-3.0	PLATED	10
Ⓛ	125.0	+3.0/-3.0	PLATED	8
▪	40.0	+2.0/-2.0	NON-PLATED	2
Ⓢ	106.0	+2.0/-2.0	NON-PLATED	2
◎	128.0	+2.0/-2.0	NON-PLATED	2

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SCALE: NONE	SHEET 2 OF 3	REV

+/- 10% 50 OHM IMPEDANCE

TRACES .012
TOP ETCH (LAYER 1)
BOTTOM ETCH (LAYER 4)

10.

+/- 10% 90 OHM DIFFERENTIAL IMPEDANCE

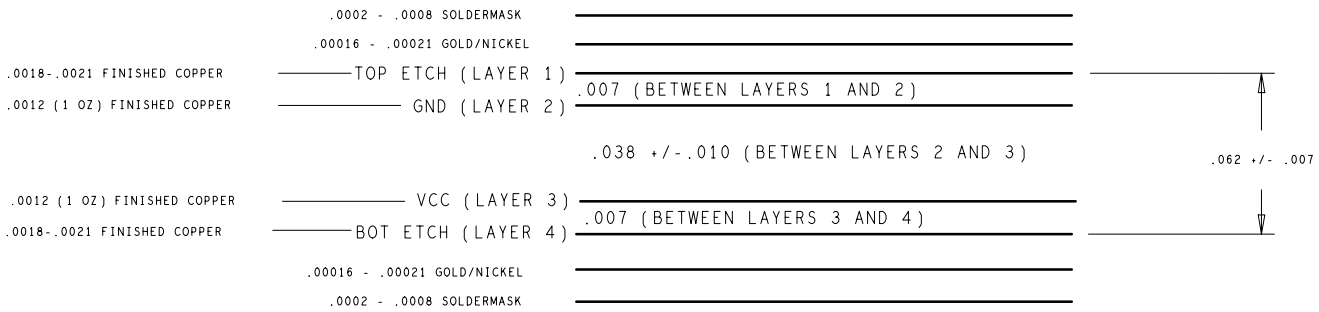
TRACES .010
SPACES .010
TOP ETCH (LAYER 1)
BOTTOM ETCH (LAYER 4)

10.

+/- 10% 100 OHM DIFFERENTIAL IMPEDANCE

TRACES .008
SPACES .012
TOP ETCH (LAYER 1)
BOTTOM ETCH (LAYER 4)

10.



DETAIL A

LAYER STACK-UP
SCALE: NONE

1.A 1.D 1.B 9.B 1.C

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PCB FABRICATION DRAWING
DP83620 SQ48A
PHYTER HP TP/FX DEMO

B	DWG 551600596-001	A
SCALE: NONE	SHEET 3 OF 3	REV