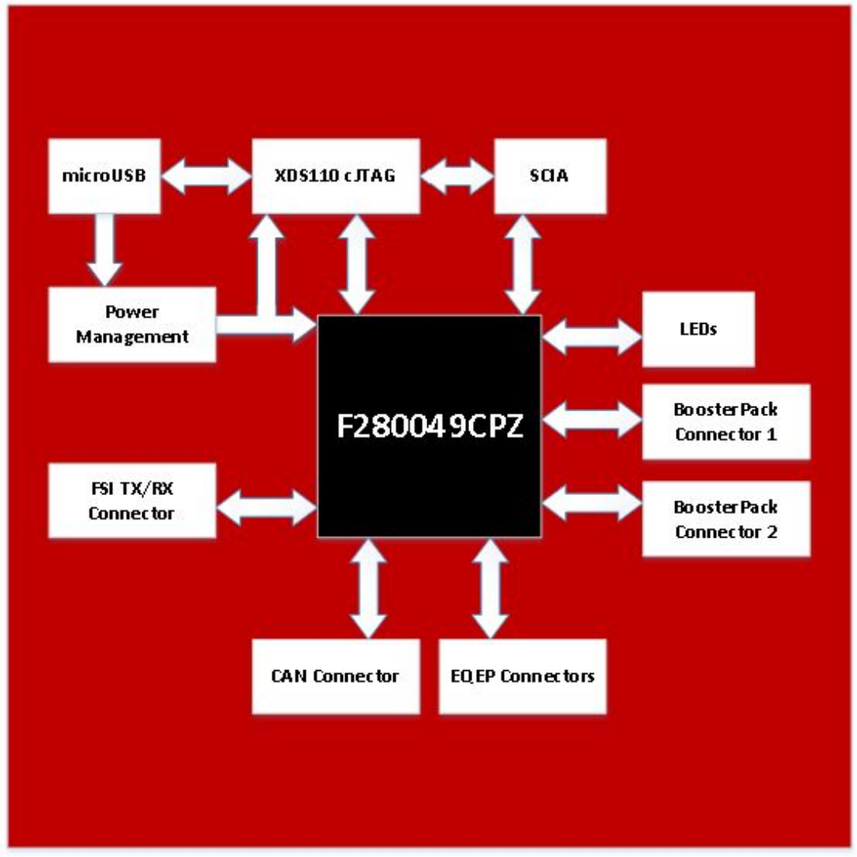

Orderable: LAUNCHXL-F280049C		Designed for: Public Release	Mod. Date: 11/1/2019
TID #: N/A		Project Title: LAUNCHXL-F280049C	
Number: MCU025	Rev: B	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 1 of 8
Drawn By:		File: MCU025B_Block_Diagram.SchDoc	Size: B
Engineer: a0232540		Contact: http://www.ti.com/support	

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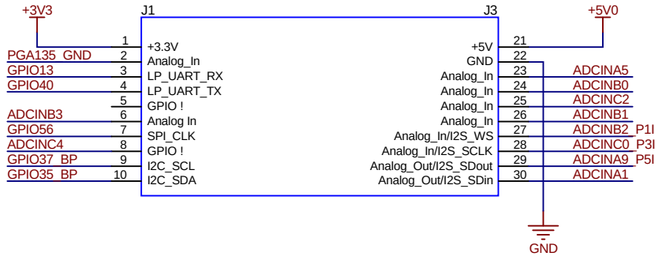
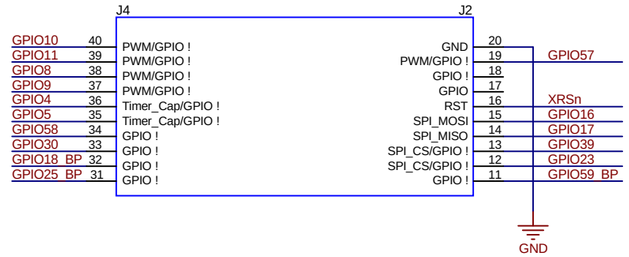
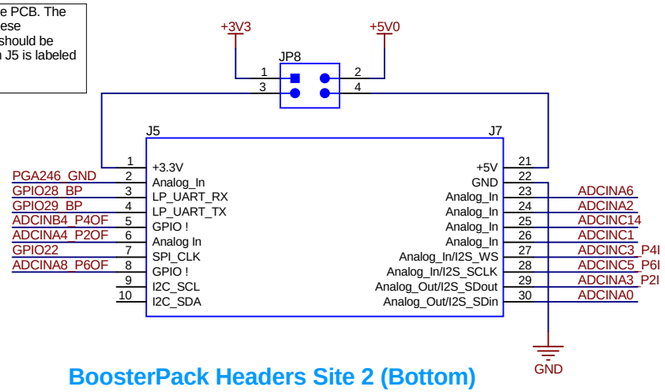


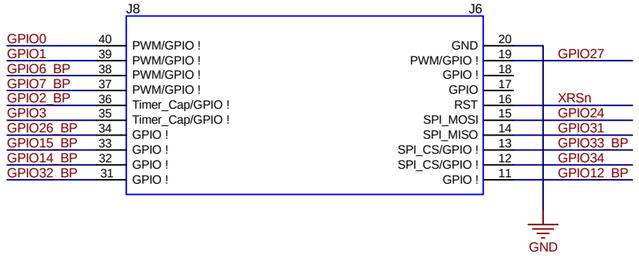
BoosterPack Headers Site 1 (Top)



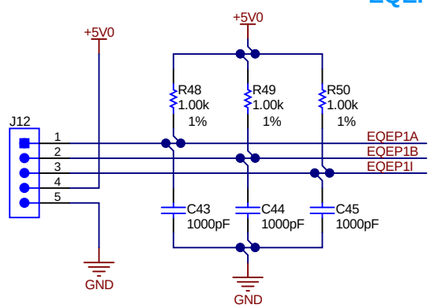
J5 - J8 are labeled on the PCB. The Pin numbers listed on these schematic components should be offset by 40. i.e. pin 1 on J5 is labeled as pin 40 on the PCB.

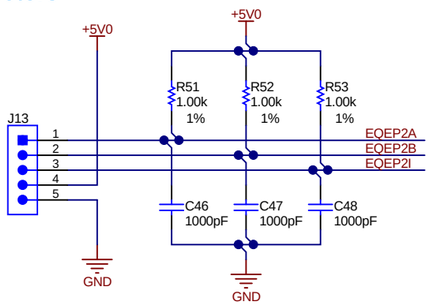


BoosterPack Headers Site 2 (Bottom)

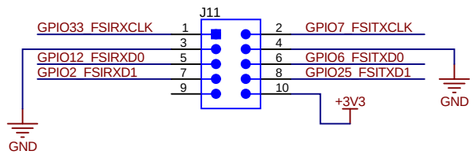


EQEP Connectors

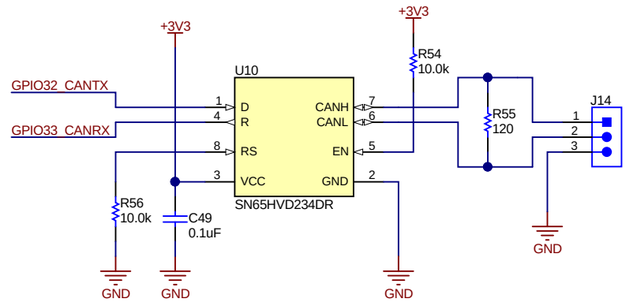




FSI Connector



CAN Connector



Orderable: LAUNCHXL-F280049C		Designed for: Public Release	Mod. Date: 12/12/2019
TID #: N/A		Project Title: LAUNCHXL-F280049C	
Number: MCU025	Rev: B	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 2 of 8
Drawn By:		File: MCU025B_Connectors.SchDoc	Size: B
Engineer: a0232540		Contact: http://www.ti.com/support	

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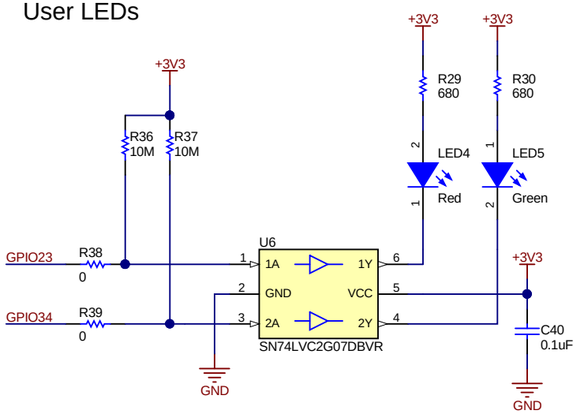
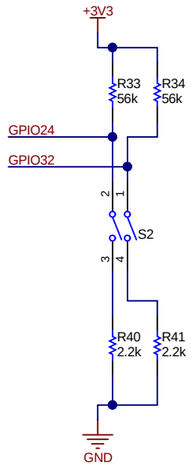
User LEDs





Boot Mode Select

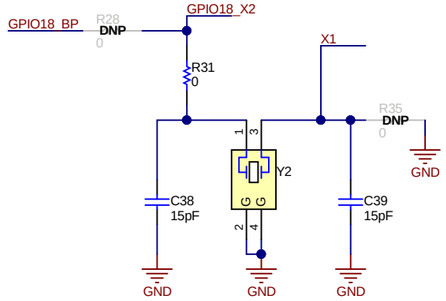
Selected Boot Mode Chart

S2 placed upside-down (so UP is open (1), DOWN is closed (0))

Mode #	GPIO24	GPIO32	Boot Mode
00	0	0	Boot from Parallel GPIO
01	0	1	Boot from SCI / Wait Mode
02	1	0	Boot from CAN
03	1	1	Boot from Flash

Oscillator

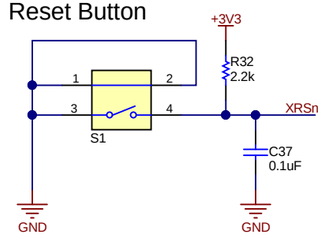
Route cleanly and place near U1



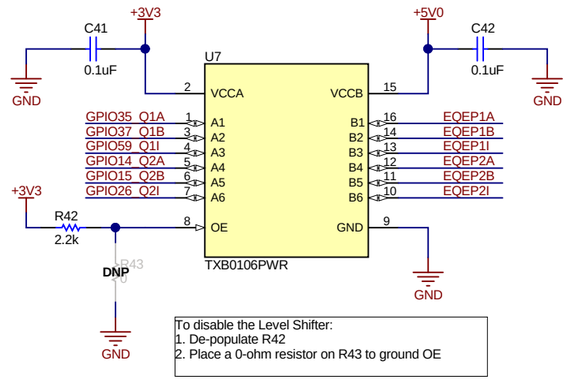
By default:
- Crystal Y2 is connected between X1 and X2.
- GPIO18_BP is not connected to the BoosterPack header.

If GPIO18 is needed at the Boosterpack Headers:
- Remove R35
- Place 0ohm resistors on both R31 and R28

Reset Button



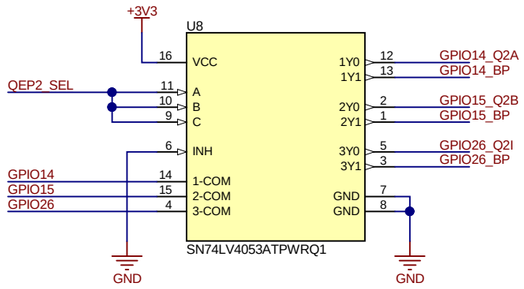
EQEP Level Shifter

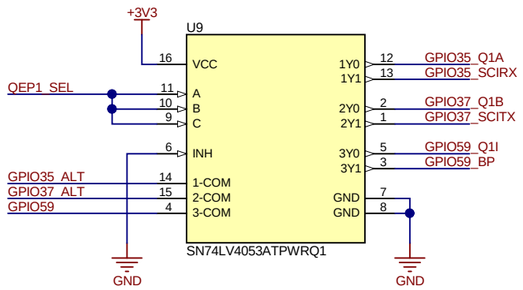


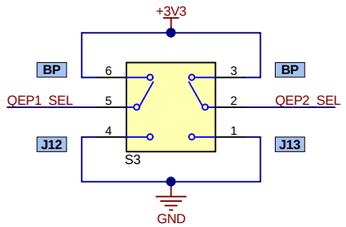
To disable the Level Shifter:
1. De-populate R42
2. Place a 0-ohm resistor on R43 to ground OE

UART Routing

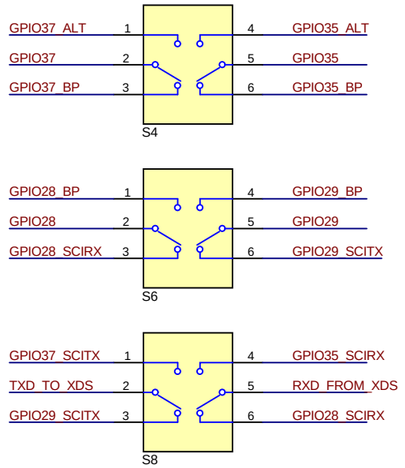
EQEP Routing





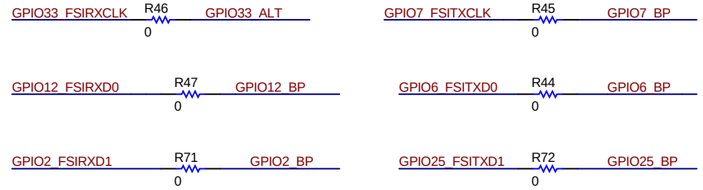


S3 (1, UP): QEP signals are routed to the BoosterPack Headers (default)
S3 (0, DOWN): QEP signals are routed to the QEP Headers



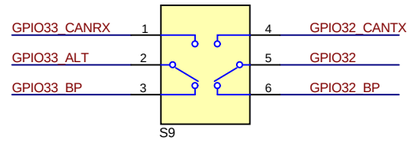
S8 is placed upside-down so the 0 position is 'up' towards the debug probe

FSI and CAN Routing



If needed, depopulate the resistors to isolate the BP headers from the FSI Headers. By default all are connected.

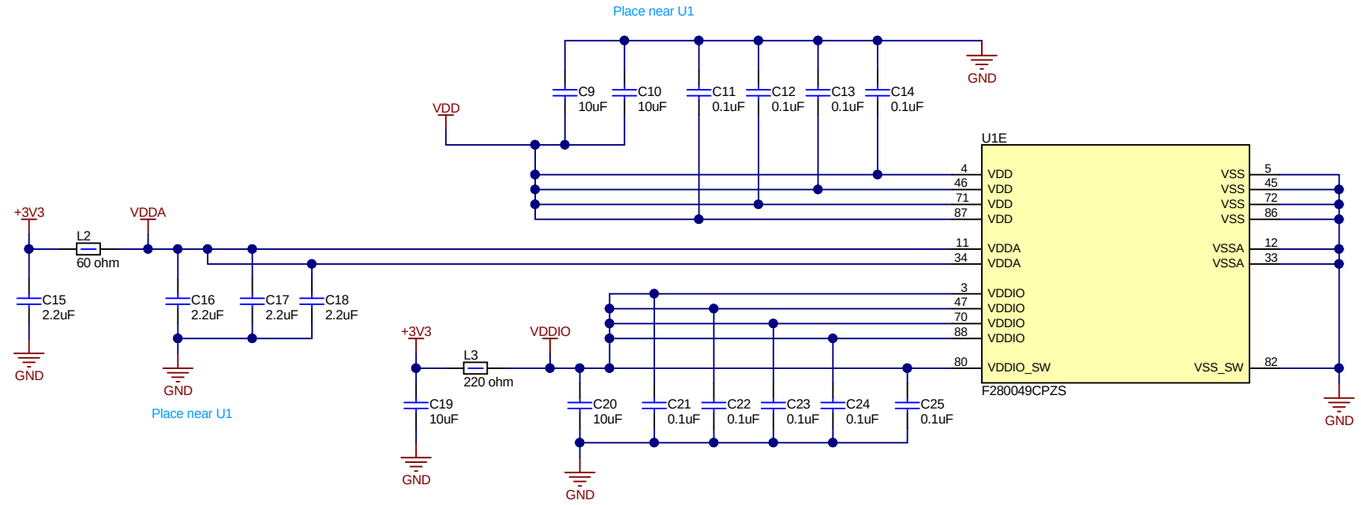
FSI routing will be as clean as possible to FSI header. BP resistors will be branches with short stubs off of main branch to reduce noise on high speed lines

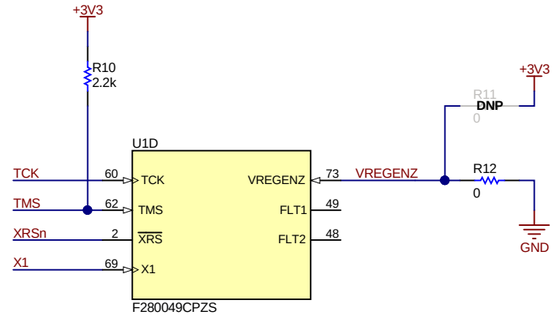


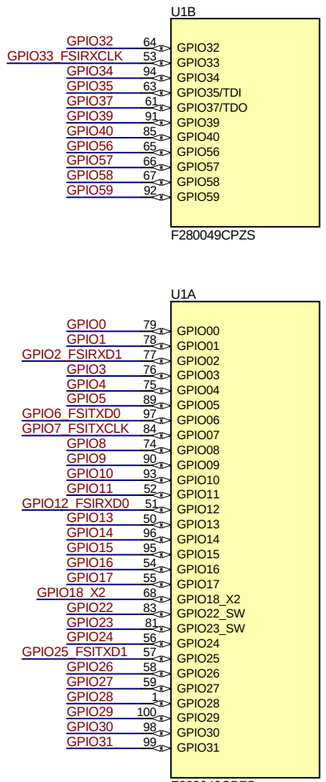
If CAN functionality is desired, ensure that R46 is populated with a 0-ohm resistor.

Orderable: LAUNCHXL-F280049C		Designed for: Public Release	Mod. Date: 12/4/2019
TID #: N/A		Project Title: LAUNCHXL-F280049C	
Number: MCU025	Rev: B	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 3 of 8
Drawn By:		File: MCU025B_AltRouting_Misc.SchDoc	Size: B
Engineer: a0232540		Contact: http://www.ti.com/support	

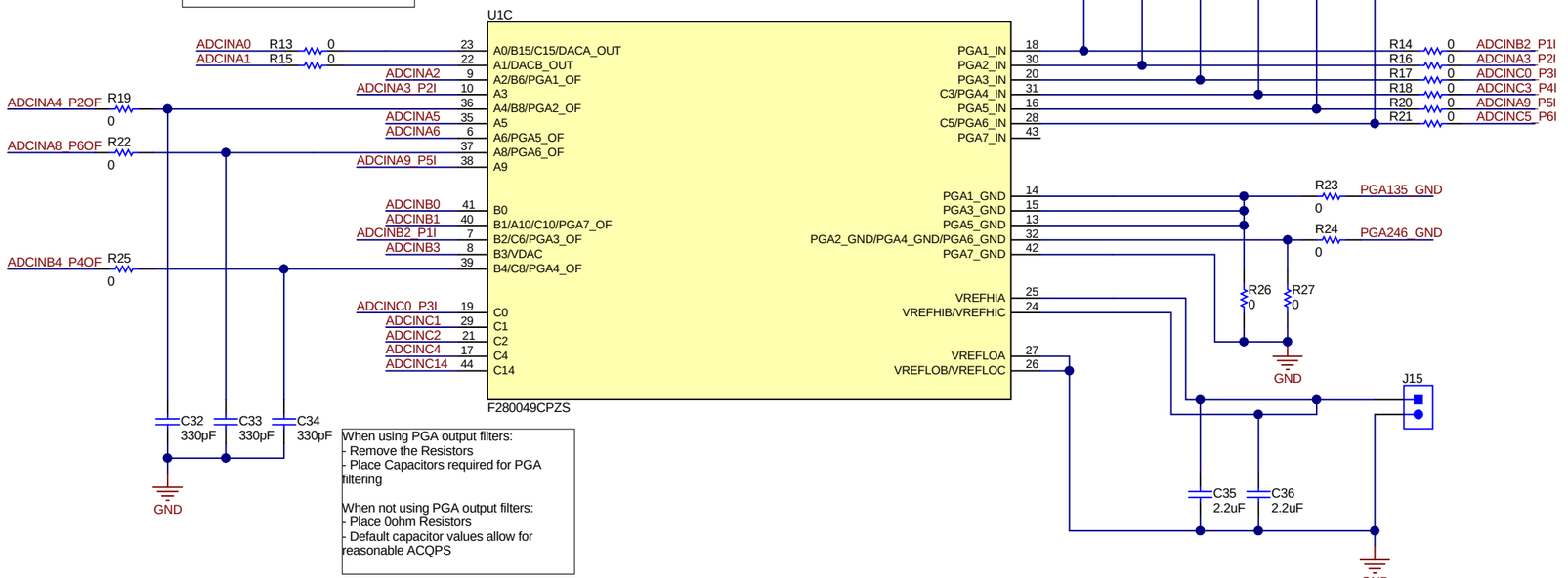
http://www.ti.com







A 0ohm series resistor has been placed on each DAC out pin. If there is not enough output resistance for the DAC, replace the 0ohm resistor with an appropriate value



Orderable: LAUNCHXL-F280049C		Designed for: Public Release	Mod. Date: 11/12/2019
TID #: N/A		Project Title: LAUNCHXL-F280049C	
Number: MCU025	Rev: B	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 4 of 8
Drawn By:		File: MCU025B_F280049C_Device.SchDoc	Size: B
Engineer: a0232540		Contact: http://www.ti.com/support	

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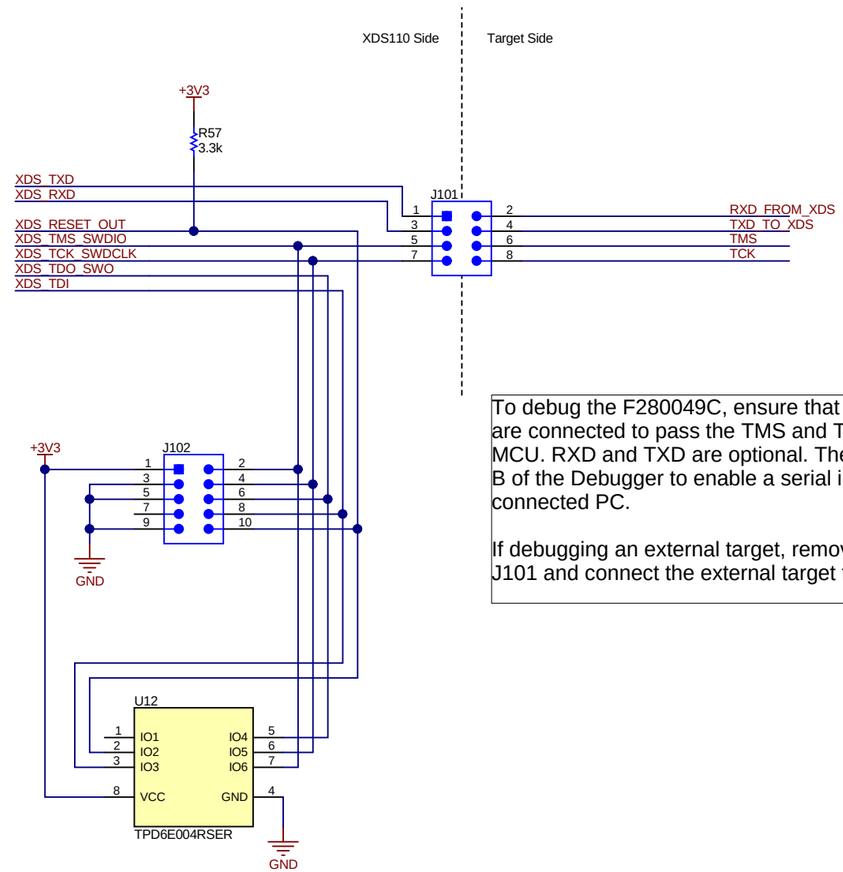
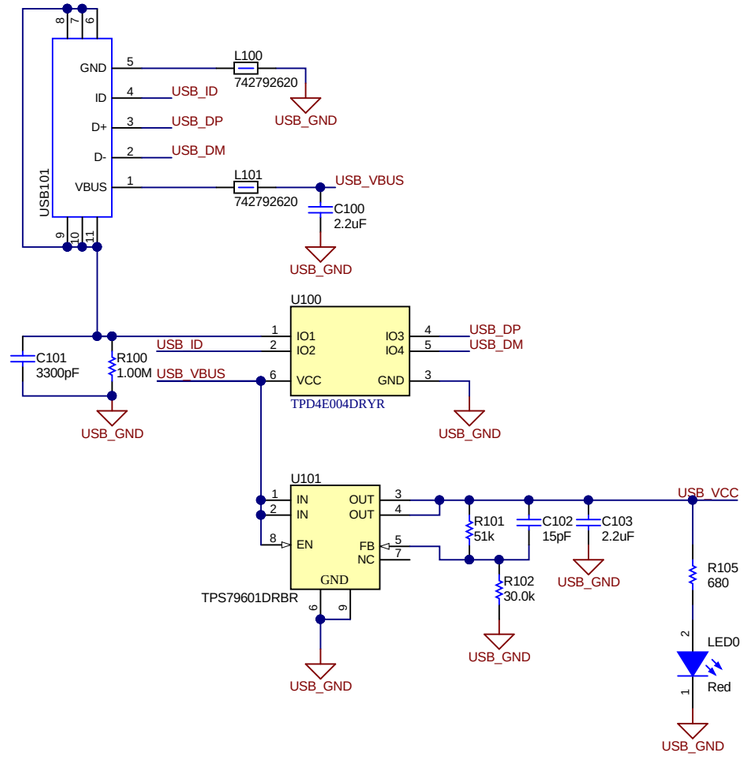


To debug the F280049C, ensure that the jumpers on J101 are connected to pass the TMS and TCK signals to the MCU. RXD and TXD are optional. These are for Channel B of the Debugger to enable a serial interface to the connected PC.

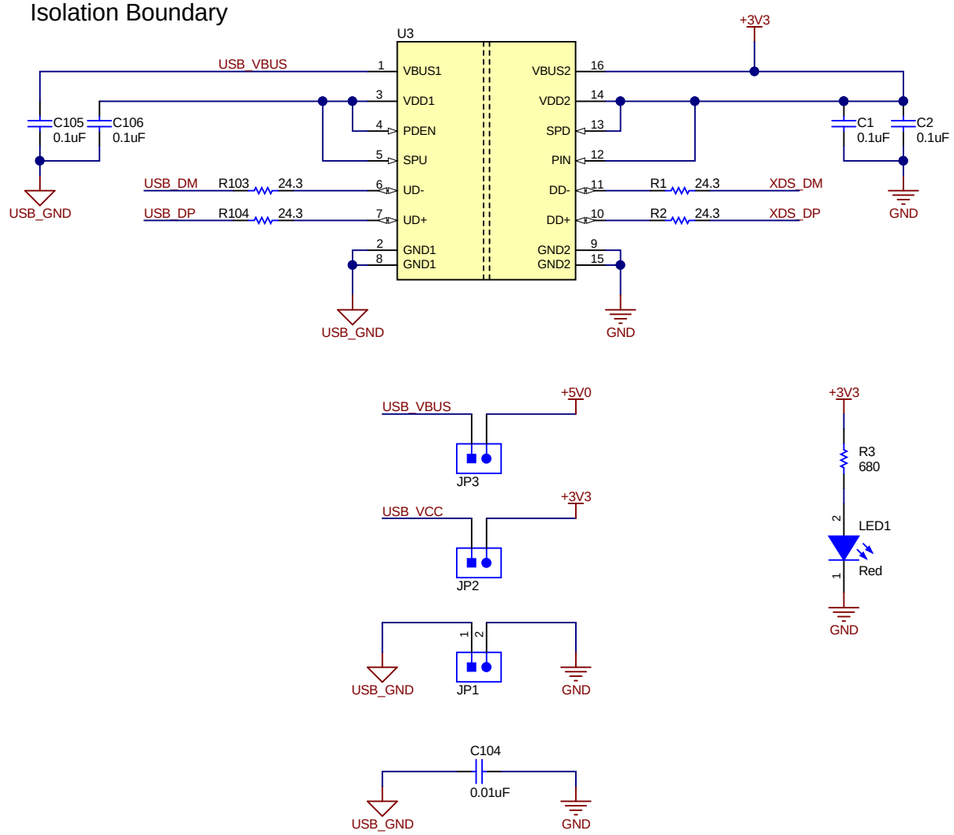
If debugging an external target, remove the jumpers from J101 and connect the external target to J102.

Orderable: LAUNCHXL-F280049C		Designed for: Public Release	Mod. Date: 11/1/2019
TID #: N/A		Project Title: LAUNCHXL-F280049C	
Number: MCU025	Rev: B	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 5 of 8
Drawn By:		File: MCU025B_XDS110_Target_Interface.SchDoc	Size: B
Engineer: a0232540		Contact: http://www.ti.com/support	

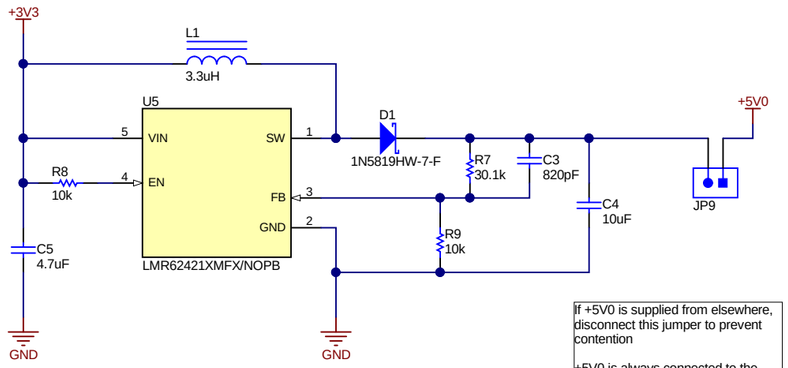
USB & XDS Power



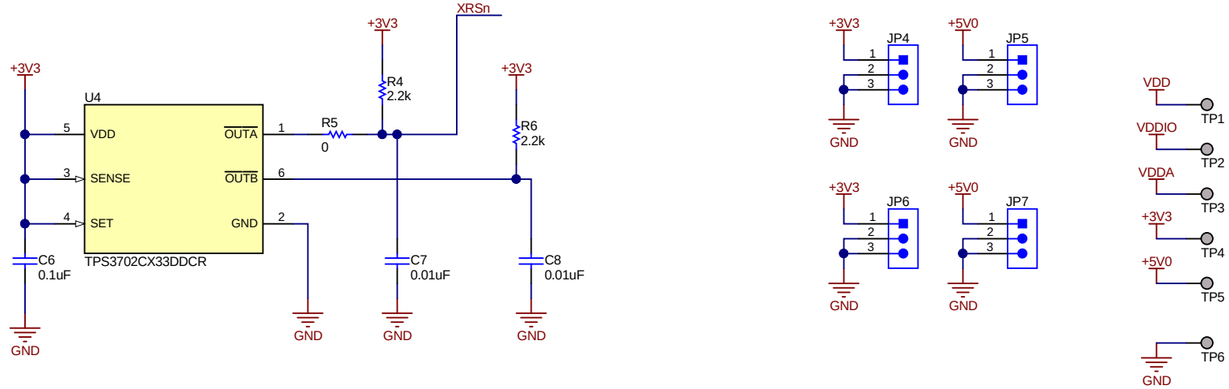
Isolation Boundary



3.3V to 5V Boost



System Supervisory Circuit



Orderable: LAUNCHXL-F280049C		Designed for: Public Release	Mod. Date: 11/18/2019
TID #: N/A		Project Title: LAUNCHXL-F280049C	
Number: MCU025	Rev: B	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 6 of 8
Drawn By:		File: MCU025B_XDS110_USB_Power.SchDoc	Size: B
Engineer: a0232540		Contact: http://www.ti.com/support	

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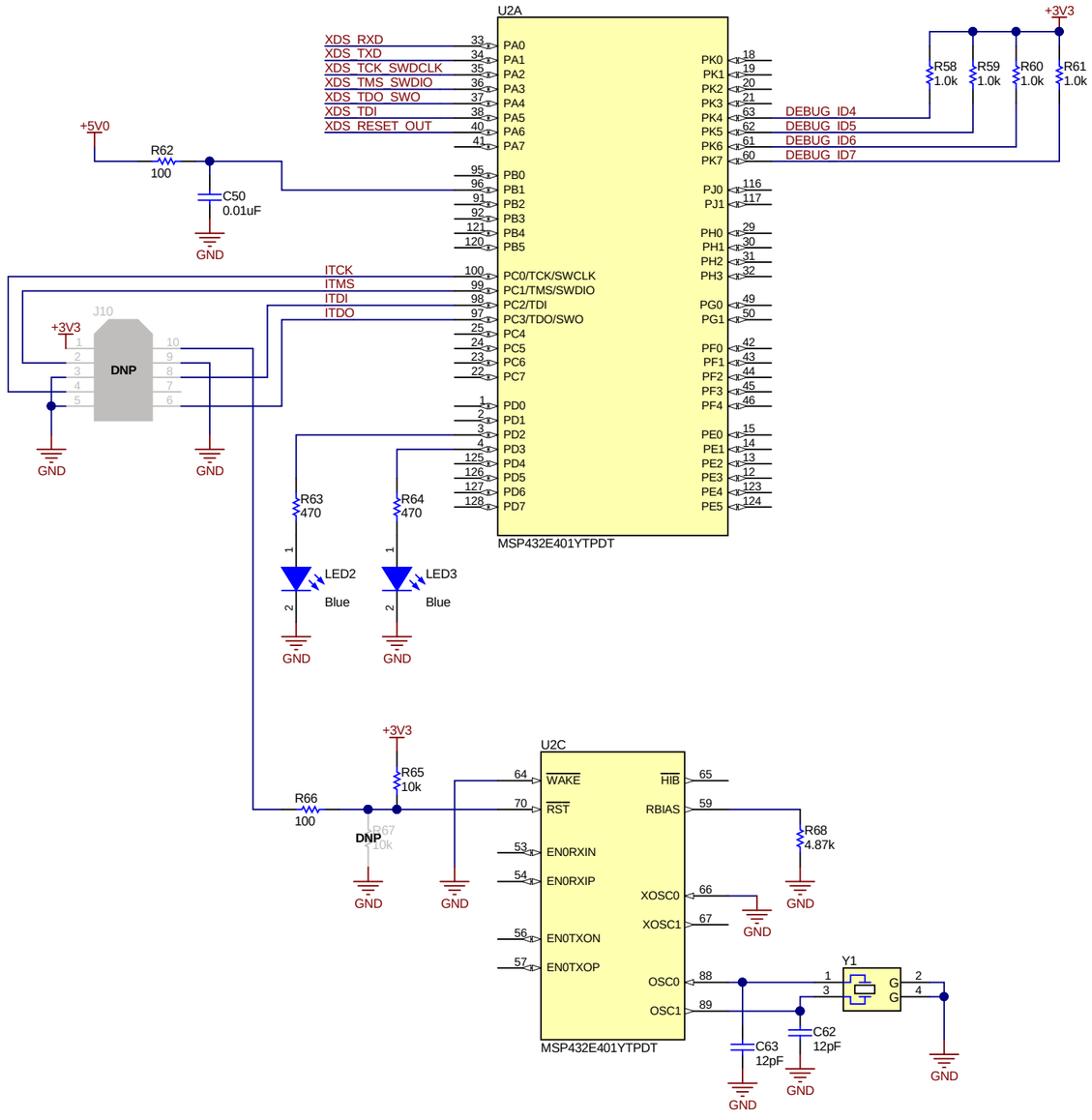

Orderable: LAUNCHXL-F280049C		Designed for: Public Release	Mod. Date: 11/12/2019
TID #: N/A		Project Title: LAUNCHXL-F280049C	
Number: MCU025	Rev: B	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 7 of 8
Drawn By:		File: MCU025B_XDS110_MCU.SchDoc	Size: B
Engineer: a0232540		Contact: http://www.ti.com/support	

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DNP FID1 DNP FID2 DNP FID3

DNP FID4 DNP FID5 DNP FID6

MH1 MH2

MH3 MH4

PCB Number: MCU025
PCB Rev: B

Logo1
PCB
LOGO
Texas Instruments

CE Logo1

Logo4
PCB
LOGO
INSTASPIN_FOC_LOGO

Logo3
PCB
LOGO
FCC disclaimer

Logo2
PCB
LOGO
WEEE logo

H1
MECH
AK67421-0.3

M1 M2 M3 M4 M5 M6 M7 M8 M9

ZZ2
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Orderable: LAUNCHXL-F280049C		Designed for: Public Release	Mod. Date: 11/19/2019
TID #: N/A		Project Title: LAUNCHXL-F280049C	
Number: MCU025	Rev: B	Sheet Title:	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 8 of 8
Drawn By:		File: MCU025B_Hardware.SchDoc	Size: B
Engineer: a0232540		Contact: http://www.ti.com/support	

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