AM62x SKEVM WITH FULTON PMIC

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REV	A1
VER	0.11

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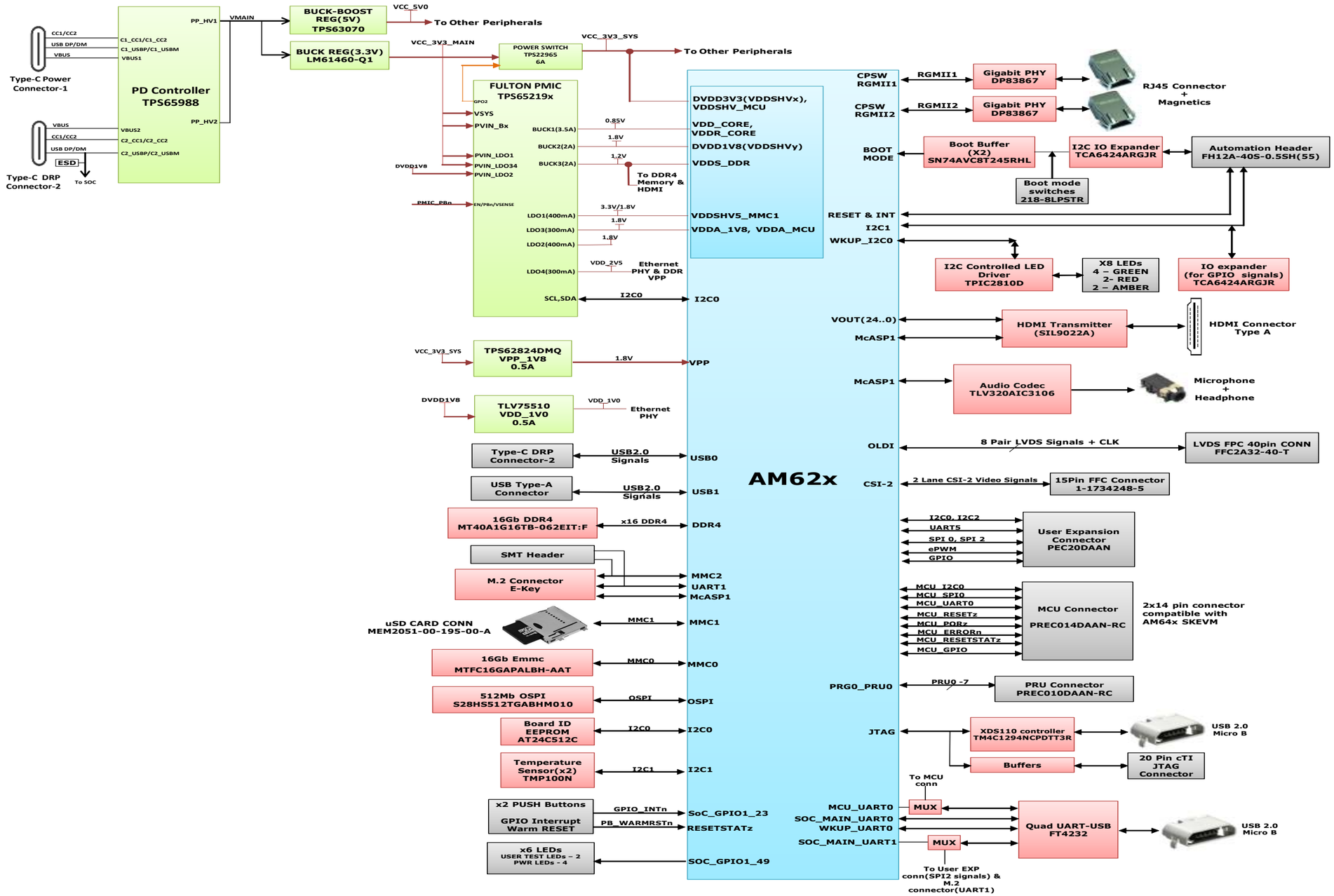
REVISION HISTORY

VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
0.01	29 AUG 2022	Drafted from PROC142E1 Schematics. R651 value changed to 1K. DNI'd R618 and R676.Changed the I2C buffer parts to TCA9517DR. Changed the part SN74AVC4T245RSVR to SN74AVC4T245DGVR	Mistral Design Team		
0.02	08 SEP 2022	Added the second GPIO Expander U110 Part# TCA6408ARGTR	Mistral Design Team		
0.03	21 SEP 2022	Changed the Current monitors Res Filter values from 10E to 0E to the Sense pins.	Mistral Design Team		
0.04	19 OCT 2022	Added Testpoint to TEMP_DIODE_P pin of SoC. Changed the GPIO_OLDI_RSTn net name to GPIO_TS_RSTn.	Mistral Design Team		
0.05	24 OCT 2022	Changed the Fulton PMIC part from TPS6521903RHBR to TPS6521904RHBR. Mounted R699 and DNI'd R123. DNI'd the current monitor section of U36	Mistral Design Team		
0.06	3 Nov 2022	Changed the DDR4 part from MT40A1G16KD-062E IT:E to MT40A1G16TB-062E IT:F. Changed the eMMC part from MTFC16GAPALBH-IT to MTFC32GAZAQHD-IT.	Mistral Design Team		
0.07	15 Nov 2022	Removed the PMIC_STBY connection from SOC to PMIC.	Mistral Design Team		
0.08	22 Nov 2022	Added 2x 47uF on VCC_5V0. DNI'd C432, C433(10uF) and changed C415 to 4.7uF. Added 22pF CAP across R108	Mistral Design Team		
0.09	1 Dec 2022	Removed MMC2 connector section (J18) and associated resistors	Mistral Design Team		
0.10	11 APR 2023	Changed the HDMI external swing resistance to 7.5K. Added Standoff,Screw & Washer for M.2 connector. DNI'd R650 on SoC_USB1_DRVVBUS	Mistral Design Team		
0.11	16 MAY 2023	Depopulated Pull up of SOC_WLAN_IRQ_1V8 (R6)	Mistral Design Team		

BLOCK DIAGRAM



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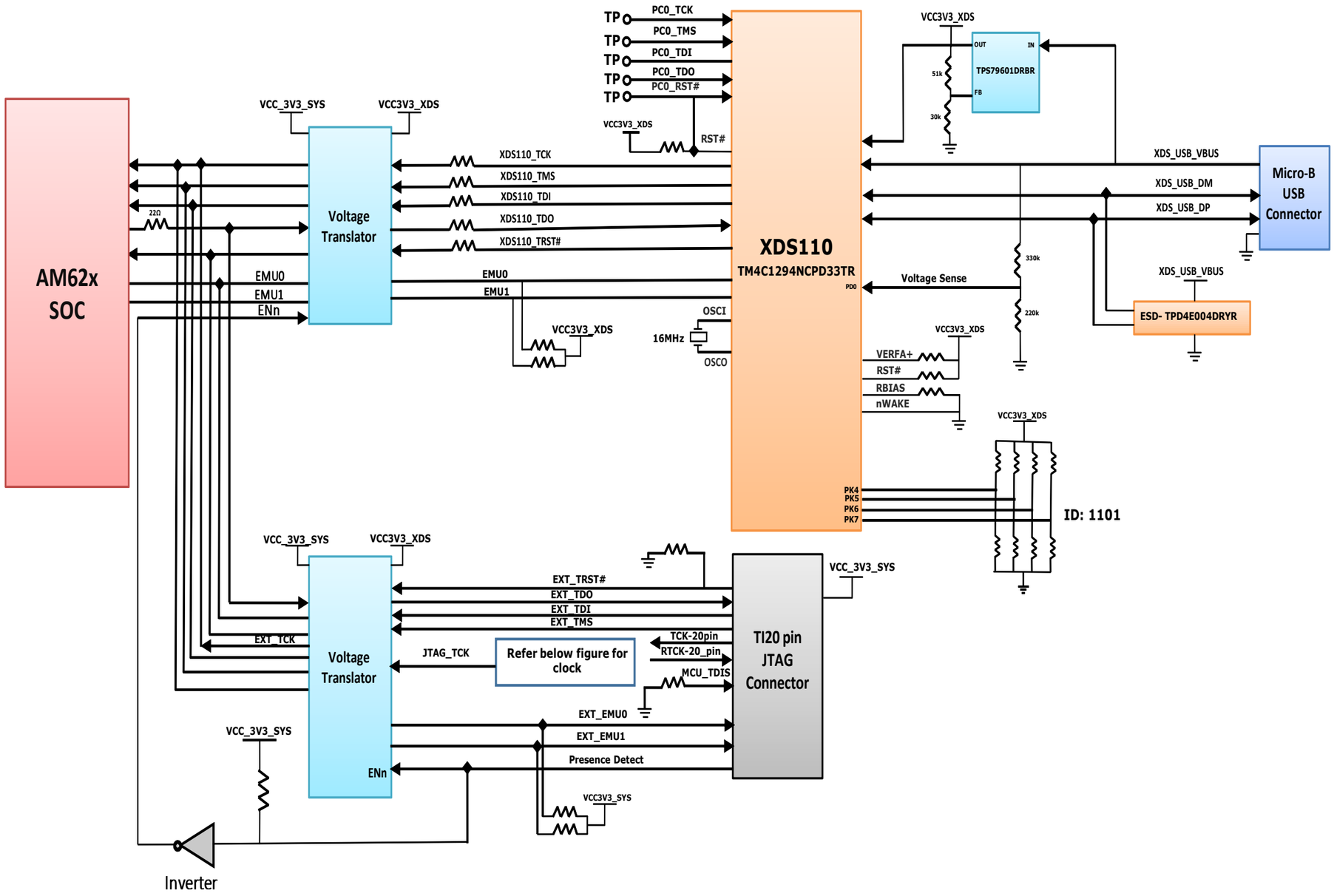
BLOCK DIAGRAM_XDS110



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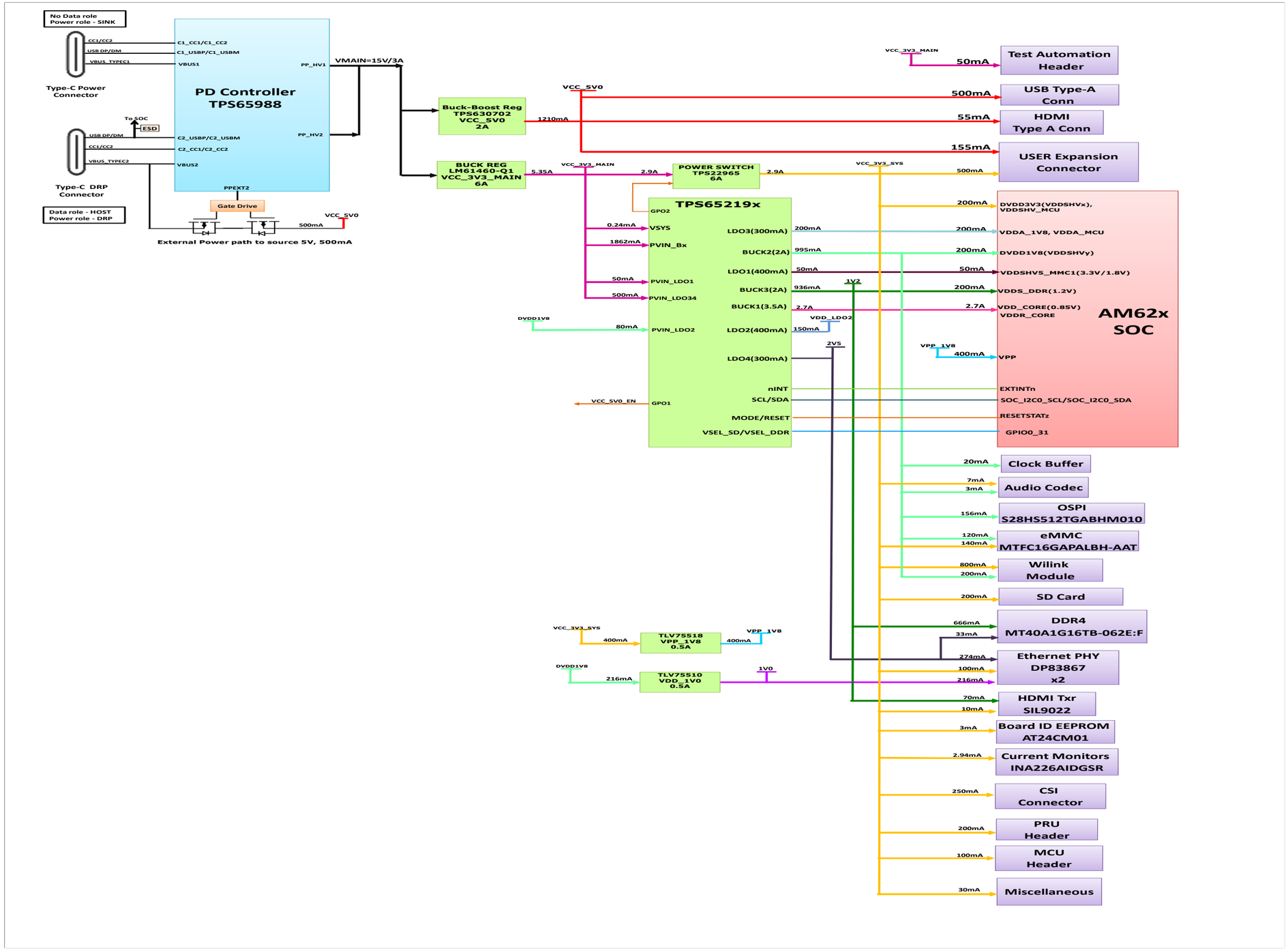
POWER BLOCK DIAGRAM



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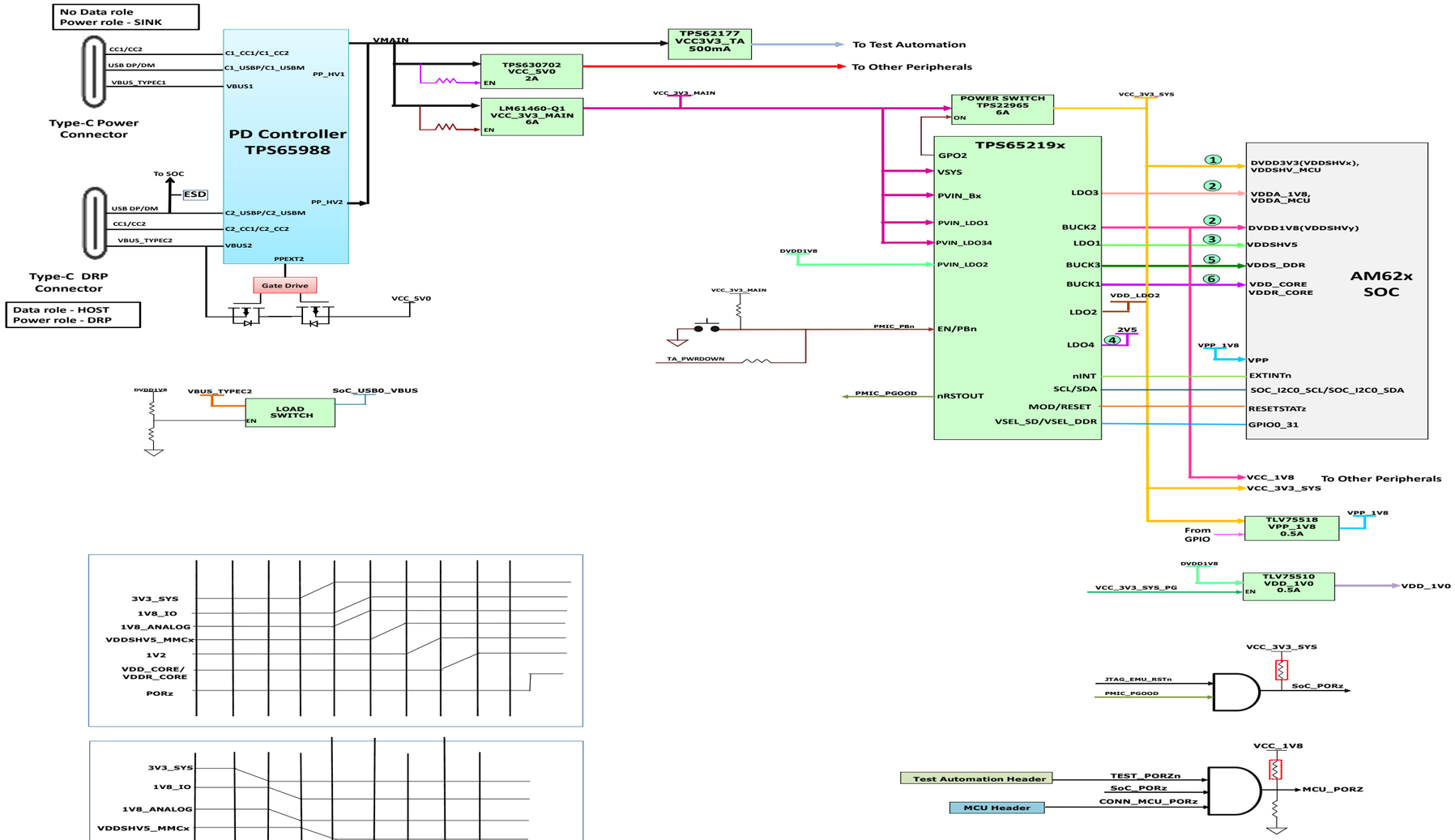
POWER SEQUENCE



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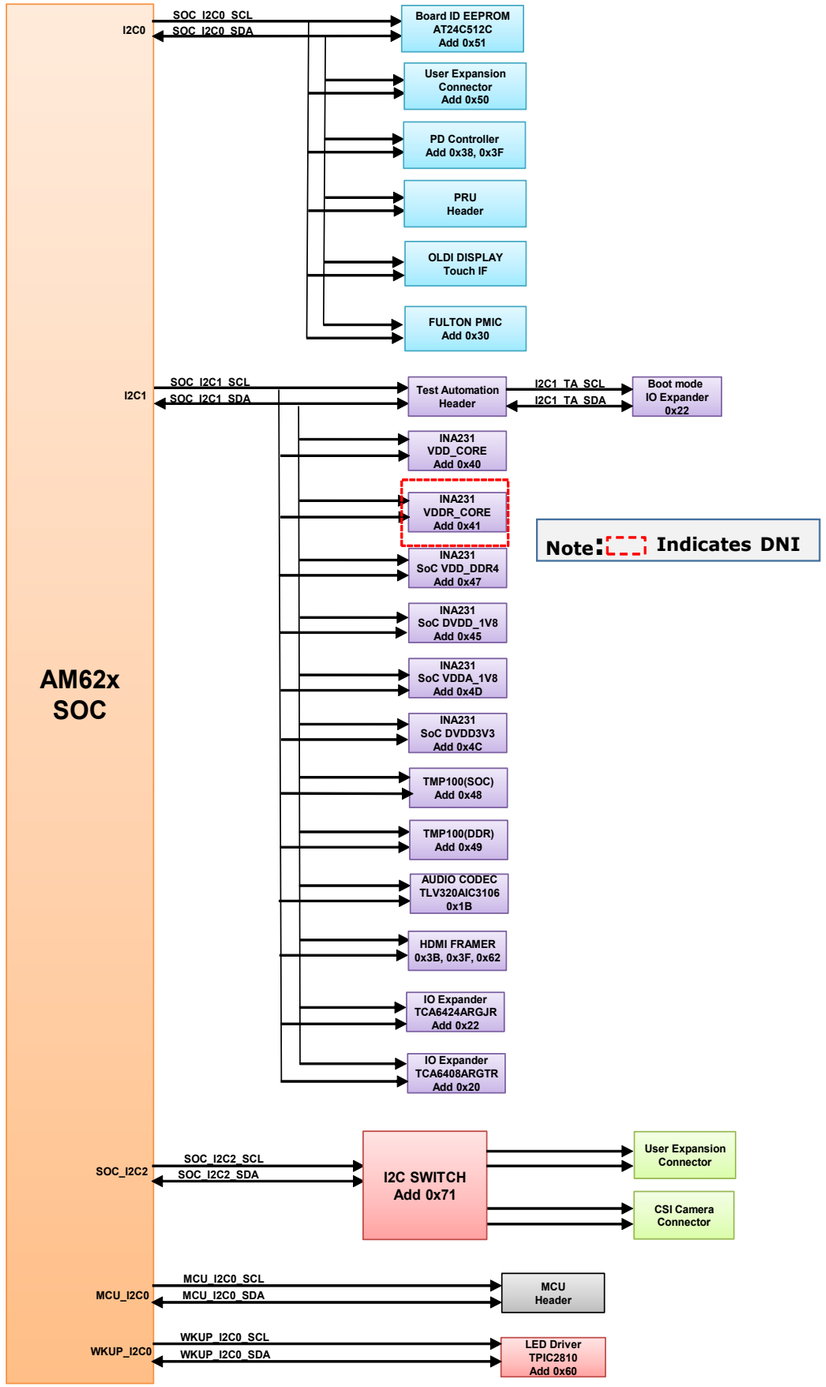
I2C TREE



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Title	I2C TREE		
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GPIO MAPPING TABLE

SL NO.	GPIO DESCRIPTION	GPIO NETNAME	Functionality	GPIO USED	SOC MUXED SIGNAL NAME	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE	VOLTAGE DOMAIN ON SOC SIDE	VOLTAGE CONNECTED ON SKEVM
1	Enable for WLAN Interface	SoC_WLAN_EN_1V8	ENABLE	GPIO0_71	MMC2_SDCD	OUTPUT	LOW	HIGH	VDDSHV6	SoC_DVDD1V8
2	WLAN Interrupt	SoC_WLAN_IRQ_1V8	INTERRUPT	GPIO0_72	MMC2_SDWP	INPUT	HIGH	LOW	VDDSHV6	SoC_DVDD1V8
3	Enable for BT Interface	BT_EN_SOC_3V3	ENABLE	MCU_GPIO0_1	MCU_SPI0_CS0	OUTPUT	HIGH	LOW	VDDSHV_MCU	SoC_DVDD3V3
4	CPSW Ethernet PHY Interrupt PRU Connector Interrupt PMIC_INTn	CPSW_RGMII_INTn/PRU_INTn	INTERRUPT	GPIO1_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
5	OSPI Reset Control GPIO	GPIO_OSPI_RSTn	RESET	GPIO0_12	OSPI0_CSn1	OUTPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
6	OSPI Interrupt	OSPI_INTn	INTERRUPT	GPIO0_13	OSPI0_CSn2	INPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
7	SD Card IO Voltage Select	VSEL_SD	ENABLE	GPIO0_31	GPMC0_CLK	OUTPUT	LOW	HIGH	VDDSHV3	SoC_DVDD3V3
8	IO Expander Interrupt	MCU_GPIO0_15	INTERRUPT	MCU_GPIO0_15	MCU_MCAN1_TX	INPUT	HIGH	LOW	VDDSHV_CANUART	SoC_DVDD3V3
9	TEST GPIO1 from Test Automation Connector/ User Interrupt Push Button									
10	User Test LED 1	SOC_GPIO1_49	GPIO	GPIO1_49	MMC1_SDWP	OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
IO EXPANDER - 01										
1	CPSW Ethernet PHY-2 Reset Control GPIO	GPIO_CPSW2_RST	RESET	IO EXPANDER - P01		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
2	CPSW Ethernet PHY-1 Reset Control GPIO	GPIO_CPSW1_RST	RESET	IO EXPANDER - P01		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
3	PRU Board Detection	PRU_DETECT	DETECTION	IO EXPANDER - P02		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
4	SD Card Load Switch Enable	MMC1_SD_EN	ENABLE	IO EXPANDER -P03		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
5	SOC eFuse Voltage(VPP=1.8V) Regulator Enable	VPP_LDO_EN	ENABLE	IO EXPANDER - P04		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
6	EXP CONN 3.3V Power Switch Enable	EXP_PS_3V3_EN	ENABLE	IO EXPANDER - P05		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
7	EXP CONN 5V Power Switch Enable	EXP_PS_5V0_EN	ENABLE	IO EXPANDER - P06		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
8	EXP CONN HAT Board Detection	RPI_HAT_DETECT	DETECTION	IO EXPANDER - P07		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
9	M.2 Connector Alert	WLAN_ALERT_3V3	ALERT	IO EXPANDER – P10		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
10	M.2 Connector WAKEUP	BT_UART_WAKE_SOC_3V3	WAKEUP	IO EXPANDER – P11		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
11	SOC UART1 Mux Select	UART1_MUX_SEL	SELECT	IO EXPANDER - P12		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
12	Enable for Wilink Level Translators	WL_LT_EN	ENABLE	IO EXPANDER - P13		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
13	HDMI Transmitter Reset Control GPIO	GPIO_HDMI_RSTn	RESET	IO EXPANDER - P14		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
14	Raspberry Pi Camera CSI0 GPIO1	CSI_GPIO1	INPUT/OUTPUT	IO EXPANDER - P15		NA	NA	NA	VDDSHV0	SoC_DVDD3V3
15	Raspberry Pi Camera CSI0 GPIO2	CSI_GPIO2	INPUT/OUTPUT	IO EXPANDER - P16		NA	NA	NA	VDDSHV0	SoC_DVDD3V3
16	PRU Power Switch Enable	PRU_3V3_EN	ENABLE	IO EXPANDER - P17		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
17	HDMI Interrupt	HDMI_INTn	INTERRUPT	IO EXPANDER - P20		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
18	TEST GPIO2 from Test Automation Connector	TEST_GPIO2	GPIO for communications with AM62x	IO EXPANDER - P21		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
19	MCASP2 Enable and Direction Control	AUD_BUF_EN	ENABLE	IO EXPANDER - P22		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
20		WL_BUF_EN	ENABLE	IO EXPANDER - P23		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
21		AUD_BUF_CLK_DIR	DIRECTION CONTROL	IO EXPANDER - P24		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
22		WL_BUF_CLK_DIR	DIRECTION CONTROL	IO EXPANDER - P25		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
23	OLDI Display Touch Interrupt	TS_INT#	INTERRUPT	IO EXPANDER - P26		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
24	User Test LED 2	IO_EXP_TEST_LED	GPIO	IO EXPANDER - P27		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
IO EXPANDER - 02										
1	M.2 Connector SDIO Reset Control GPIO	WLAN_SDIO_RST_3V3	RESET	IO EXPANDER – P0		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
2	OLDI Display Reset control	GPIO_TS_RSTn	RESET	IO EXPANDER – P1		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
3	Audio Codec Reset Control GPIO	GPIO_AUD_RSTn	DETECTION	IO EXPANDER – P2		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
4	eMMC Reset control GPIO	GPIO_eMMC_RSTn	RESET	IO EXPANDER – P3		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3

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TEXAS INSTRUMENTS

MISTRAL

Title	GPIO MAPPING TABLE		
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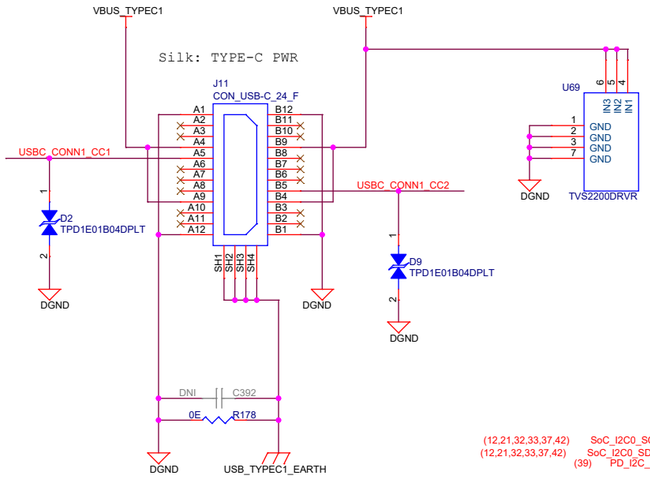
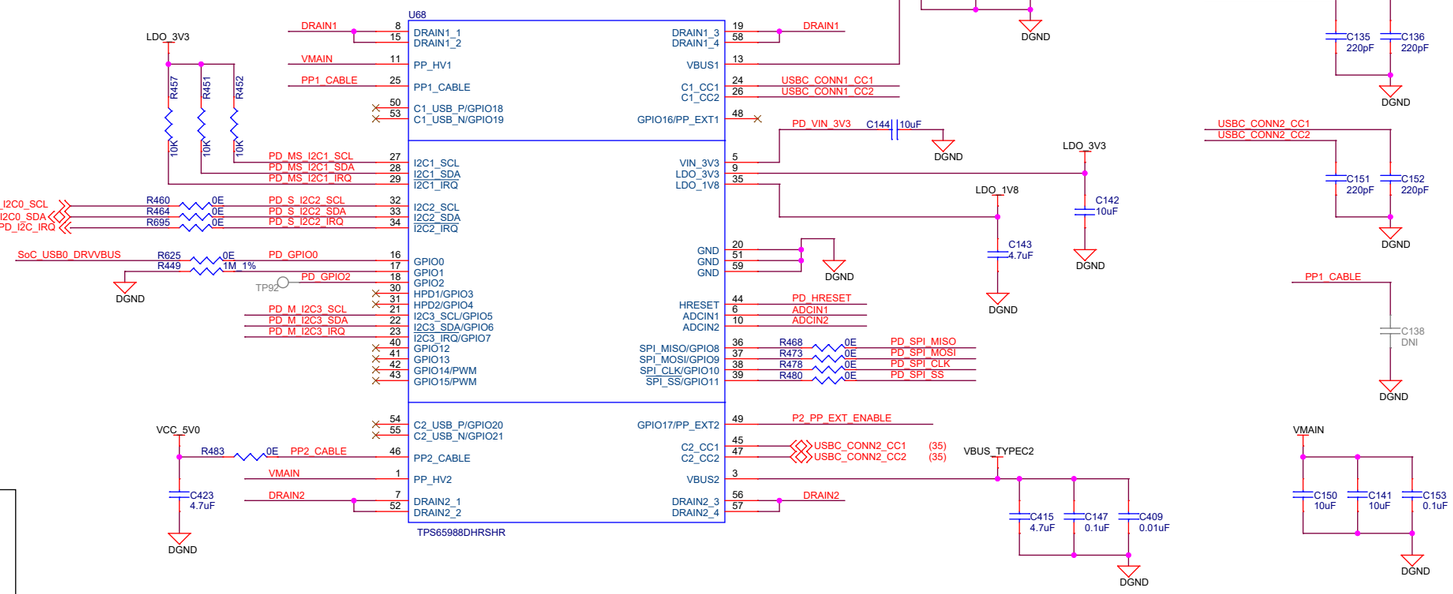
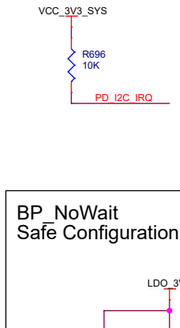
USB TYPE-C POWER

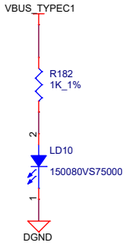


TYPE-C DUAL PD CONTROLLER



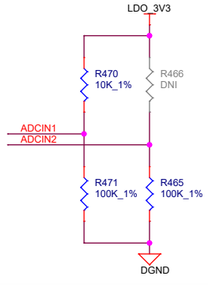


POWER INDICATION LED: VBUS_TYPEC1

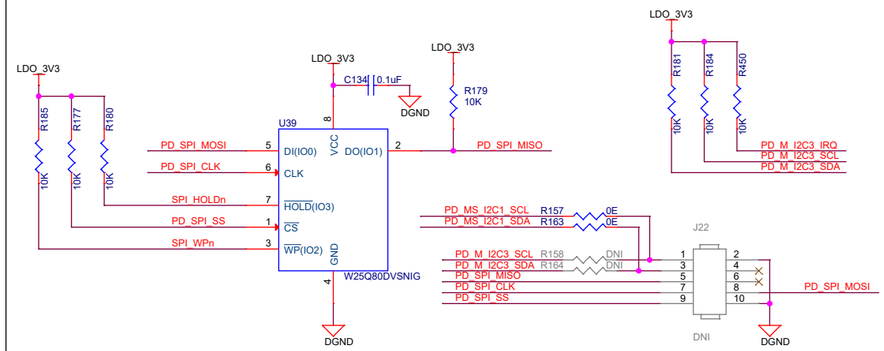


I2C Slave Address	Port1	Port2
I2C2(Default)	0x38	0x3F
I2C1	0x20	0x24

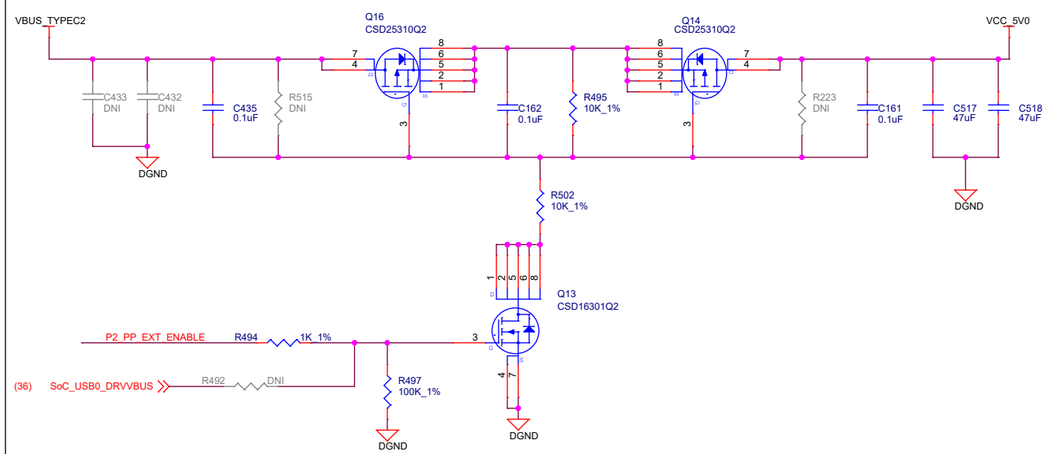
BP_NoWait
Safe Configuration



SPI EEPROM & PROGRAMMING HEADER



EXTERNAL POWER PATH FOR SOURCING, 5V/0.5A



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Title	USB TYPE-C POWER		
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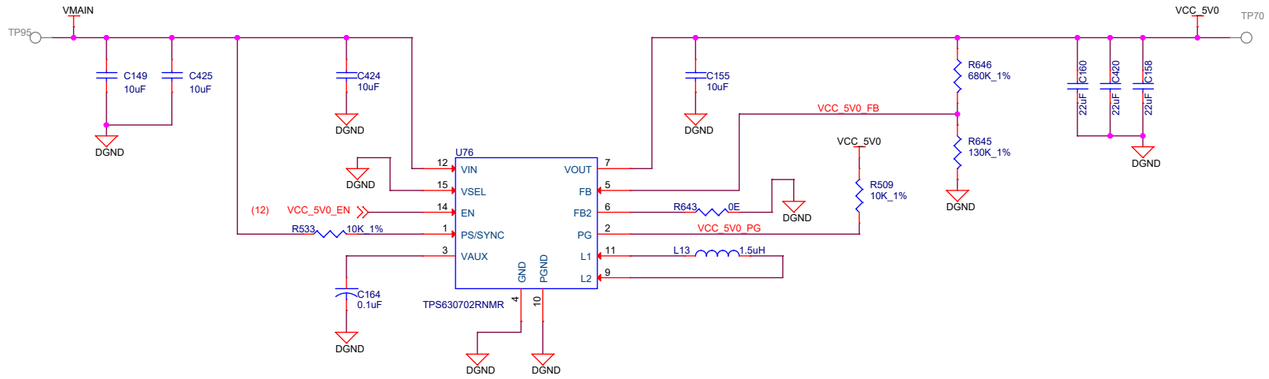
PERIPHERAL POWER SUPPLY-1



GROUND TEST POINTS

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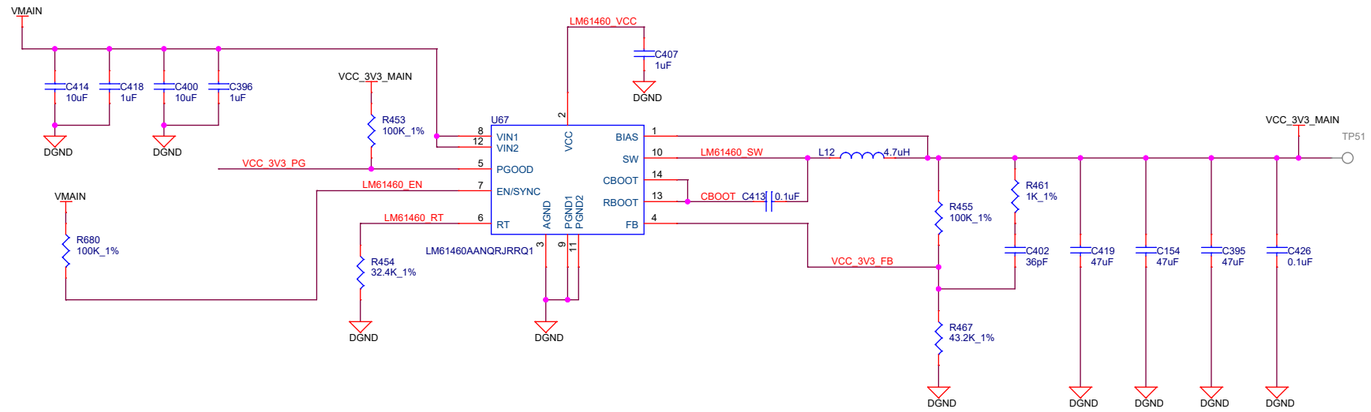
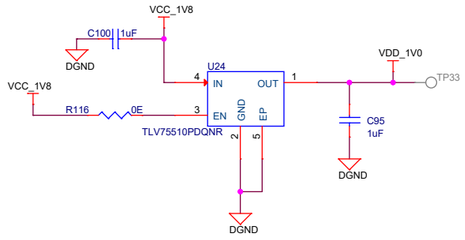
PERIPHERAL POWER SUPPLY-2

3.3V, 6.0AMPS SUPPLY

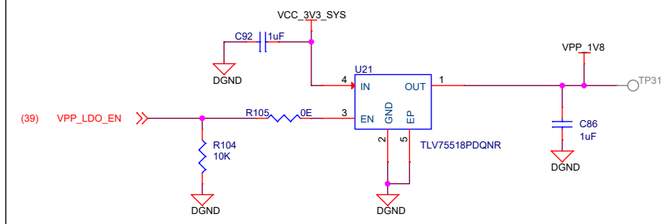
VinMin = 4.5V
VinMax = 24V
Vout = 3.3V @ 6A



1.0V, 0.5AMPS SUPPLY (ETHERNET)



1.8V VPP, 0.5AMPS SUPPLY



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Title	PERIPHERAL POWER SUPPLY-2	
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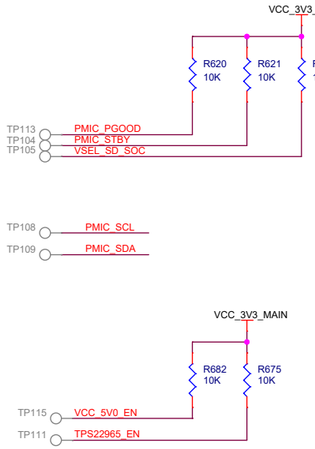
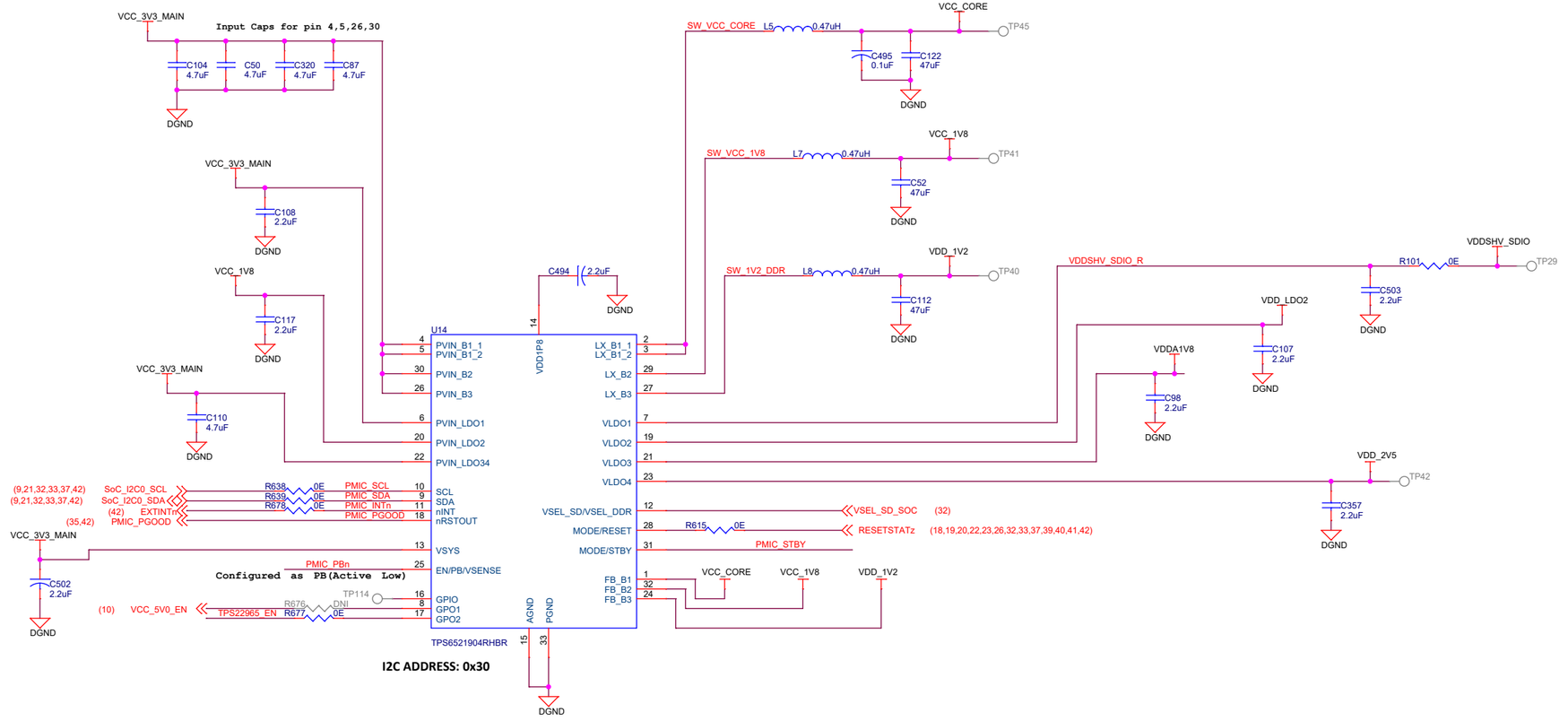
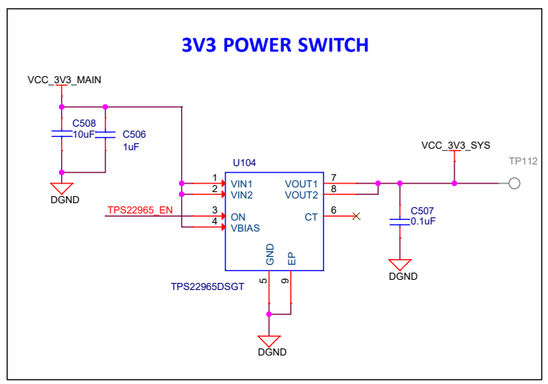
FULTON PMIC

PMIC REGULATORS	VOLTAGE RAIL	CURRENT(mA)
BUCK 1	VCC_CORE(0.85V)	2700
BUCK 2	VCC_1V8	995
BUCK 3	VDD_1V2	936
LDO 1	VDDSHV_SDIO	50
LDO 2	VDD_LDO2	150
LDO 3	VDDA1V8	200
LDO 4	VDD_2V5	300

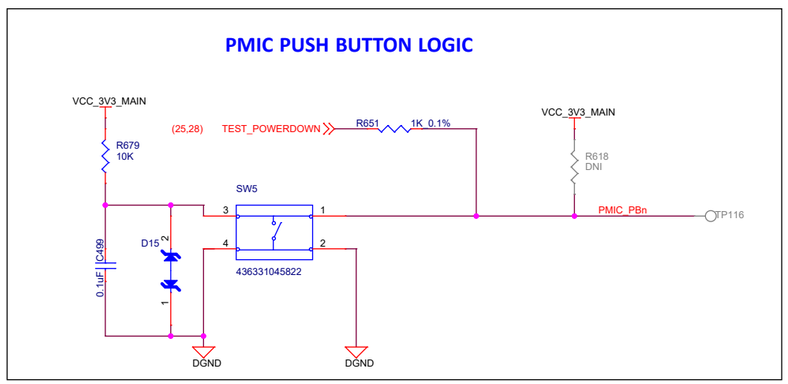




3V3 POWER SWITCH



PMIC PUSH BUTTON LOGIC



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Title	SOC POWER SUPPLY	
Size C	PROC142A1(002)	Rev A1
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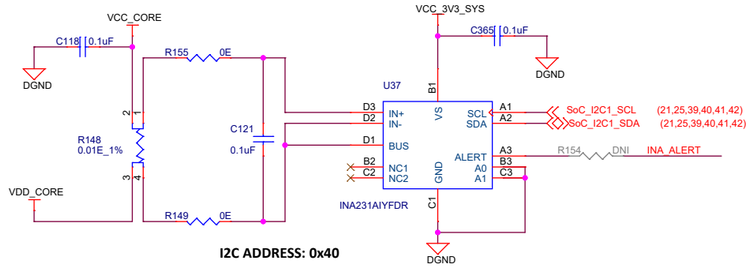
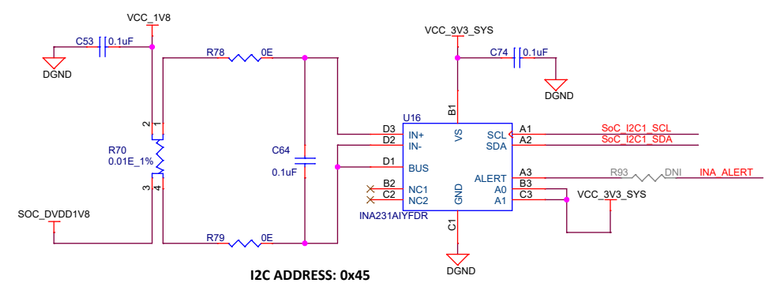
CURRENT MONITORING DEVICES

VDD_CORE



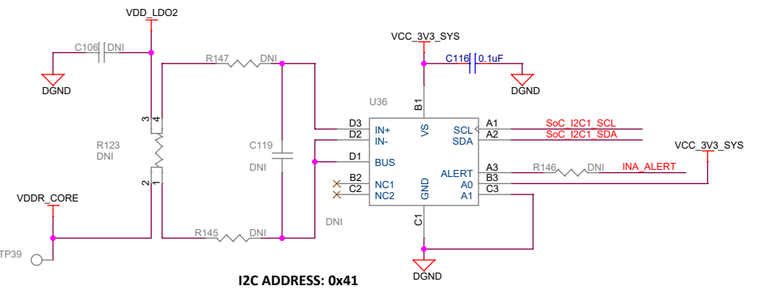
I2C ADDRESS: 0x40

SoC_DVDD1V8



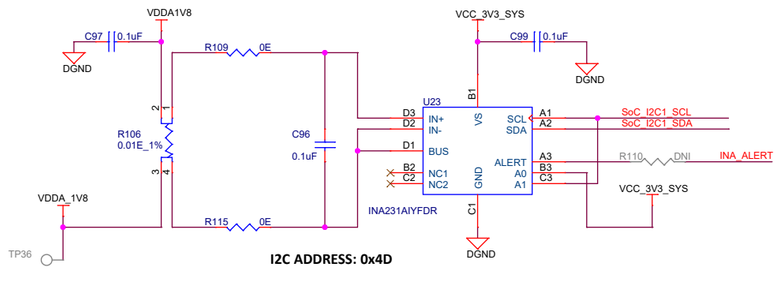
I2C ADDRESS: 0x45

VDDR_CORE



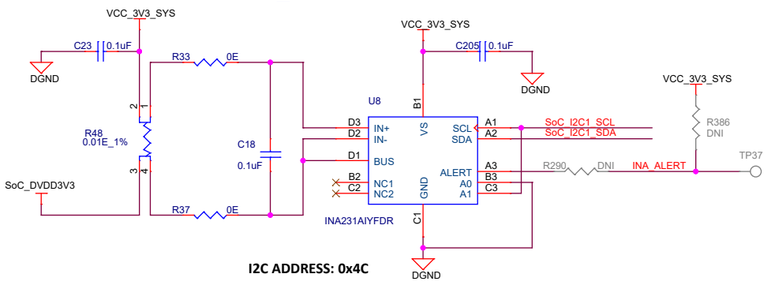
I2C ADDRESS: 0x41

VDDA_1V8



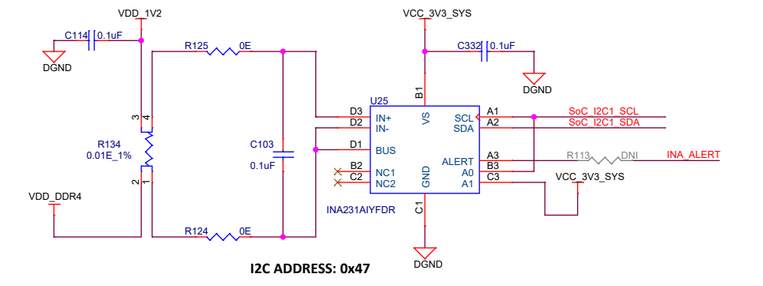
I2C ADDRESS: 0x4D

SoC_DVDD3V3



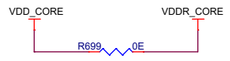
I2C ADDRESS: 0x4C

VDD_DDR4



I2C ADDRESS: 0x47

RES Option to short VDD_CORE and VDDR_CORE rails when both are 0.85V(Both should be generated from the same source)



CORE SUPPLY	ARRAY CORE SUPPLY	Assembly
0.75 VDD_CORE	0.85 VDDR_CORE	DNI R699 and Mount R123
0.85 VDD_CORE	0.85 VDDR_CORE	DNI R123 and Mount R699

INA I2C SLAVE ADDRESS

POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC_1V8	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4D
VCC1V2_DDR	VDD_DDR4	47

Designed for TI by Mistral Solutions Pvt Ltd

TEXAS INSTRUMENTS

MISTRAL

Title	CURRENT MONITORING DEVICES	
Size C	PROC142A1(002)	Rev A1
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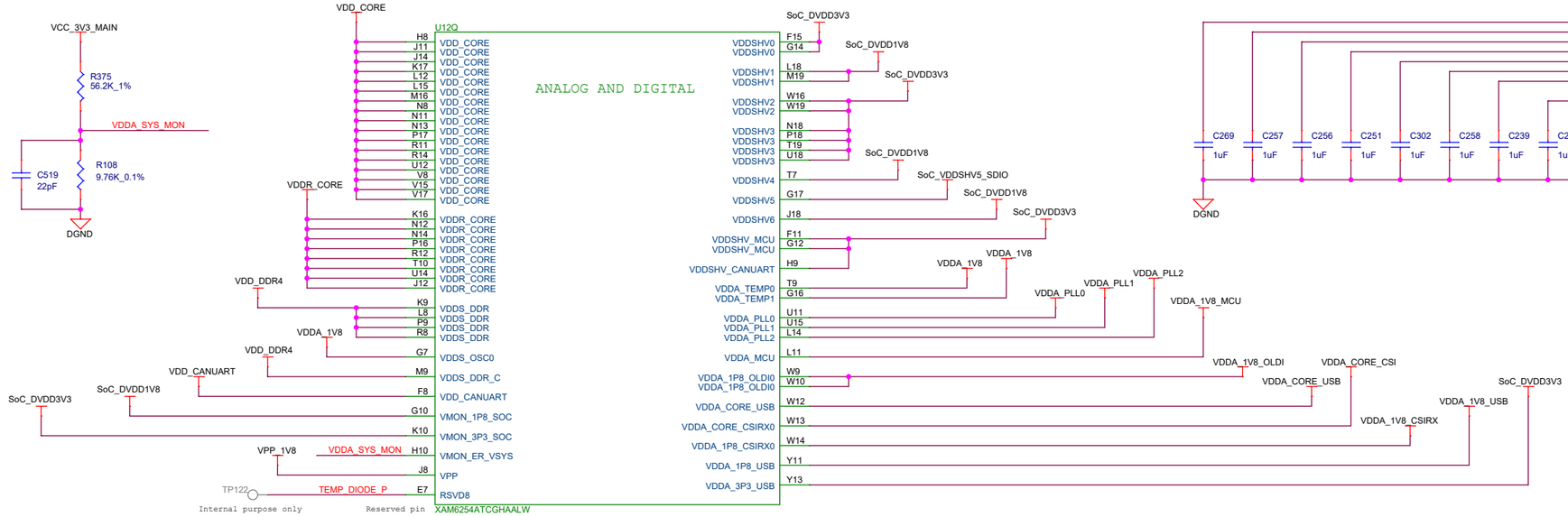
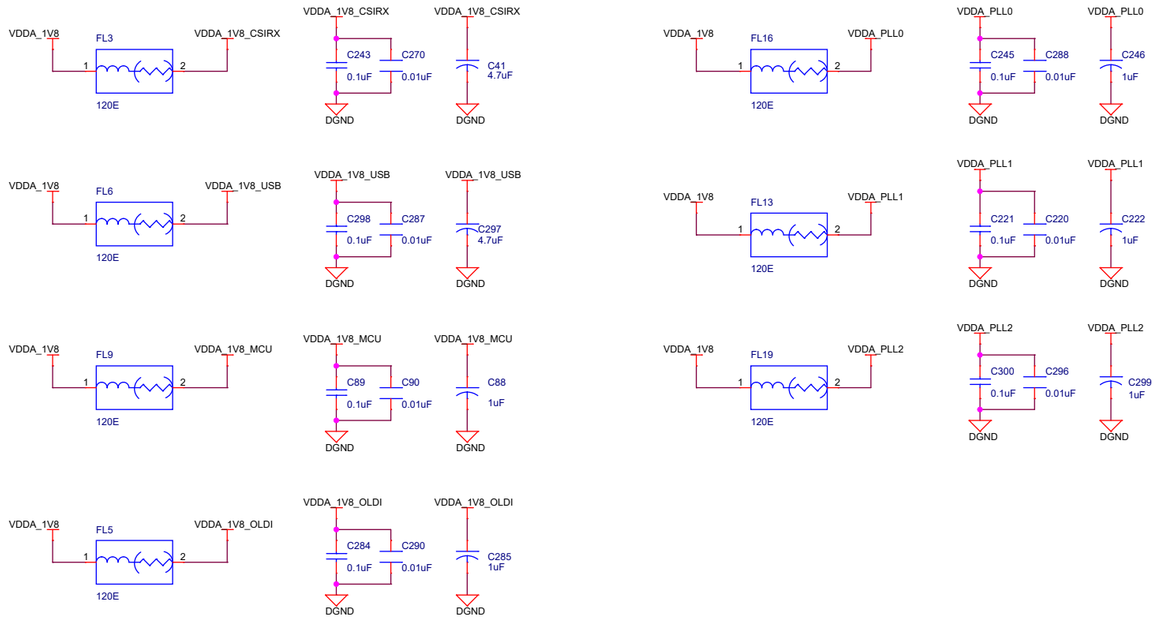
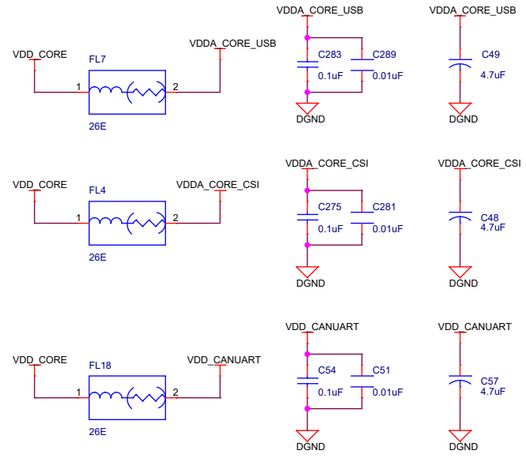
SOC POWER



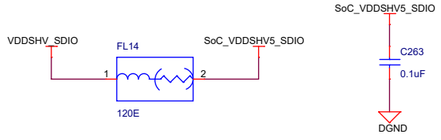
1.8V Analog SUPPLY



CORE SUPPLY



3.3V/1.8V MMC1 SUPPLY



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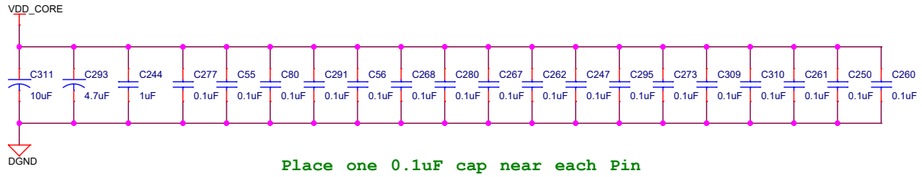
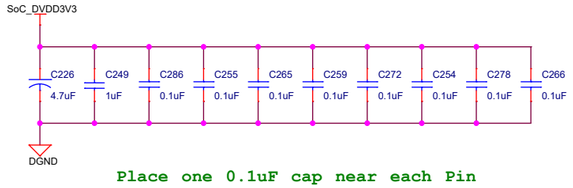
Title	SOC POWER	
Size: C	Variant Name = PROC142A1(002)	Rev: A1
Date: Tuesday, April 11, 2023	Sheet 14 of 44	

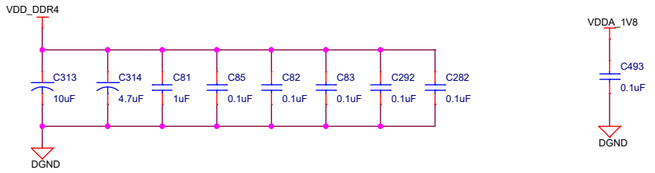
SOC POWER DECAPS



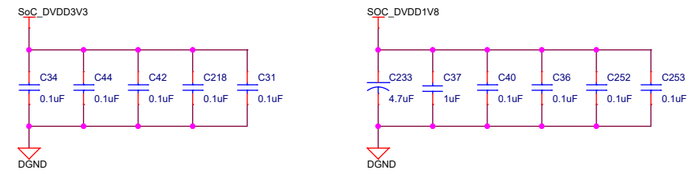
Place one 0.1uF cap near each Pin



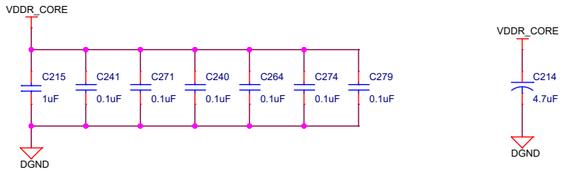
Place one 0.1uF cap near each Pin



Place one 0.1uF cap near each Pin

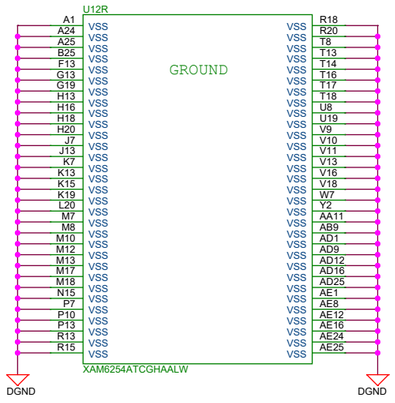


Place one 0.1uF cap near each Pin



Place one 0.1uF cap near each Pin

SOC VSS



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Title	SOC POWER CAPS & SOC VSS	
Size C	Variant Name = PROC142A1(002)	Rev
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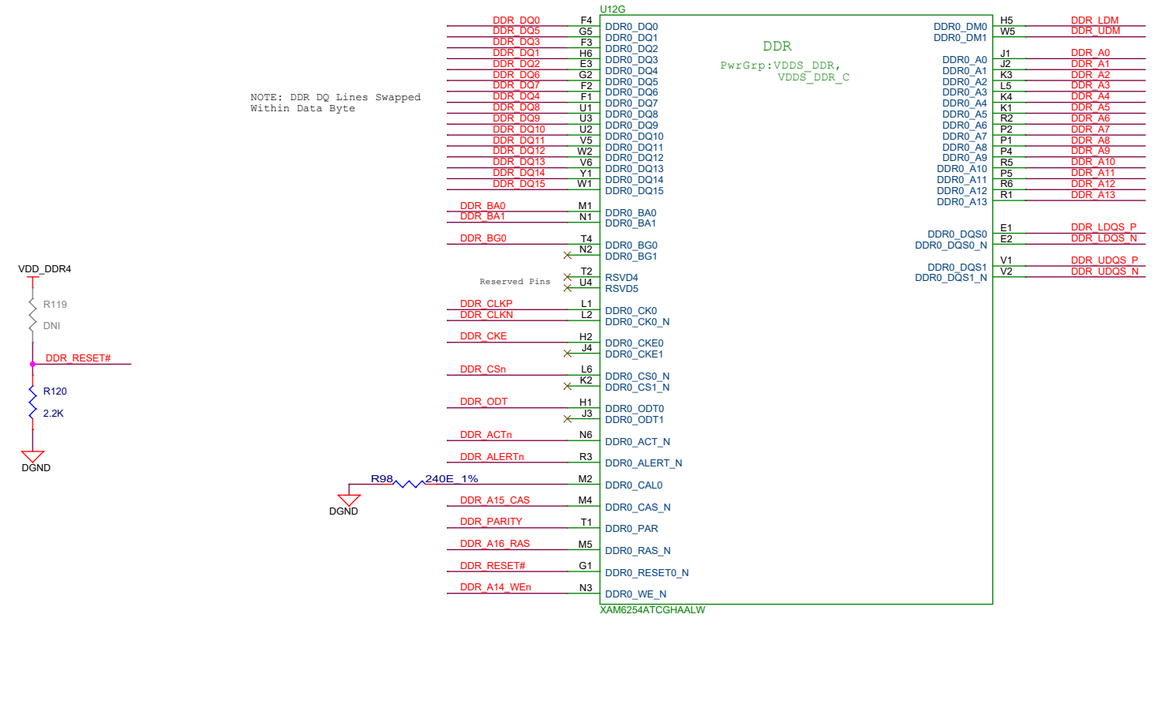
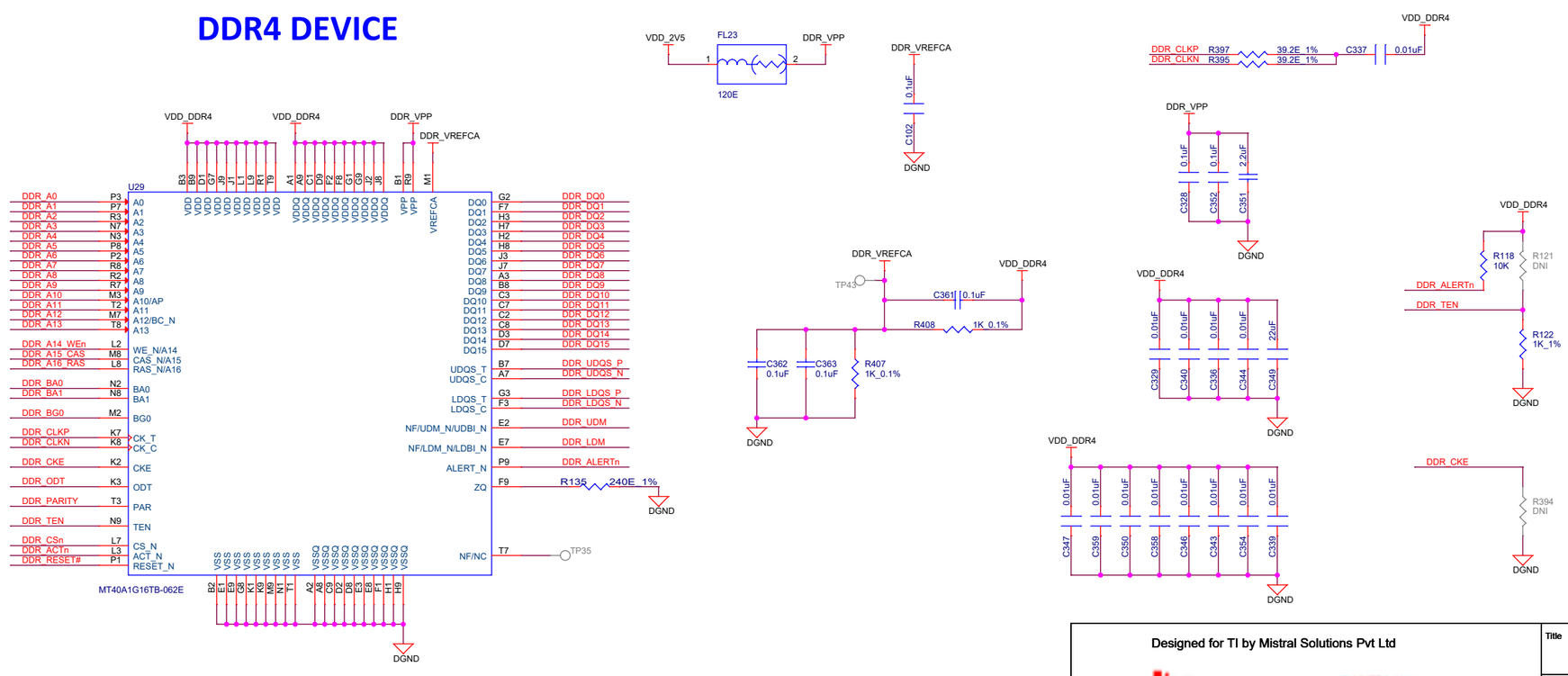
SOC DDR INTERFACE



DDR4 DEVICE



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Title	DDR4 Interface	
Size	Variant Name = PROC142A1(002)	Rev
C		A1
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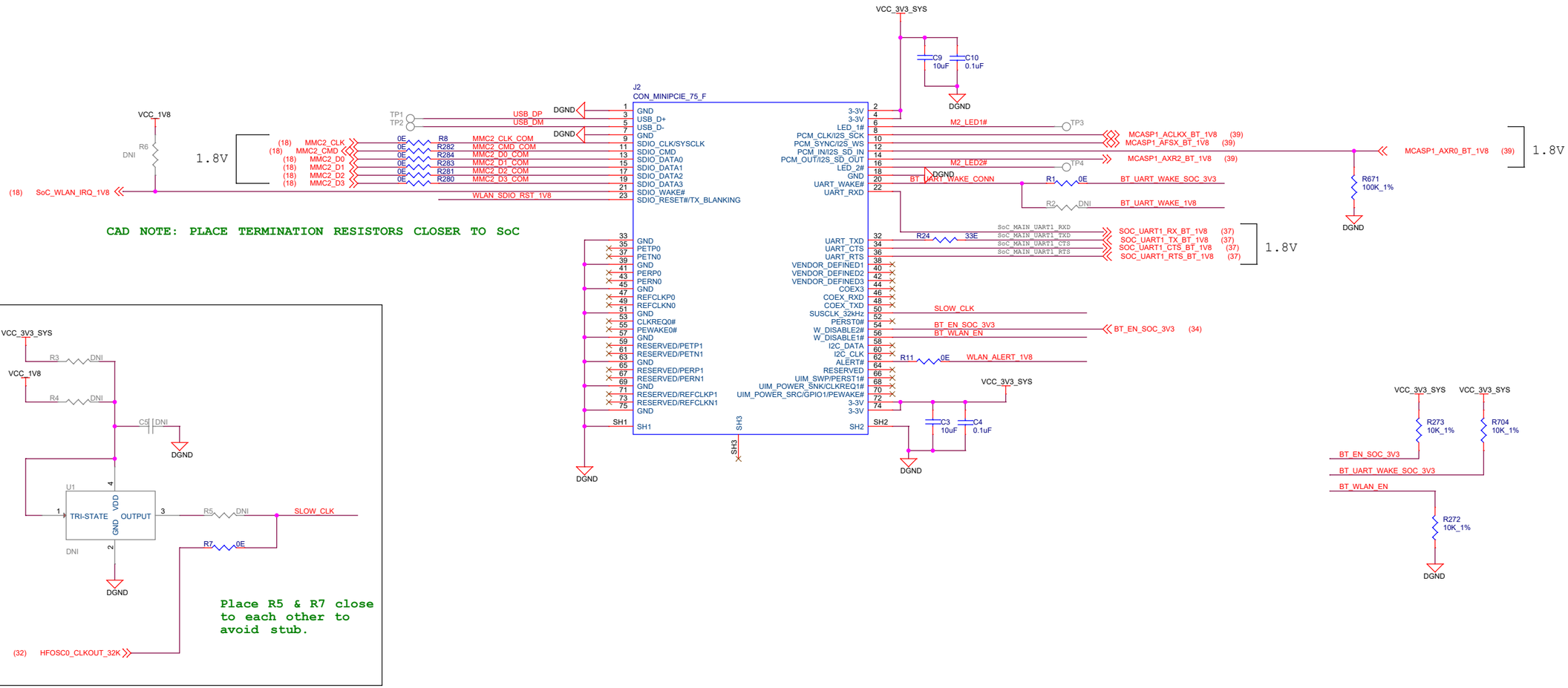
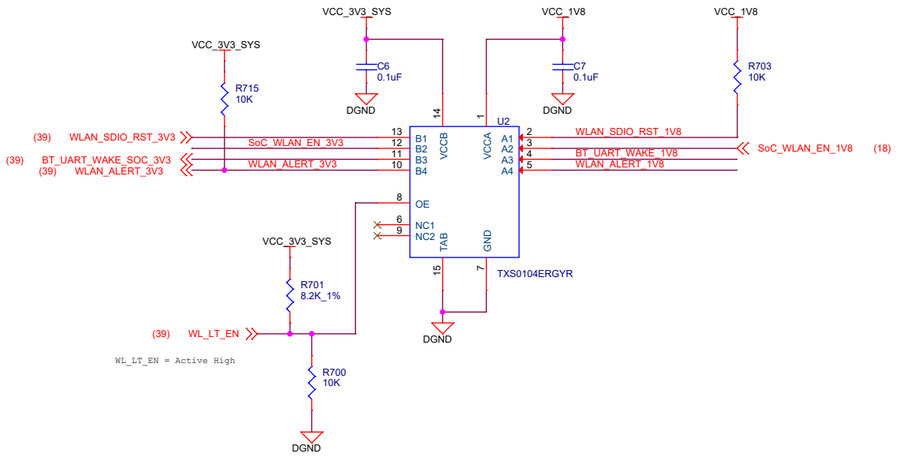
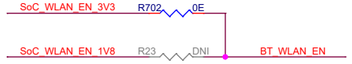
M.2 INTERFACE

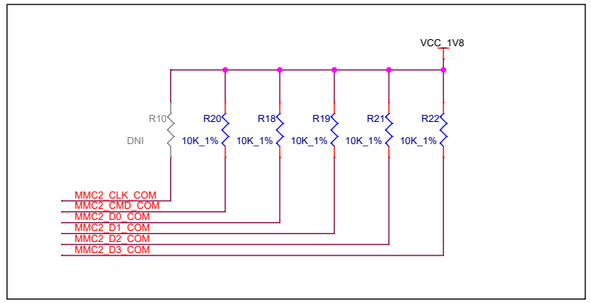


CAD NOTE: PLACE TERMINATION RESISTORS CLOSER TO SoC

Place R5 & R7 close to each other to avoid stub.







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Title	M.2 CONNECTOR	
Size C	PROC142A1(002)	Rev A1
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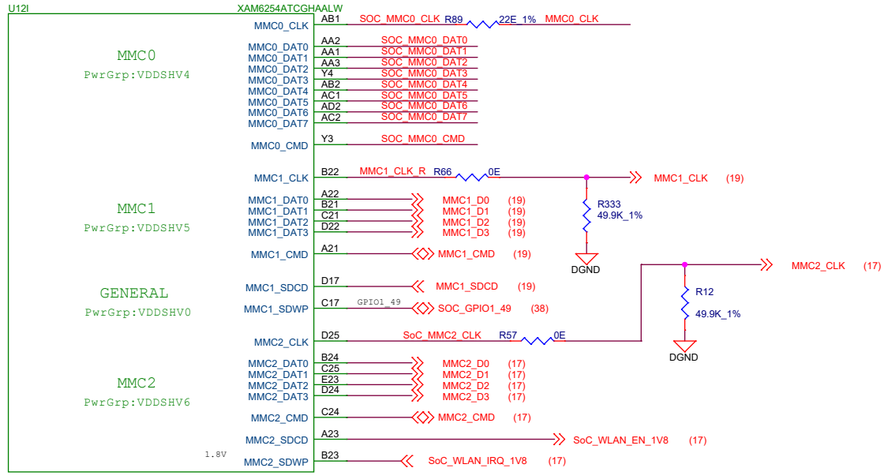
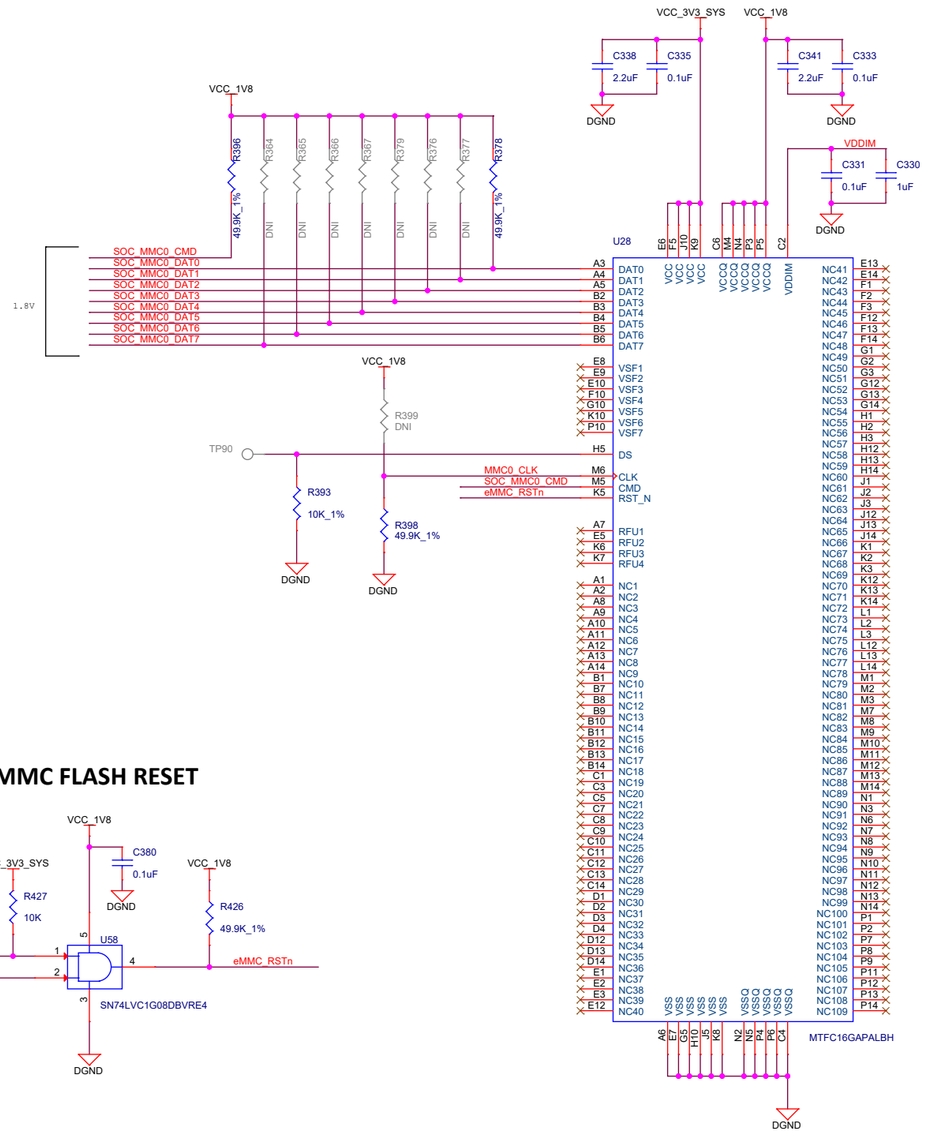
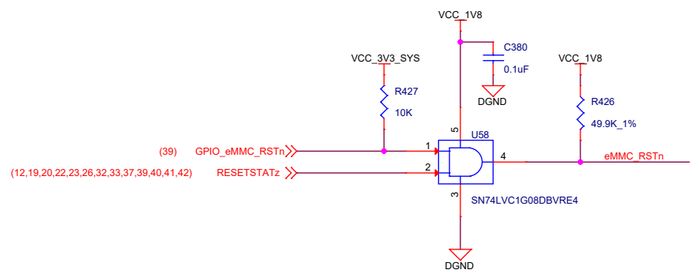
SOC - MMC Interface



eMMC FLASH



eMMC FLASH RESET



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Title	eMMC FLASH INTERFACE	
Size	PROC142A1(002)	Rev
C		A1
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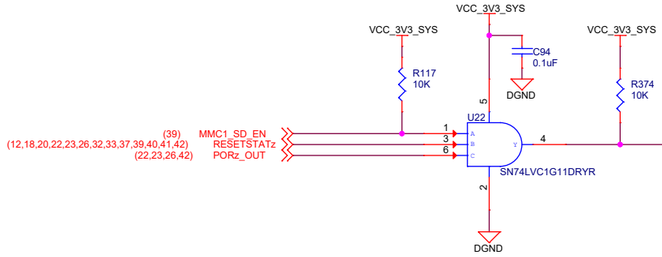
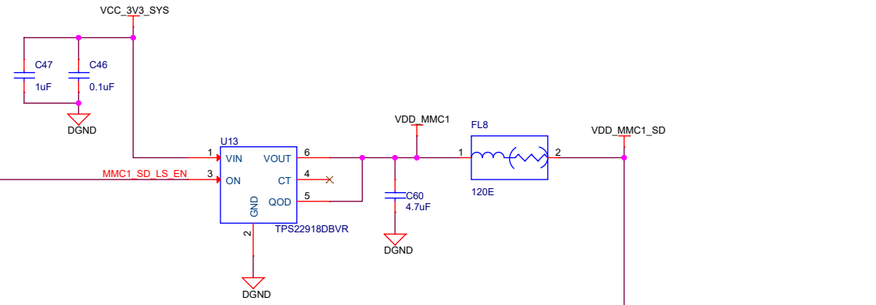
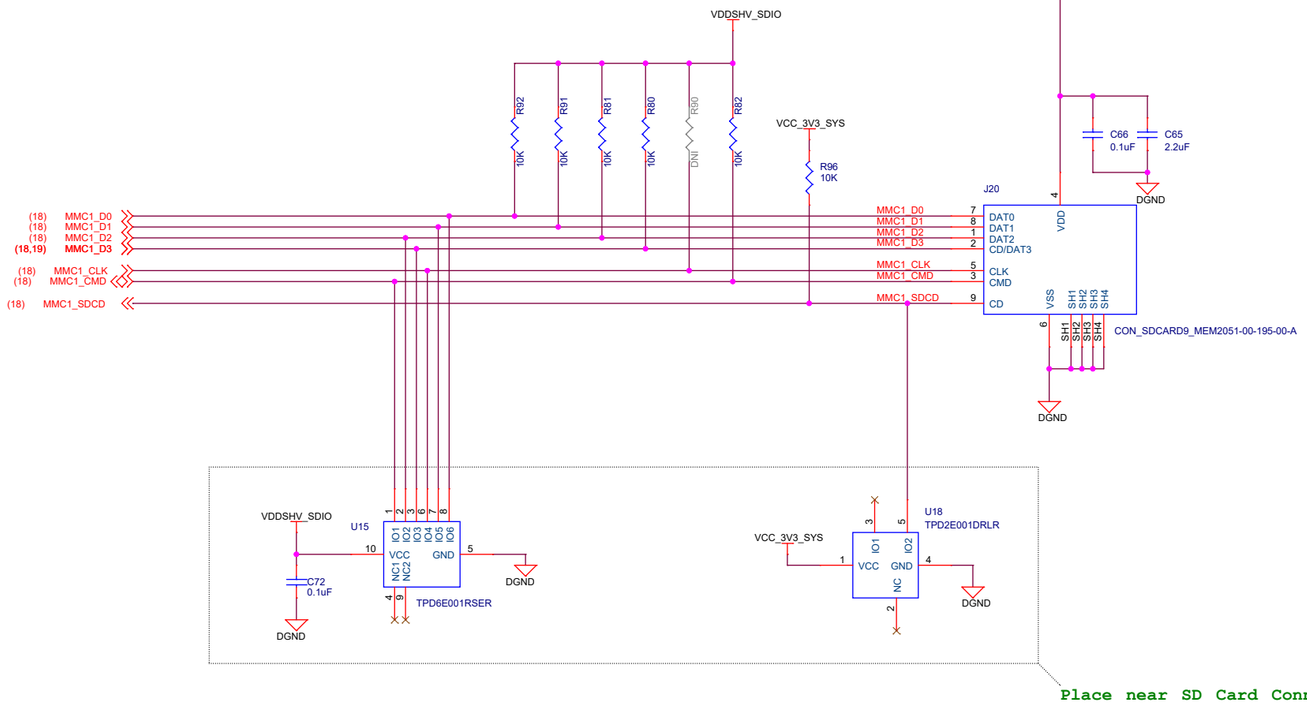
SD CARD INTERFACE

SD CARD RESET



LOAD SWITCH





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Title	SD CARD INTERFACE	
Size C	PROC142A1(002)	Rev A1
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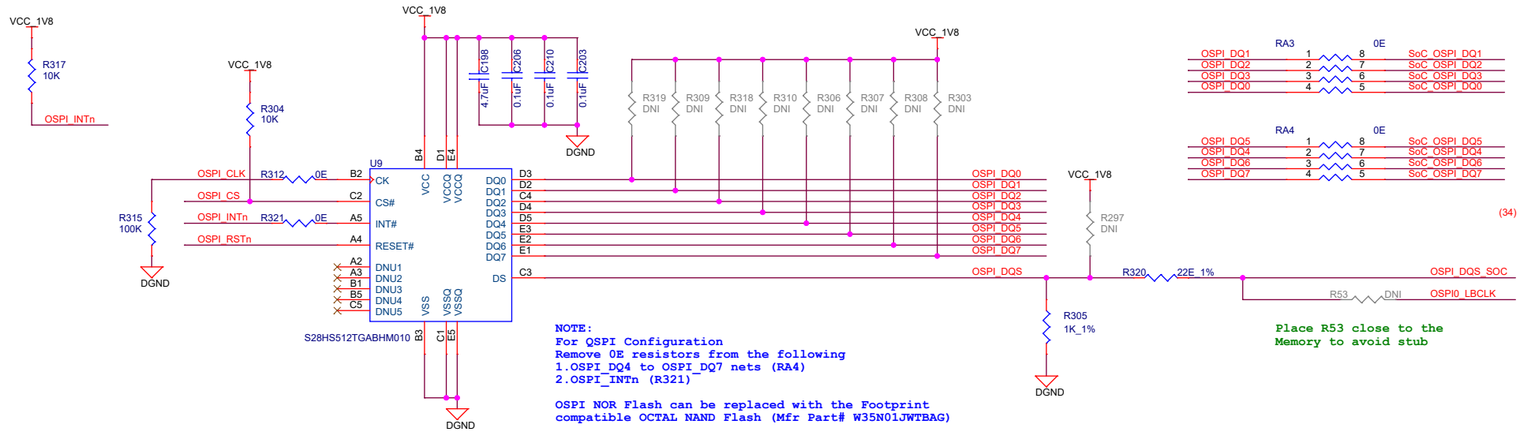
OSPI FLASH

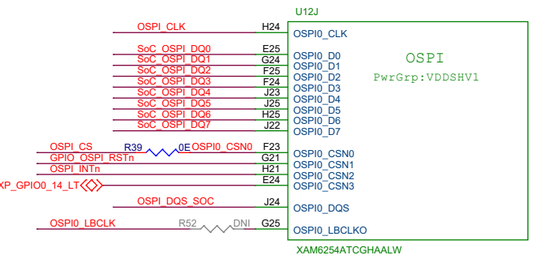


NOTE:
For QSPI Configuration
Remove 0E resistors from the following
1.OSPI_DQ4 to OSPI_DQ7 nets (RA4)
2.OSPI_INTn (R321)

OSPI NOR Flash can be replaced with the Footprint
compatible OCTAL NAND Flash (Mfr Part# W35N01JWTBAG)

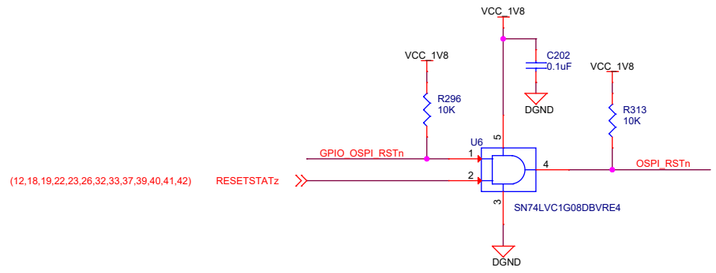
Place R53 close to the
Memory to avoid stub

SOC OSPI INTERFACE



Place R52 close to the SOC Ball
with as little trace as possible

OSPI FLASH RESET



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Title	OSPI INTERFACE	
Size: C	PROC142A1(002)	Rev: A1
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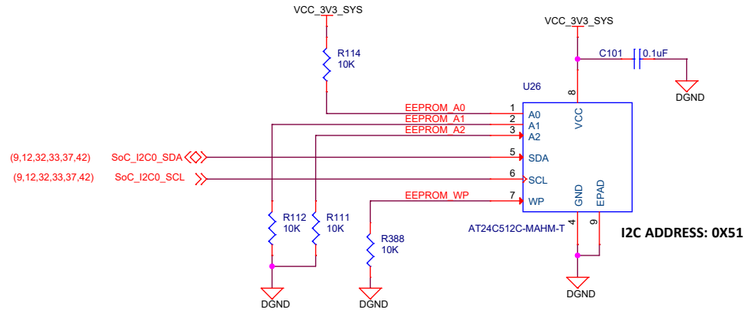
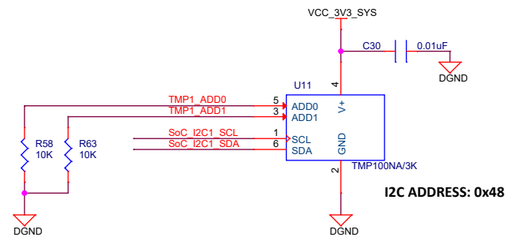
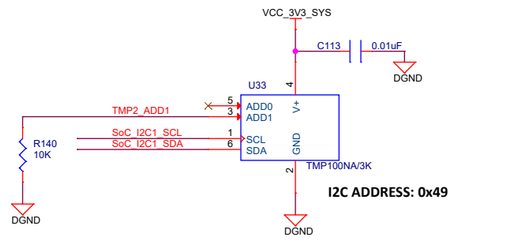
BOARD ID EEPROM



TEMPERATURE SENSORS



CAD NOTE: PLACE TEMP SENSOR U11 CLOSE TO SoC



CAD NOTE: PLACE TEMP SENSOR U33 CLOSE TO DDR4

Designed for TI by Mistral Solutions Pvt Ltd

Title	BOARD ID EEPROM & TEMPERATURE SENSORS	
Size: C	PROC142A1(002)	Rev: A1
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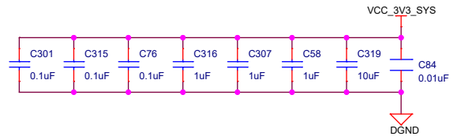
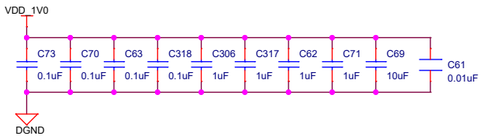
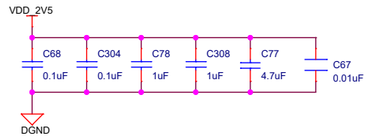
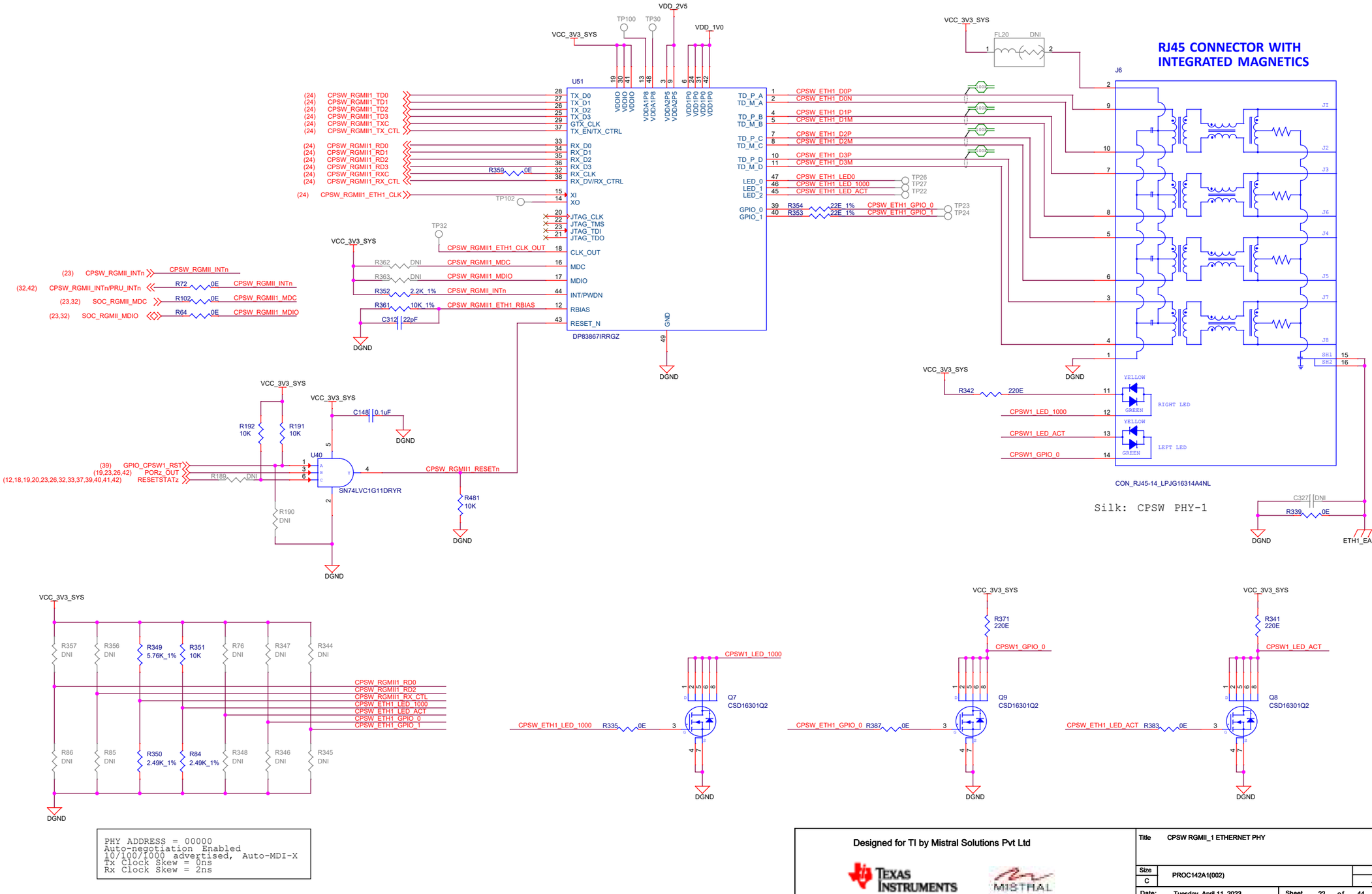
CPSW RGMII 1 - PHY









Silk: CPSW PHY-1

PHY ADDRESS = 00000
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 0ns
Rx Clock Skew = 2ns

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Title	CPSW RGMII_1 ETHERNET PHY	
Size C	PROC142A1(002)	Rev A1
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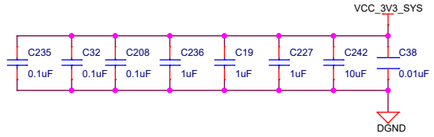
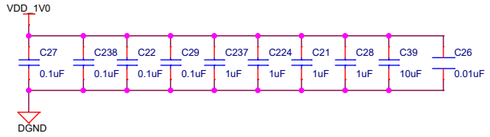
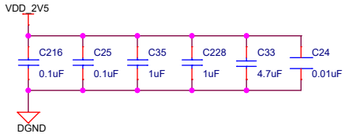
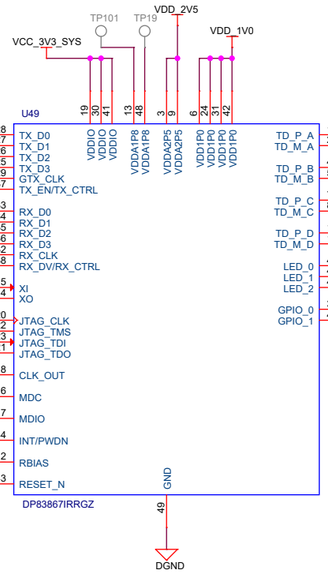
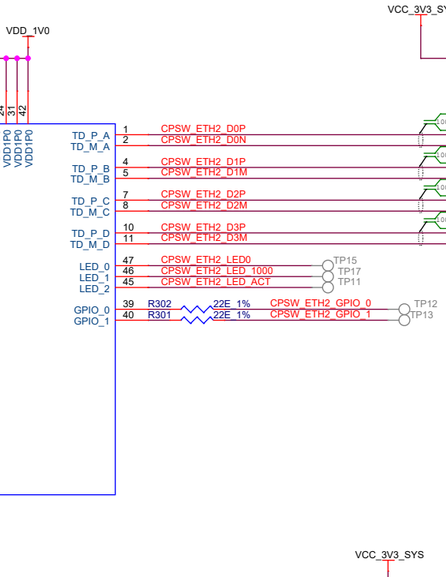
CPSW RGMII 2 - PHY

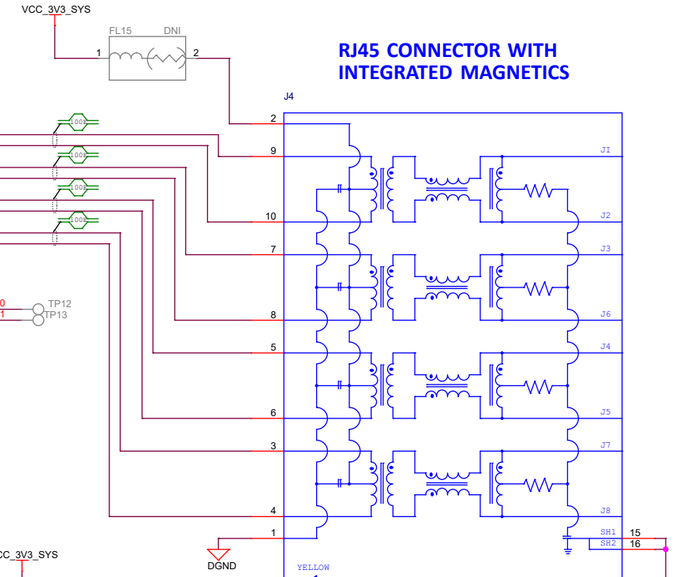


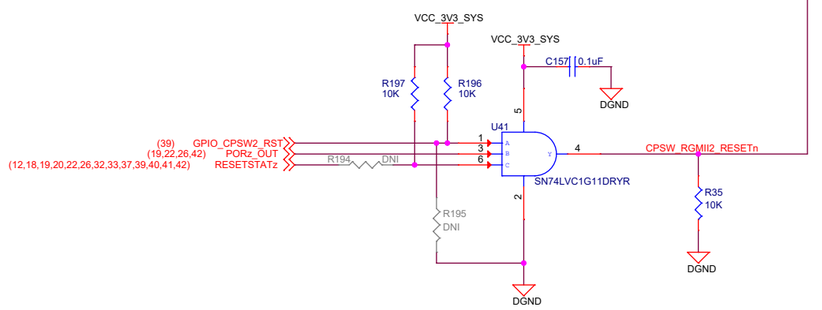


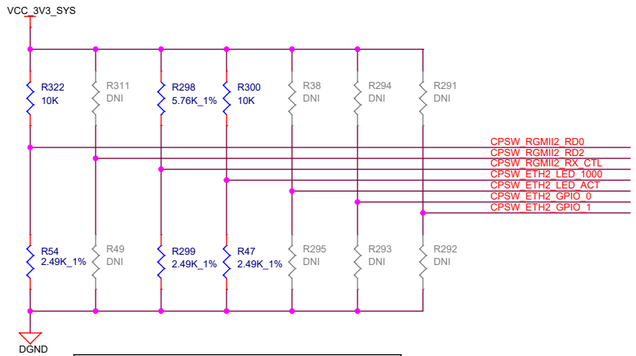


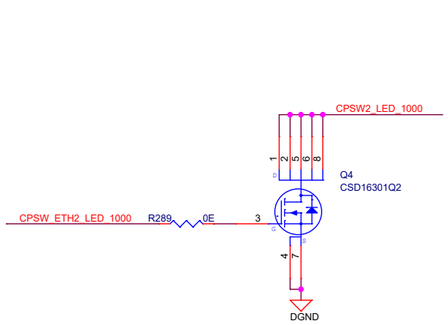


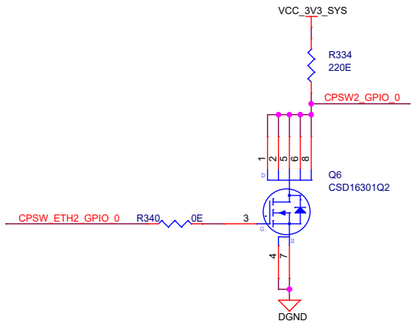


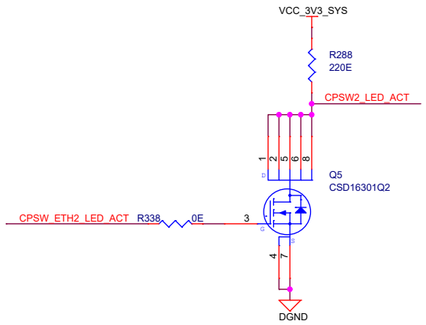













```
PHY ADDRESS = 00001
Auto-negotiation  Enabled
10/100/1000 advertised,  Auto-MDI-X
Tx Clock Skew = 0ns
Rx Clock Skew = 2ns
```

Silk: CPSW PHY-2

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Title	CPSW RGMII_2 ETHERNET PHY	
Size: C	PROC142A1(002)	Rev: A1
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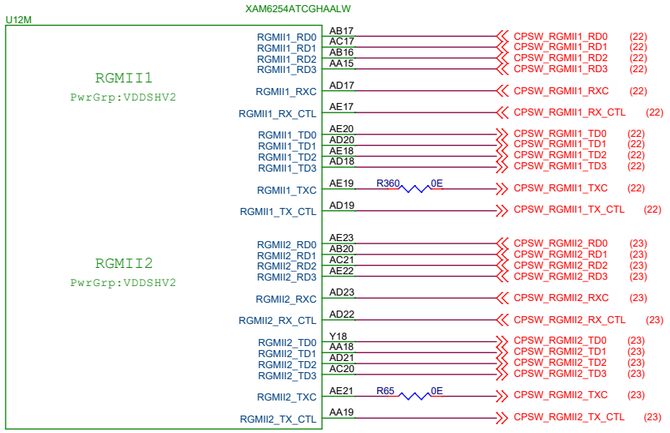
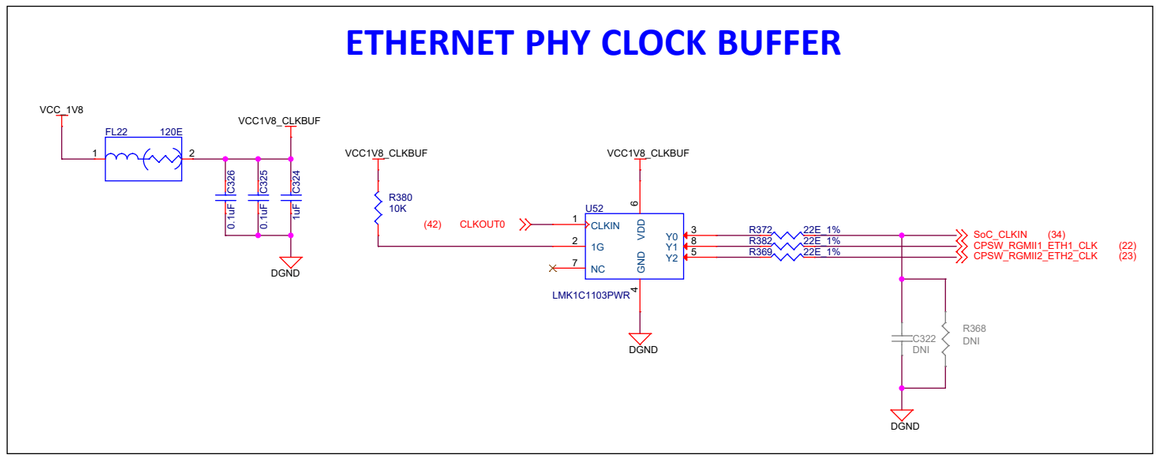
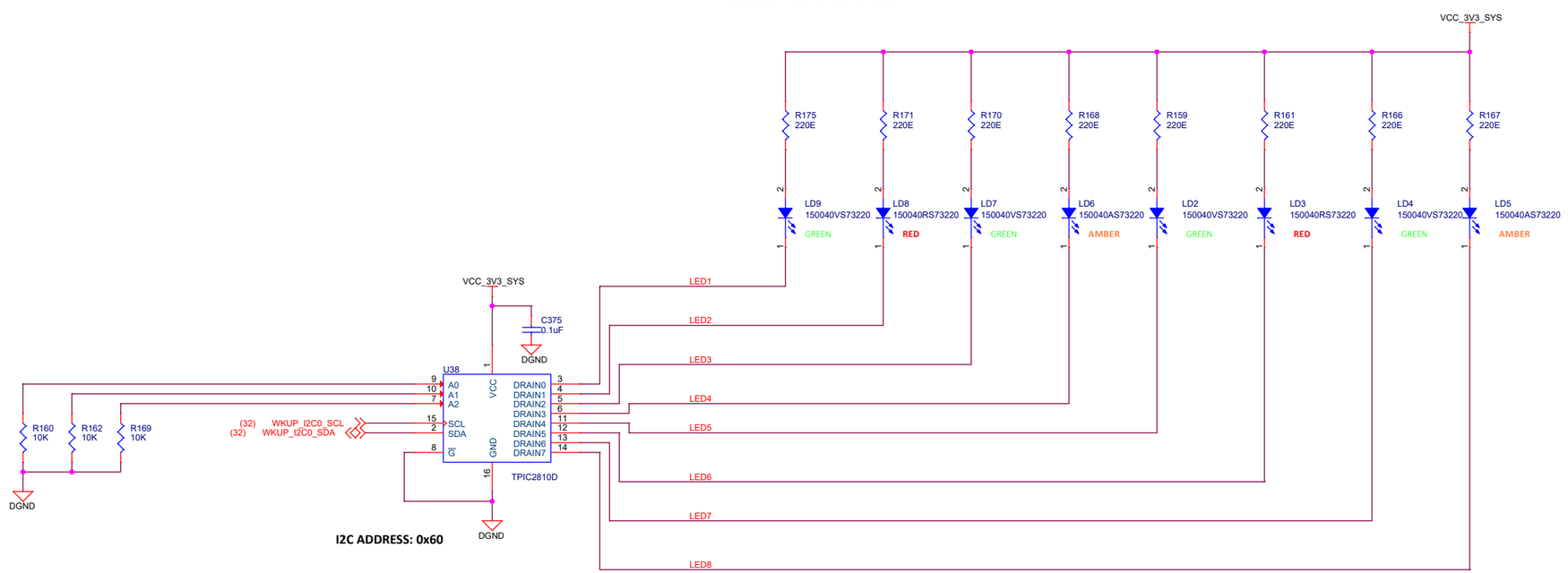


ETHERNET PHY CLOCK BUFFER



LED DRIVER



Designed for TI by Mistral Solutions Pvt Ltd

Title	ETHERNET PHY CLOCK BUFFER & LED DRIVER	
Size C	PROC142A1(002)	Rev A1
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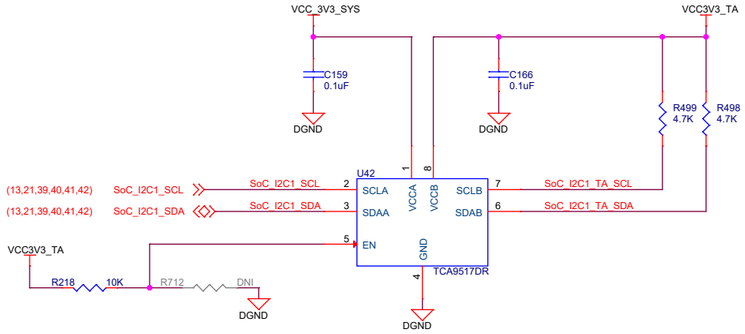
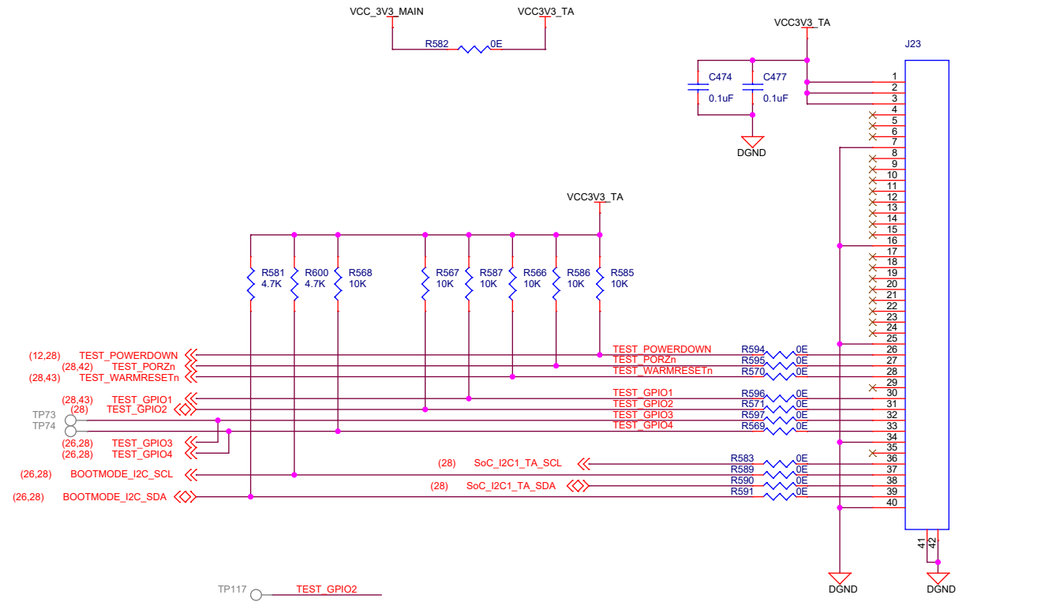
I2C BUS BUFFER



40-PIN TEST AUTOMATION HEADER



CON_FLEX_40X1_FH12A-40S-0.5SH

Silk: AUTOMATION HDR

TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the EVM	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on MCU_GPIO0_15 Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to a Testpoint	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode I2C IO Expander	OUTPUT	External Pullup

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Title	TEST AUTOMATION	
Size C	PROC142A1(002)	Rev A1
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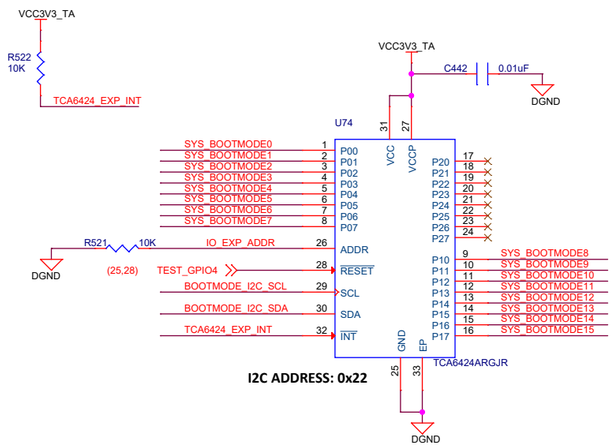
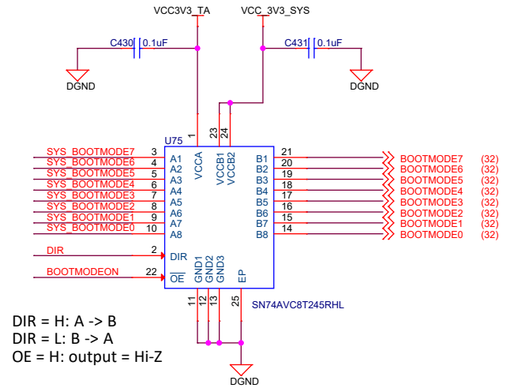
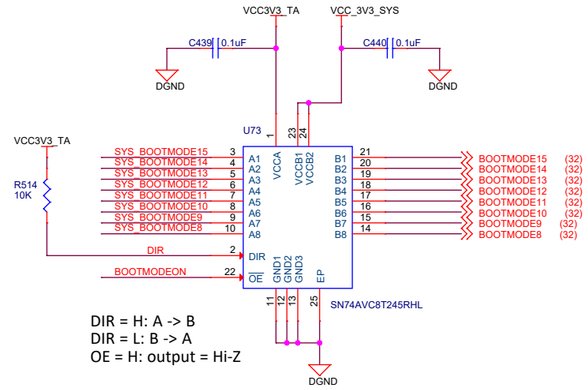
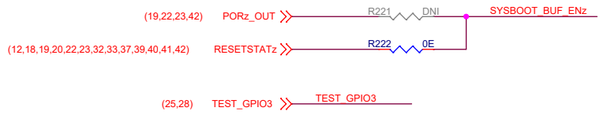
BOOTMODE IO EXPANDER

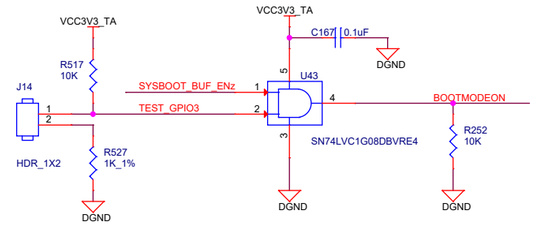


BOOT MODE BUFFERS

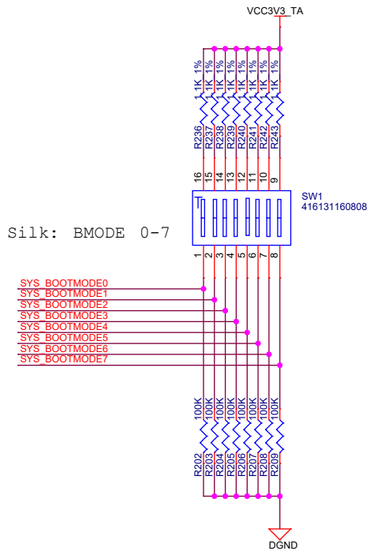




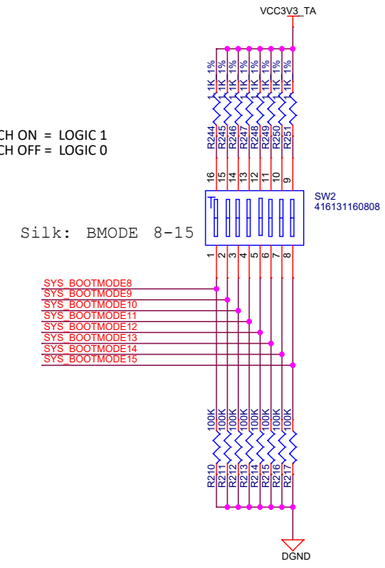




BOOT MODE SWITCHES



SWITCH ON = LOGIC 1
SWITCH OFF = LOGIC 0



BOOT MODES SUPPORTED

1. OSPI
2. MMC1 - SD CARD
3. UART
4. eMMC
5. BACKUP BOOT OPTION

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Title	BOOT MODE BUFFER & SWITCHES	
Size C	PROC142A1(002)	Rev A1
Date: Tuesday, April 11, 2023	Sheet 26 of 44	

XDS110 DEBUGGER

TP86
XDS_USB_VBUS
C180 4.7uF
D8 TPD1E10B06DPYR
DGND
C455 2.2uF
R540 0E
U79
IN1 IN2 EN GND PAD OUT1 OUT2 NR/FB NC
TPS79601DRBR
R520 51K
C441 15pF
R519 30K
C443 1uF
VCC3V3_XDS
TP77
U45B
C454 1uF
C468 0.1uF
C173 0.1uF
C181 0.01uF
C176 0.01uF
C191 0.01uF
VDD
GNDA GND
TM4C1294NCPDTT3R
C192 1uF
C189 0.01uF
VDDA VDDC
VDDC_1V2
C179 2.2uF
C178 1uF
C449 0.1uF
VBAT
R228 49.9E_1%
C169 0.1uF

Silk: JTAG

J16
VBUS D- D+ ID GND SH1 SH2 SH3 SH4
CON_MUSB-B_5_F
XDS_USB_DM
XDS_USB_DP
XDS_USB_ID
U89
IO1 IO2 IO3 IO4 VCC GND
TPD4E004DRYR
R256 0E
C185 DNI
XDS_SHIELD

U45A
PA0/U0RX PA1/U0TX PA2/SSI0CLK PA3/SSI0FSS PA4/SSI0XDAT0 PA5/SSI0XDAT1 PA6 PA7
PC0/TCK/SWCLK PC1/TMS/SWDIO PC2/TDI PC3/TDO/SWO PC4/C1- PC5/C1+ PC6/C0+ PC7/C0-
PE0/AIN3 PE1/AIN2 PE2/AIN1 PE3/AIN0 PE4/AIN9 PE5/AIN8
PG0 PG1
PJ0 PJ1
PL0 PL1 PL2 PL3 PL4 PL5 PL6/USB0DP PL7/USB0DM
PN0 PN1 PN2 PN3 PN4 PN5
PQ0 PQ1 PQ2 PQ3 PQ4
TM4C1294NCPDTT3R
PB0/USB0ID PB1/USB0VBUS PB2/I2C0SCL PB3/I2C0SDA PB4/AIN10 PB5/AIN11
PD0/AIN15 PD1/AIN14 PD2/AIN13 PD3/AIN12 PD4/AIN7 PD5/AIN6 PD6/AIN5 PD7/AIN4
PF0 PF1 PF2 PF3 PF4
PH0 PH1 PH2 PH3
PK0/AIN16 PK1/AIN17 PK2/AIN18 PK3/AIN19 PK4 PK5 PK6 PK7
PM0 PM1 PM2 PM3 PM4 PM5 PM6 PM7
PP0/C2+ PP1/C2- PP2 PP3 PP4 PP5

(29) XDS110_TCK
(29) XDS110_TMS
(29) XDS110_TDO
(29) XDS110_TDI
(29) XDS110_TRST#
TP82 TP81 TP80 TP79 TM4C129_TCK TM4C129_TMS TM4C129_TDI TM4C129_TDO
(28) BOOTMODE_XDS_I2C_SCL
(28) BOOTMODE_XDS_I2C_SDA
(28) SoC_I2C1_XDS_SDA
(28) SoC_I2C1_XDS_SCL
XDS_USB_DP
XDS_USB_DM
XDS110_EMU0
XDS110_EMU1
TEST_POWERDOWN_XDS (28)
TEST_PORZn_XDS (28)
TEST_WARMRESETn_XDS (28)
TP76
TEST_GPIO1_XDS (28)
TEST_GPIO2_XDS (28)
TEST_GPIO3_XDS (28)
TEST_GPIO4_XDS (28)

R530 100E_1%
R235 DNI
C170 0.1uF
XDS_USB_ID
XDS_USB_VBUS
R268 30K
R269 20K_1%
R267 220E
R271 220E
LD14 150080VS75000 GREEN
LD15 150040RS73220 RED

VCC3V3_XDS
R563 1K_1%
R560 1K_1%
R556 1K_1%
R552 1K_1%
R260 DNI
R259 DNI
R258 DNI
R255 DNI

Sets the unique ID of the Debugger

VCC3V3_XDS
R539 10K
TP75
R546 DNI
XDS_RSTn
U45C
RST WAKE OSC0 OSC1 XOSC0 XOSC1 RBAIS VREFA+ HIB EN0RXIP EN0RXIN EN0RX0P EN0RX0N
TM4C1294NCPDTT3R
R261 4.87K_1%
C172 12pF
C171 12pF
Y2 16.000MHz
R270 4.7K
XDS_VREF
C186 0.01uF
C190 0.1uF
U47
LM4040B25IDCKR

R264 4.7K
R265 4.7K

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Title	XDS110 DEBUGGER	
Size	PROC142A1(002)	Rev
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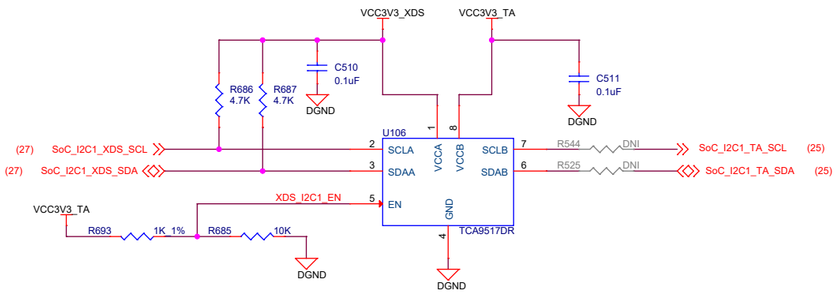
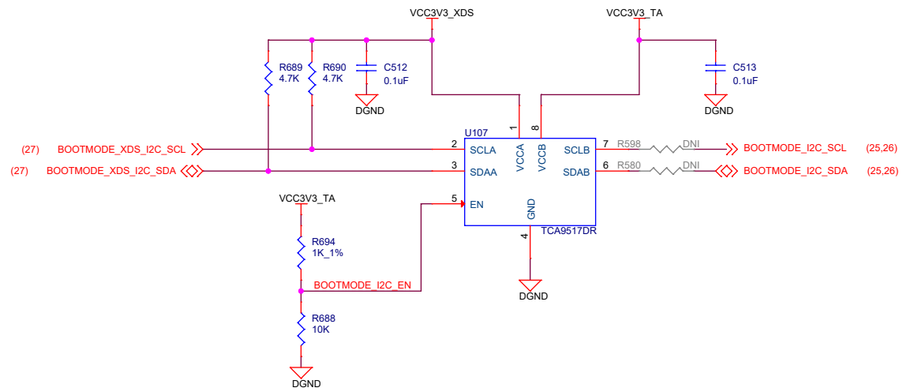
Date:	Tuesday, April 11, 2023	Sheet 27 of 44

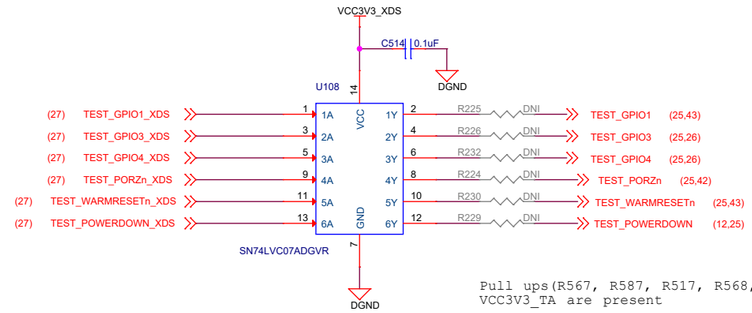
I2C_TA BUS BUFFER



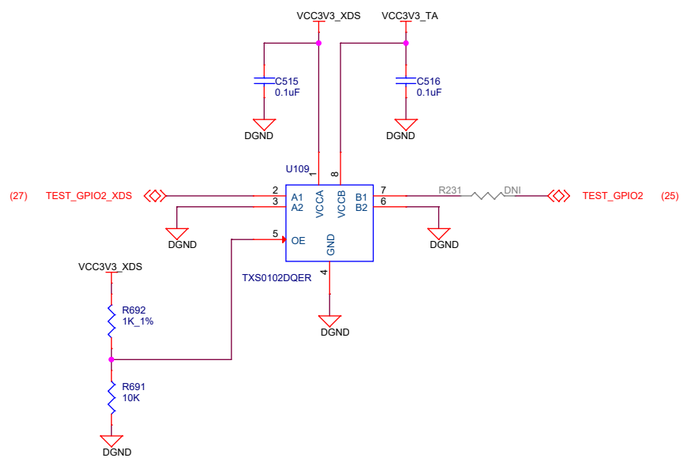
BOOTMODE_I2C_TA BUFFER



ISOLATION BUFFERS FOR TA SIGNALS



Pull ups(R567, R587, R517, R568, R585, R586 & R566) to VCC3V3_TA are present



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Title	AUTOMATION SIGNALS BUFFER	
Size C	PROC142A1(002)	Rev A1
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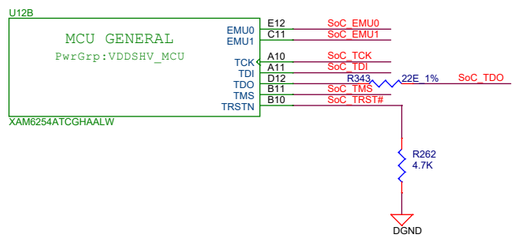
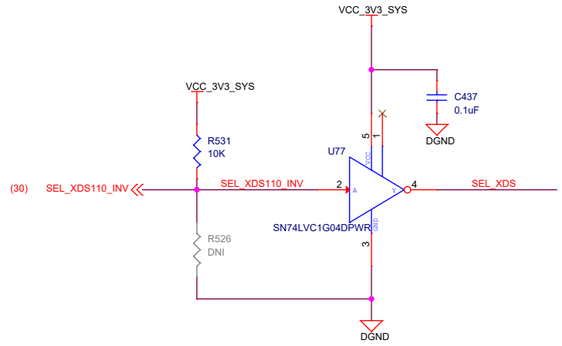
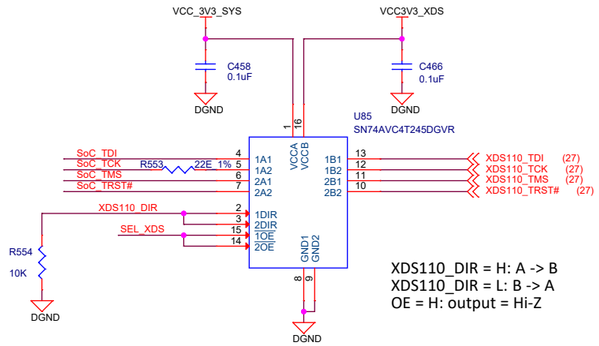
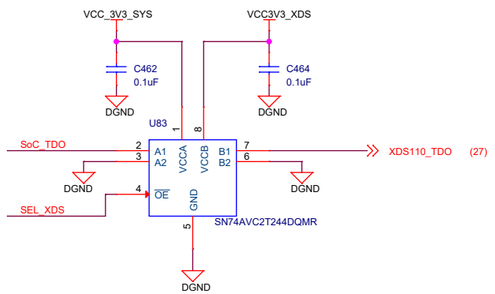
JTAG SOC SECTION

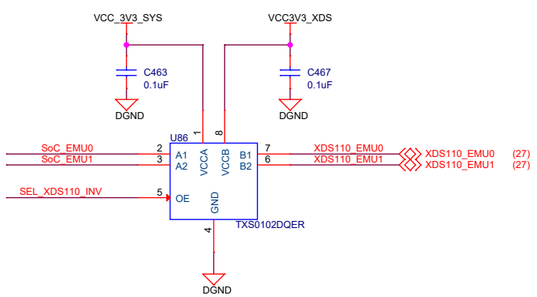




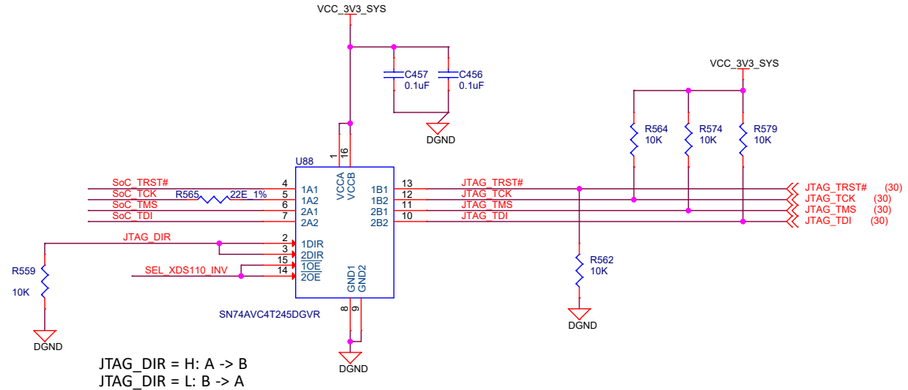
BUFFER XDS110

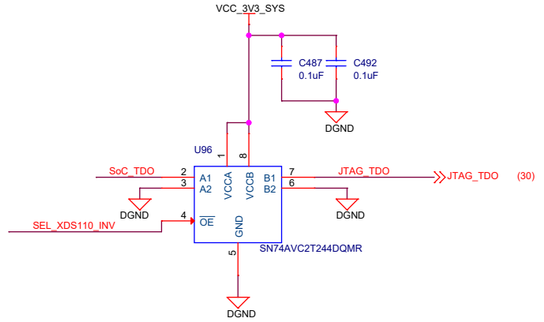




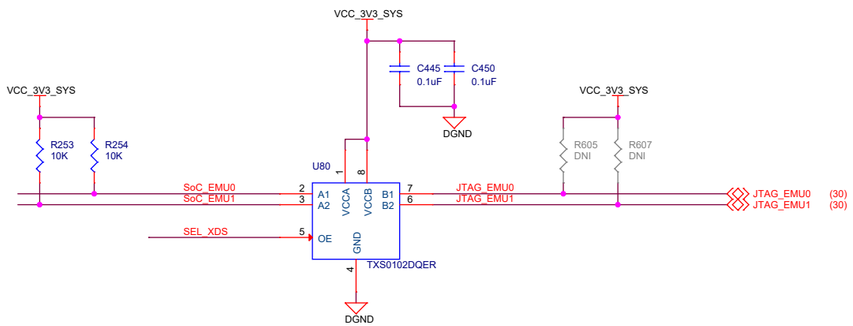


cTI20 JTAG BUFFERS





CAD NOTE: Buffers U88 and U96 need to be placed closer to the cTI-20pin connector J17 to reduce Stub length of the JTAG signals.



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Title	JTAG BUFFER	
Size: C	PROC142A1(002)	Rev: A1
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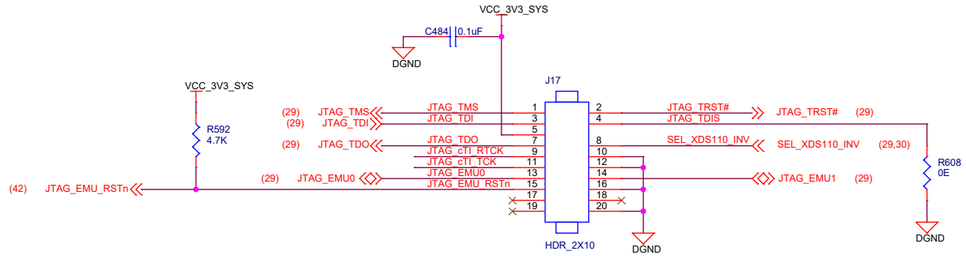
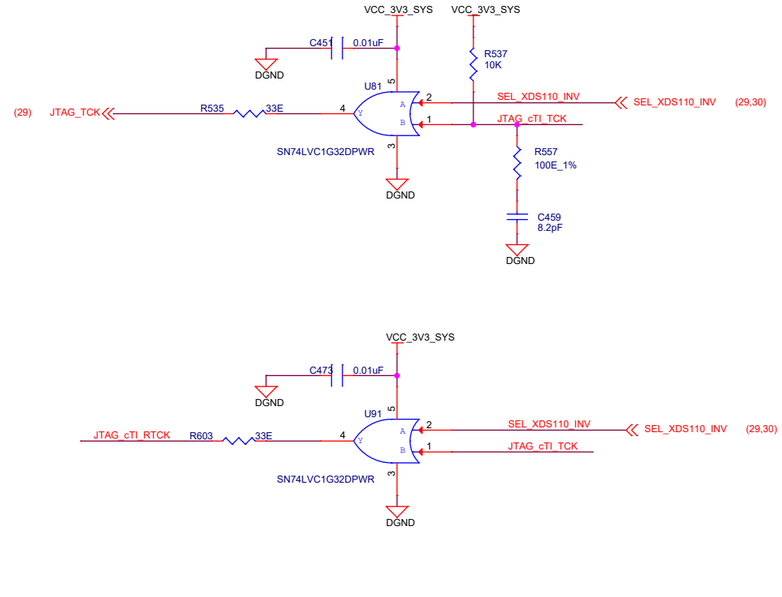
JTAG 20 PIN cTI CONNECTOR



Silk: cTI

JTAG CLOCK BUFFER



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Title	JTAG 20 PIN cTI CONNECTOR		
Size C	PROC142A1(002)		Rev A1
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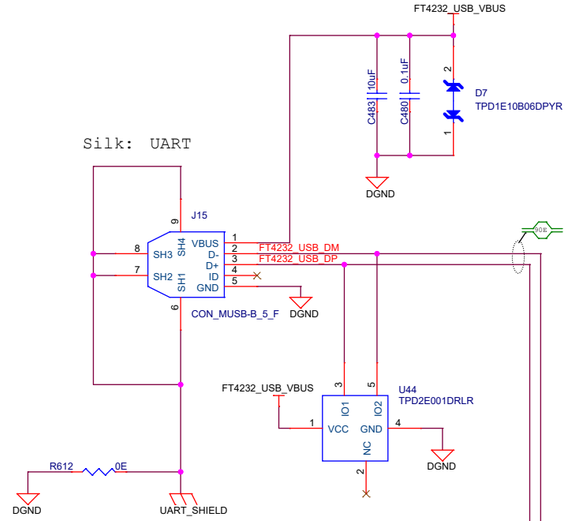
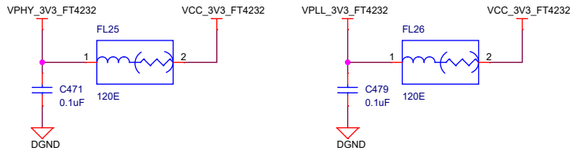
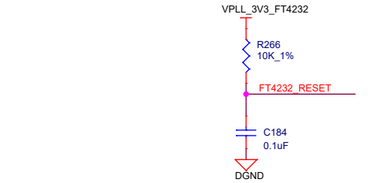
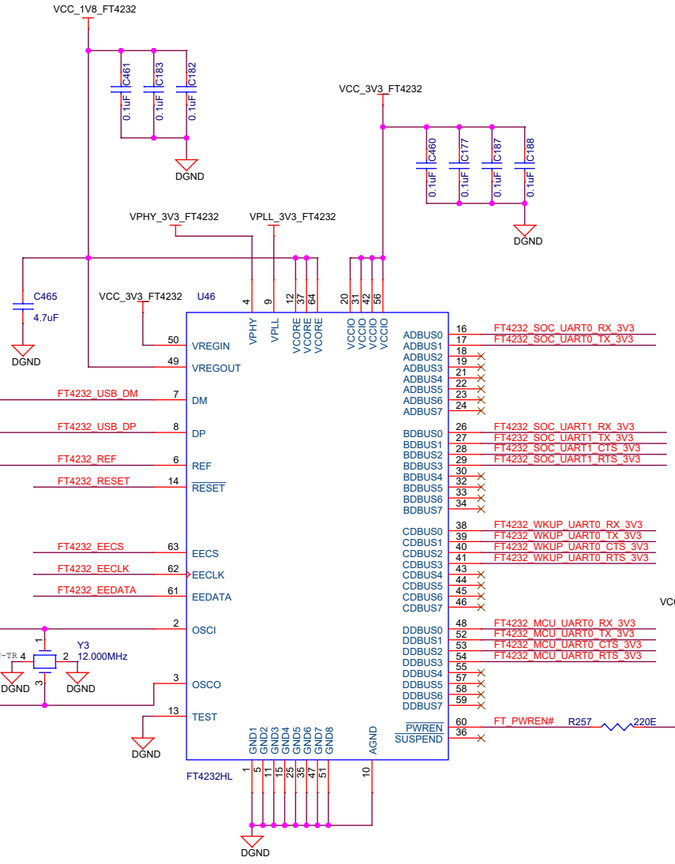
FT4232 UART

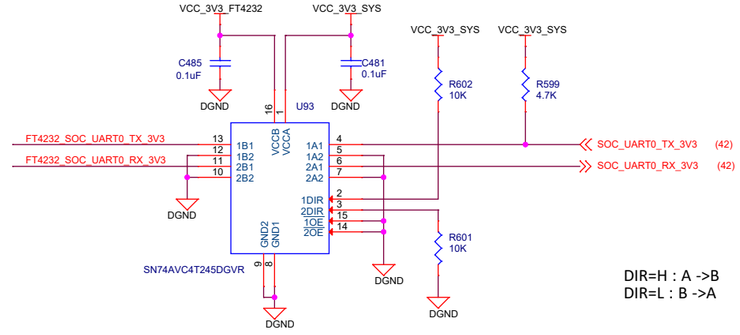
Silk: UART

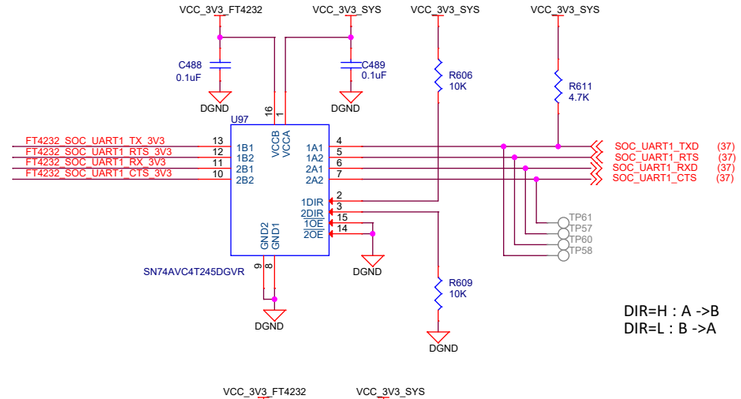


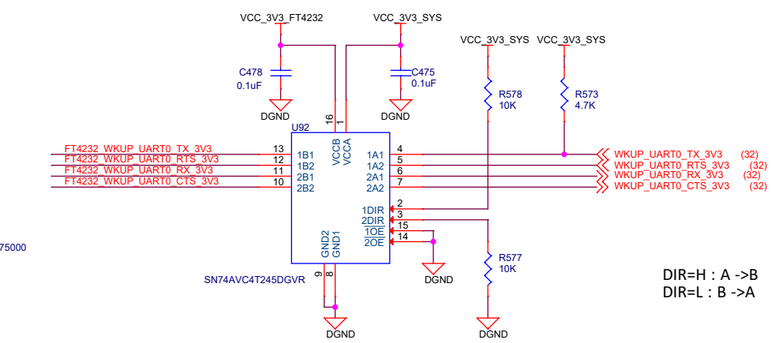


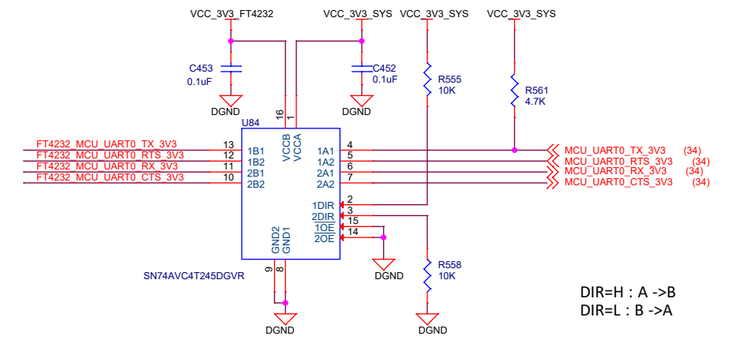




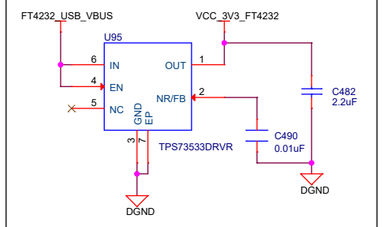




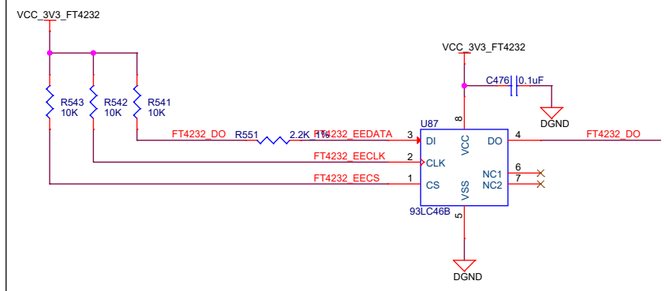




FT4232: 5V to 3.3V@500mA LDO



EEPROM



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Title	FT4232 UART TO USB BRIDGE	
Size: C	PROC142A1(002)	Rev: A1
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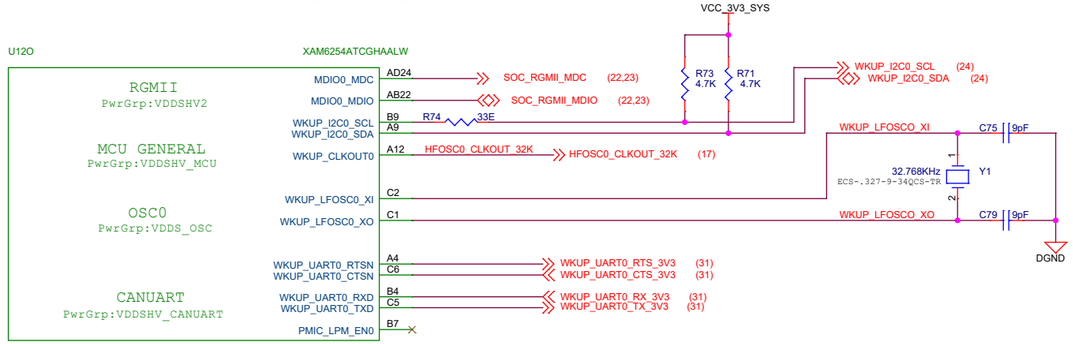
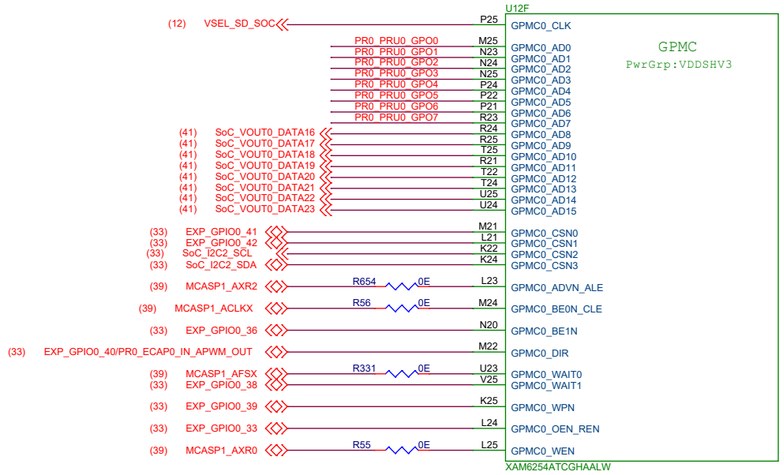
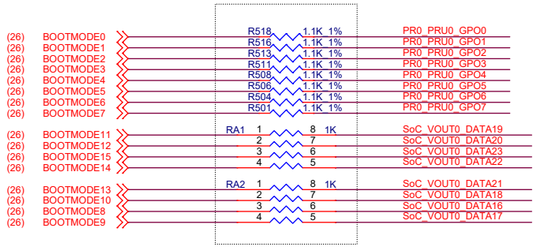
SOC WKUP DOMAIN



SOC GPMC

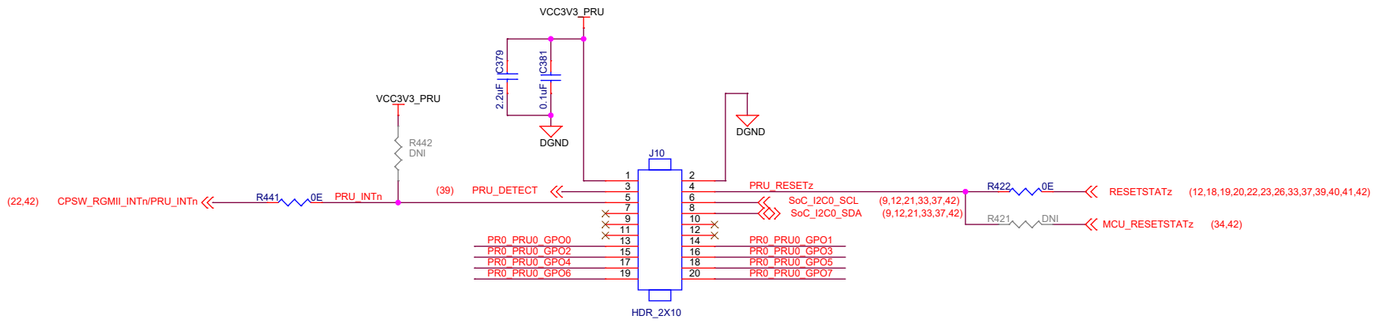


BOOTMODE PINS



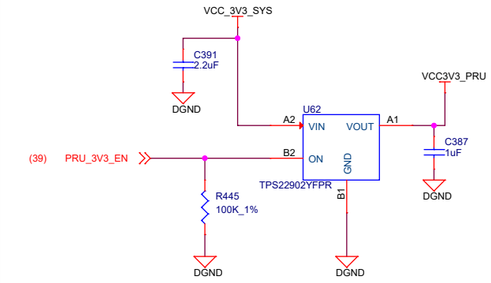
NOTE: Resistors are used to isolate the BOOTMODE control logic after the value is latched

PRU HEADER



Silk: PRU HDR

POWER SWITCH FOR PRU HEADER



3V3 supply of PRU Header is limited to sourcing 500mA max.

NOTE: PRU Header I/O are not fail-safe and shall not be driven when AM62x Starter Kit is not powered.

Designed for TI by Mistral Solutions Pvt Ltd

Title	PRU HEADER	
Size C	PROC142A1(002)	Rev A1
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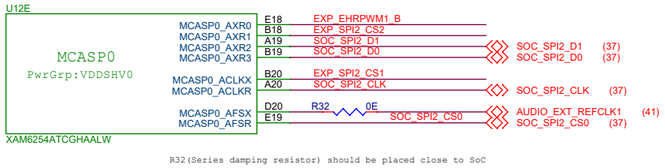
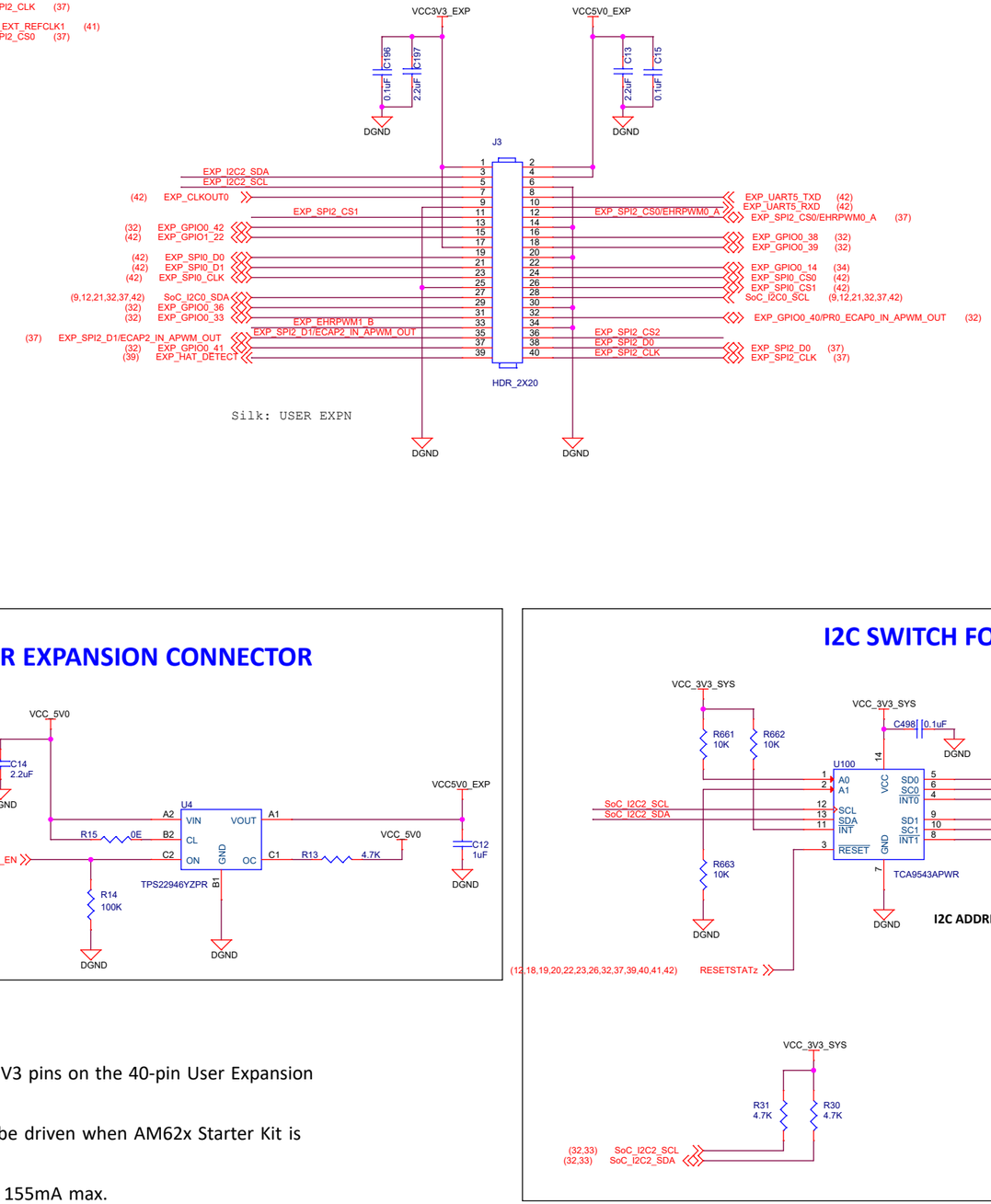
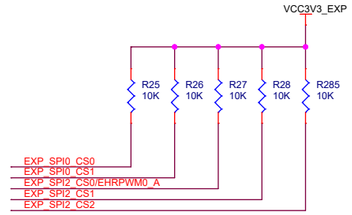
USER EXPANSION CONNECTOR

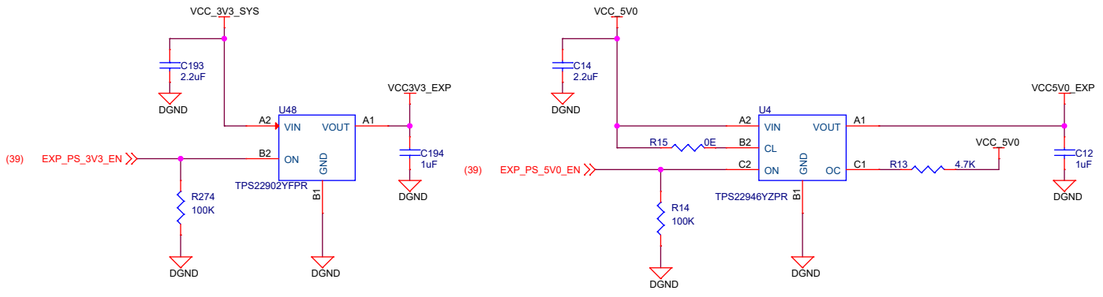




Note: Expansion boards should take care of the null modem connectivity for the UART signals (cross-over of Rx and Tx)



POWER SWITCHES FOR USER EXPANSION CONNECTOR



I2C SWITCH FOR SoC_I2C2

NOTE:

AM62x Starter Kit shall not be powered through the 5V0 or 3V3 pins on the 40-pin User Expansion Connector.

User Expansion Connector I/O are not fail-safe and shall not be driven when AM62x Starter Kit is not powered.

5V supply of User Expansion Connector is limited to sourcing 155mA max.

3V3 supply of User Expansion Connector is limited to sourcing 500mA max.

Designed for TI by Mistral Solutions Pvt Ltd

Title	USER EXPANSION CONNECTOR	
Size C	PROC142A1(002)	Rev A1
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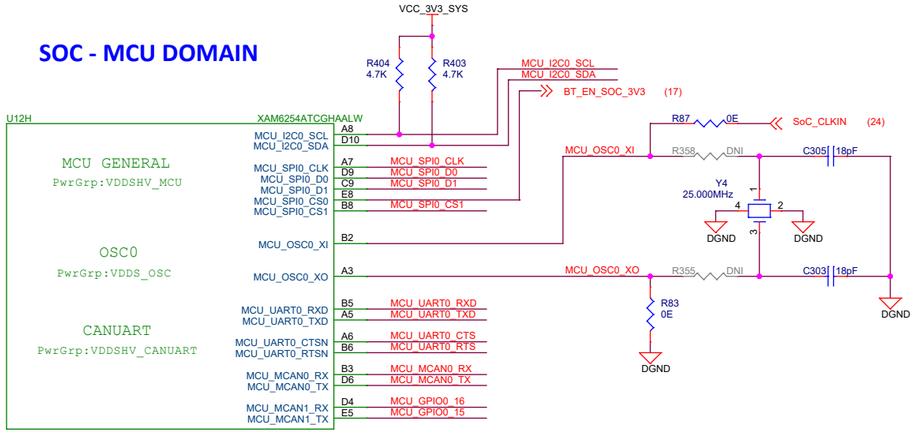
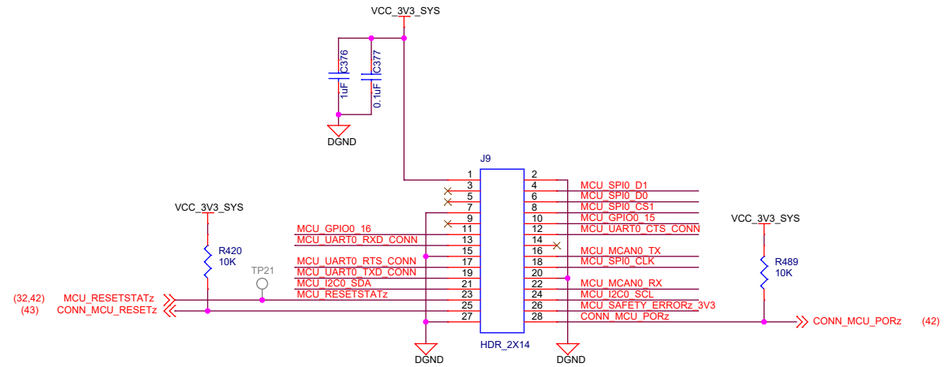
SOC - MCU DOMAIN

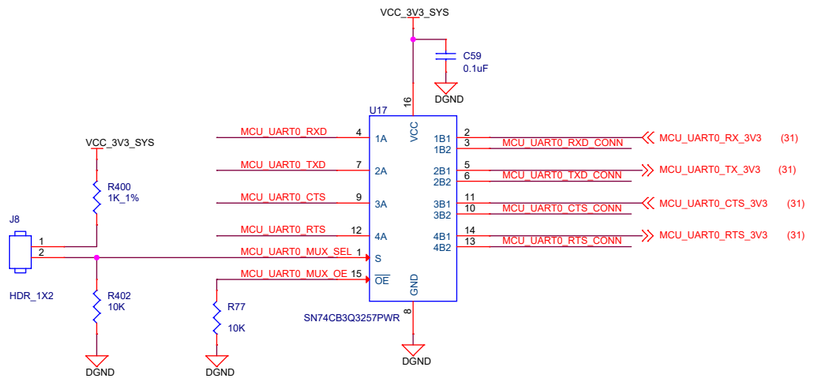


MCU HEADER

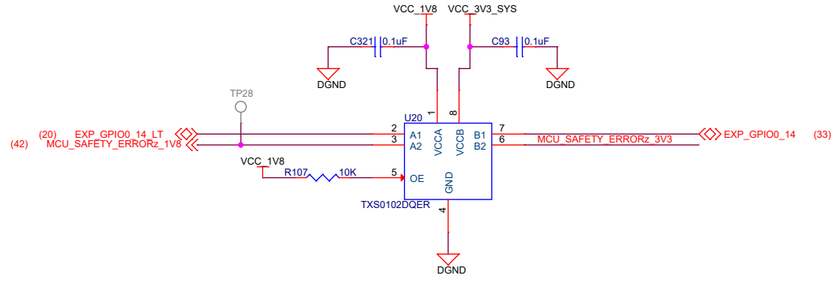


Silk: MCU HDR

MCU_UART0 MUX



OEn	SEL	INPUT/OUTPUT An	
L	L(DEFAULT)	An=nB1	SOC - FT4232
L	H	An=nB2	SOC - MCU HEADER



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Title	MCU HEADER	
Size C	PROC142A1(002)	Rev A1
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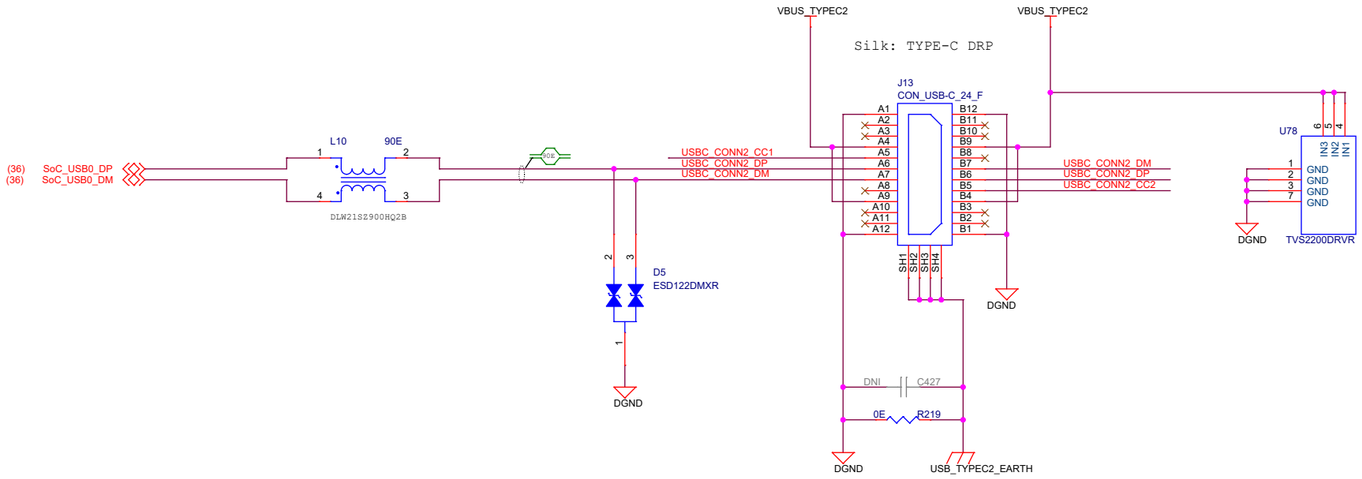
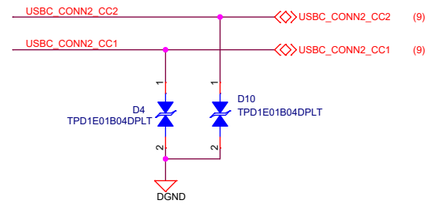
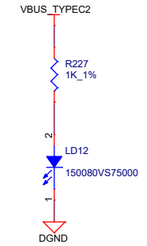
USB0 TYPE-C DRP

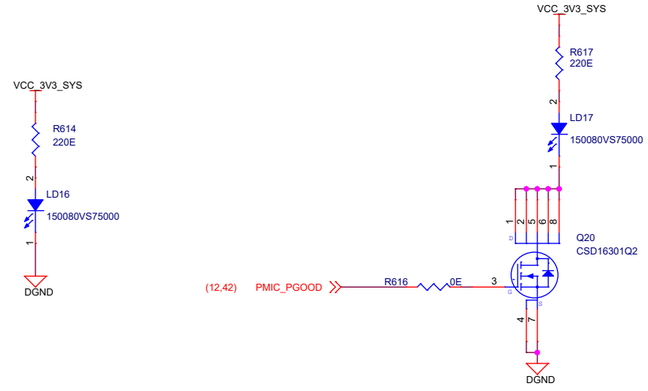




POWER INDICATION LED: VBUS_TYPEC2



POWER RAIL LEDS



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Title	USB0 TYPE-C DRP	
Size: C	PROC142A1(002)	Rev: A1
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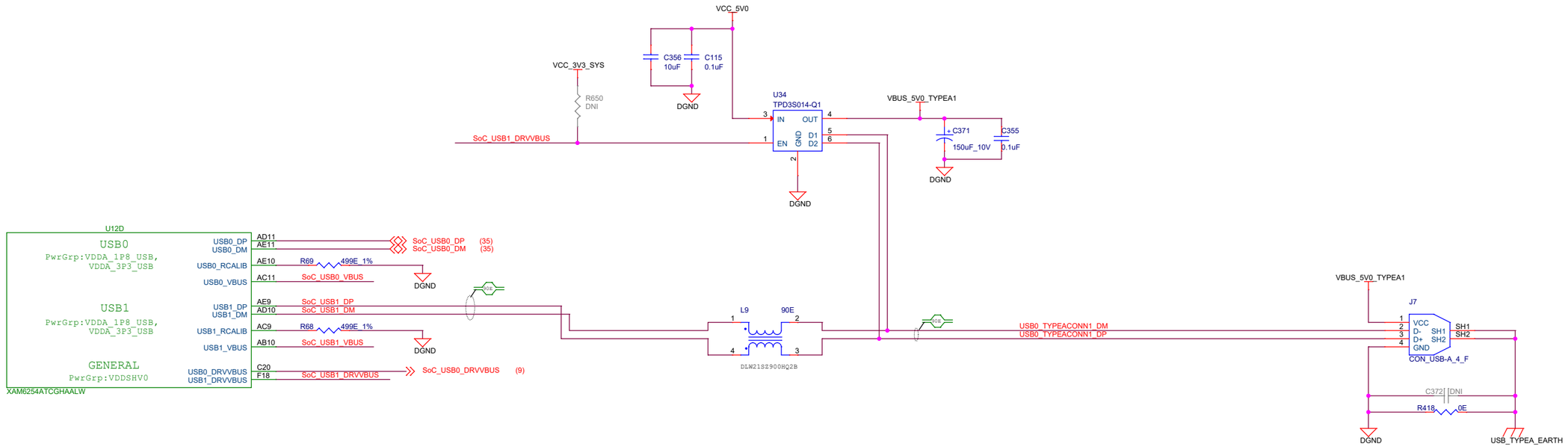
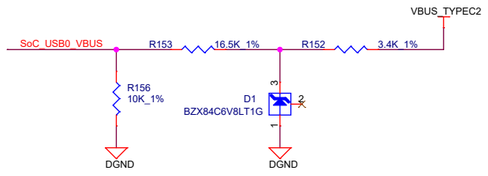
USB1 TYPE-A

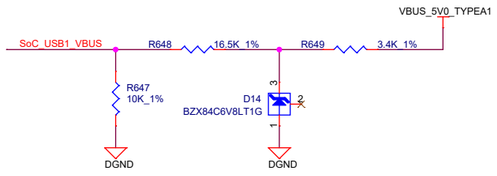


Silk: TYPE-A

Note: Recommended VBUS circuit for USB connector. Supports 5V-30V VBUS



Note: Recommended VBUS circuit for SoC_USB1_VBUS



Designed for TI by Mistral Solutions Pvt Ltd

Title	USB1 TYPE-A	
Size: C	PROC142A1(002)	Rev: A1
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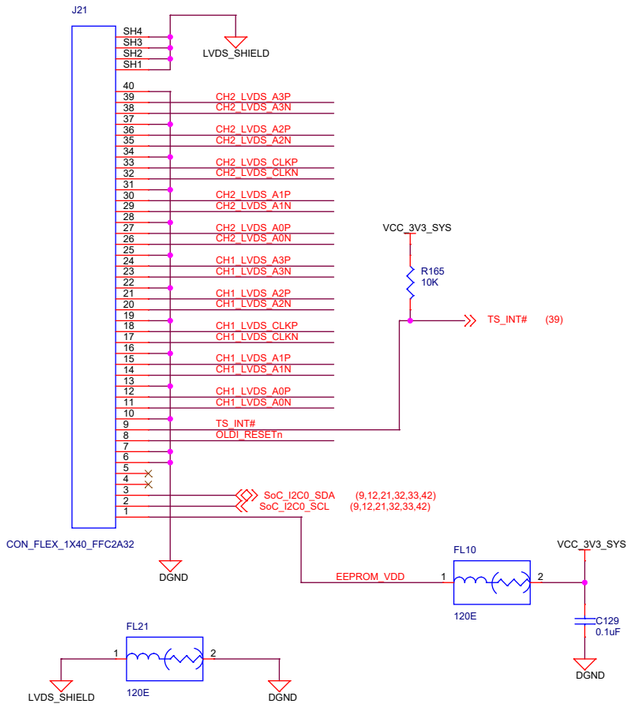
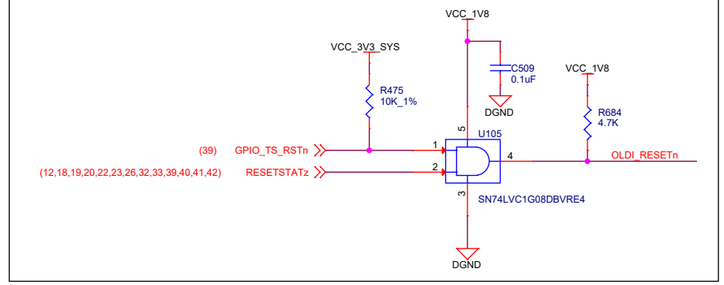
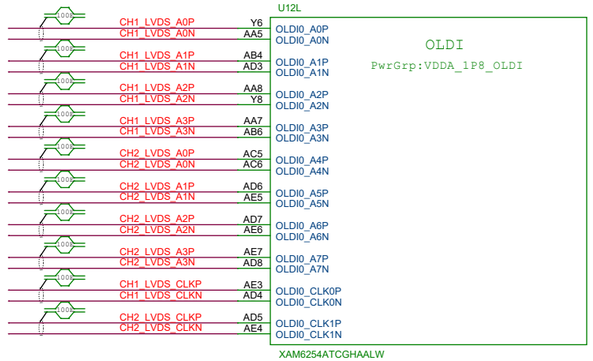
OLDI DISPLAY INTERFACE

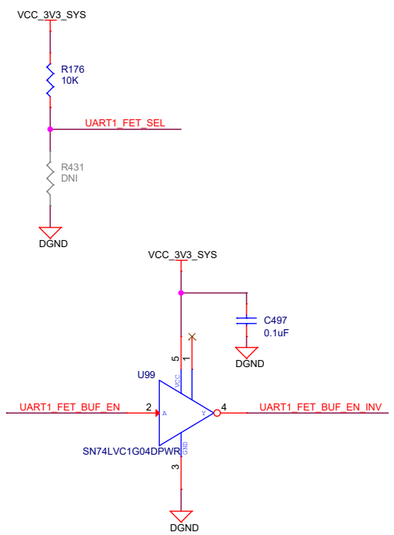


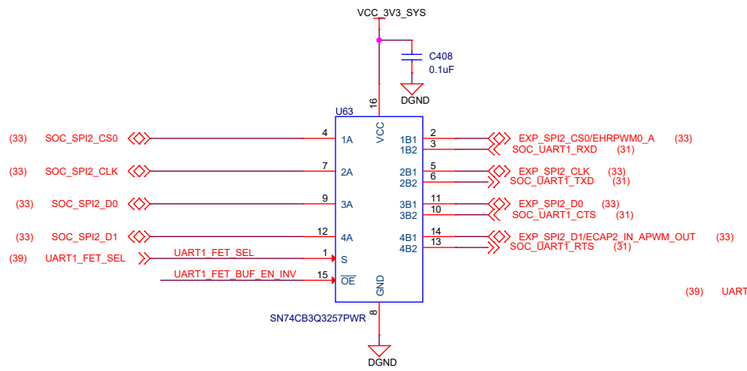
OLDI RESET

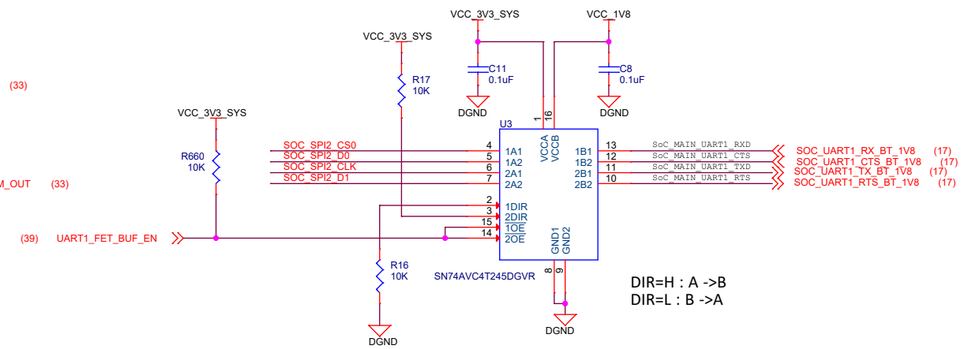




SoC UART1 FET SWITCH & BUFFER







OEn	SEL	INPUT/OUTPUT An	
L	H(DEFAULT)	An=nB2	FT4232
L	L	An=nB1	EXP CONN

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Title	OLDI DISPLAY INTERFACE	
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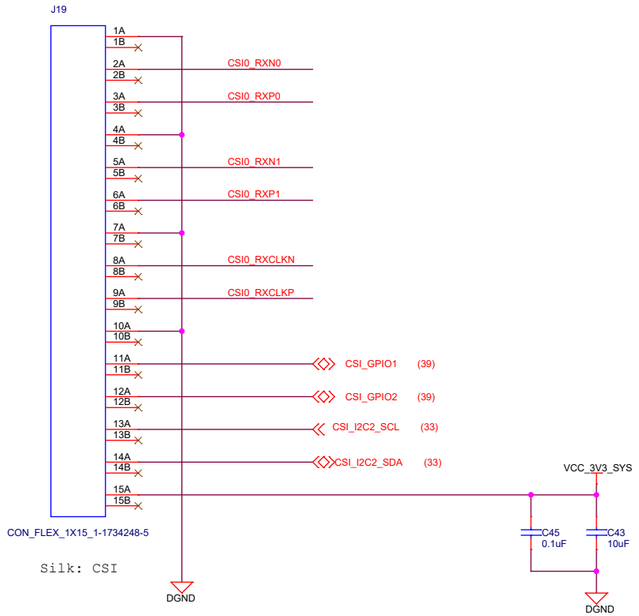
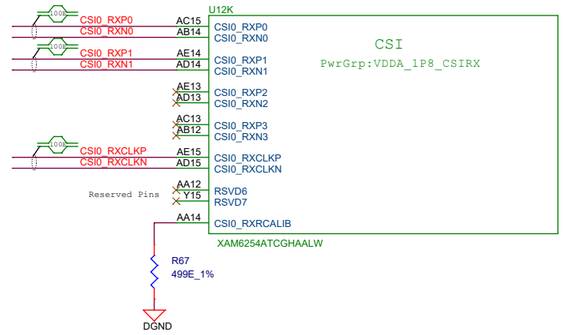
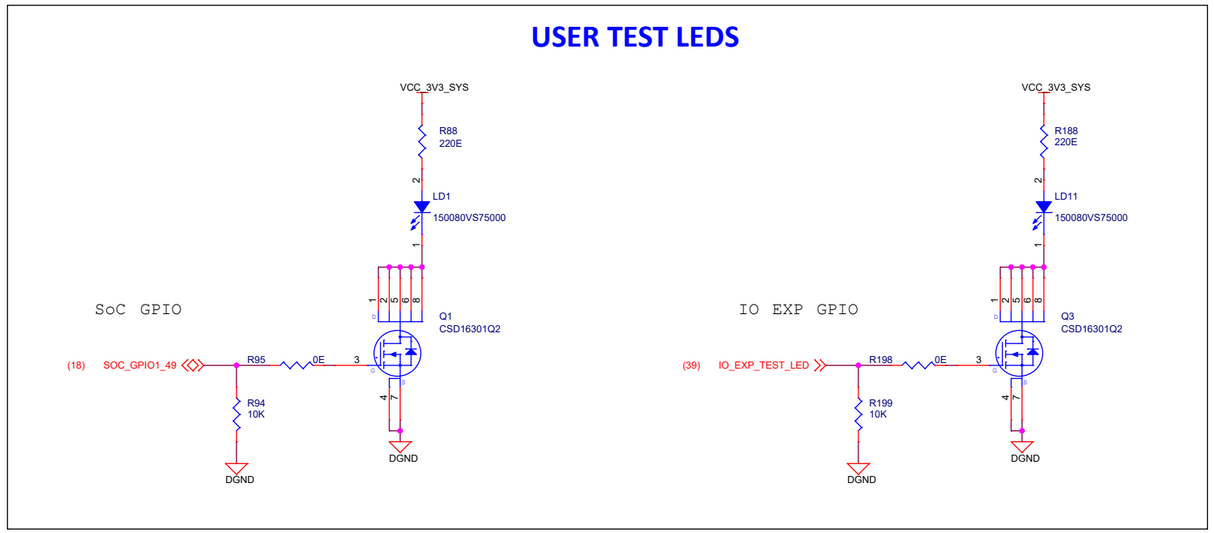
CSI INTERFACE

CSI CAMERA HEADER





USER TEST LEDS



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Title	CSI INTERFACE & USER TEST LEDS		
Size	PROC142A1(002)		Rev
C			A1
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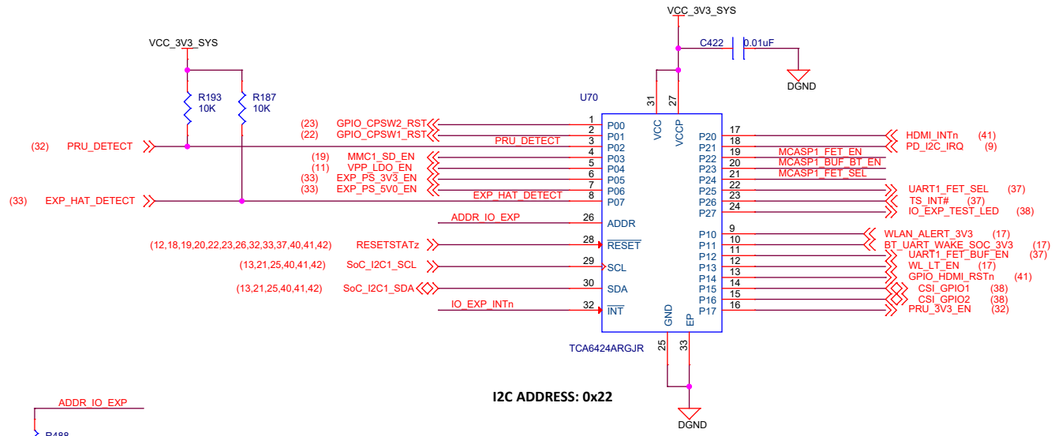
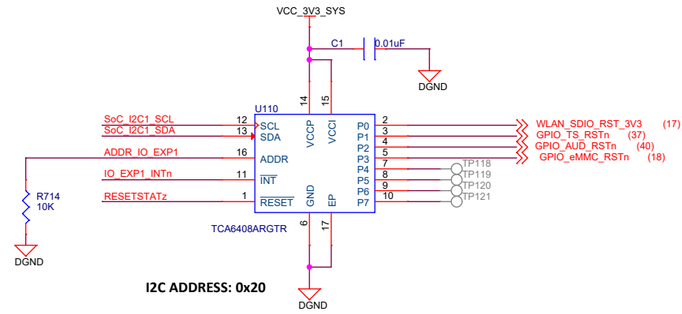
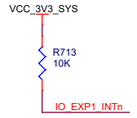
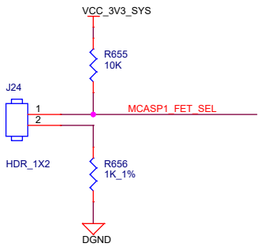
IO EXPANDERS

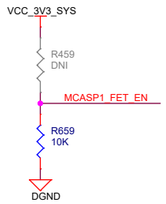


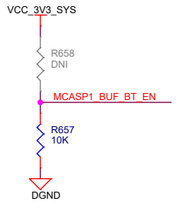


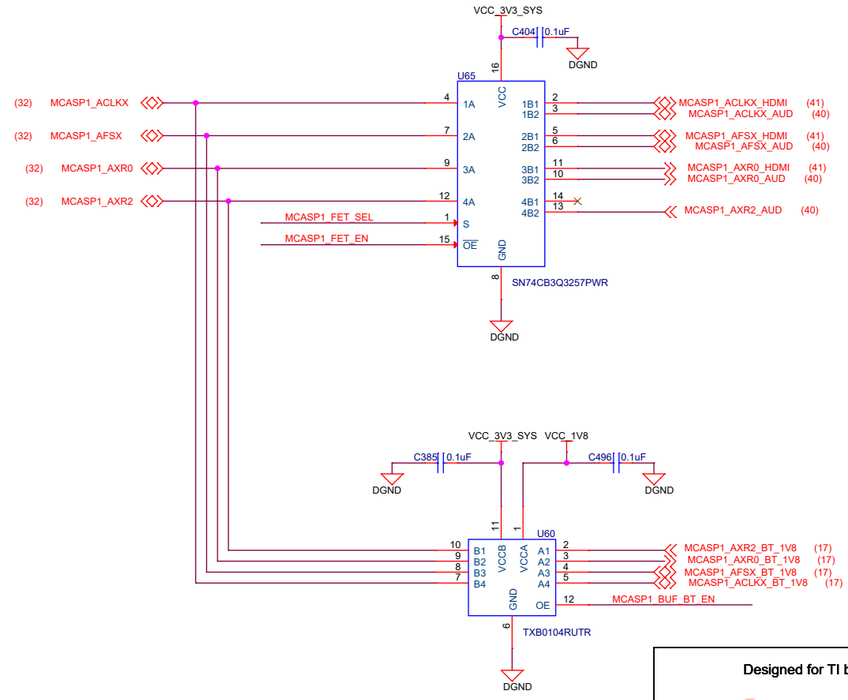


MCASP1 FET SWITCH & BUFFER









OEn	SEL	INPUT/OUTPUT An	
L	H(DEFAULT)	An=nB2	MCASP1 - CODEC
L	L	An=nB1	MCASP1 - HDMI

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Title	IO EXPANDER	
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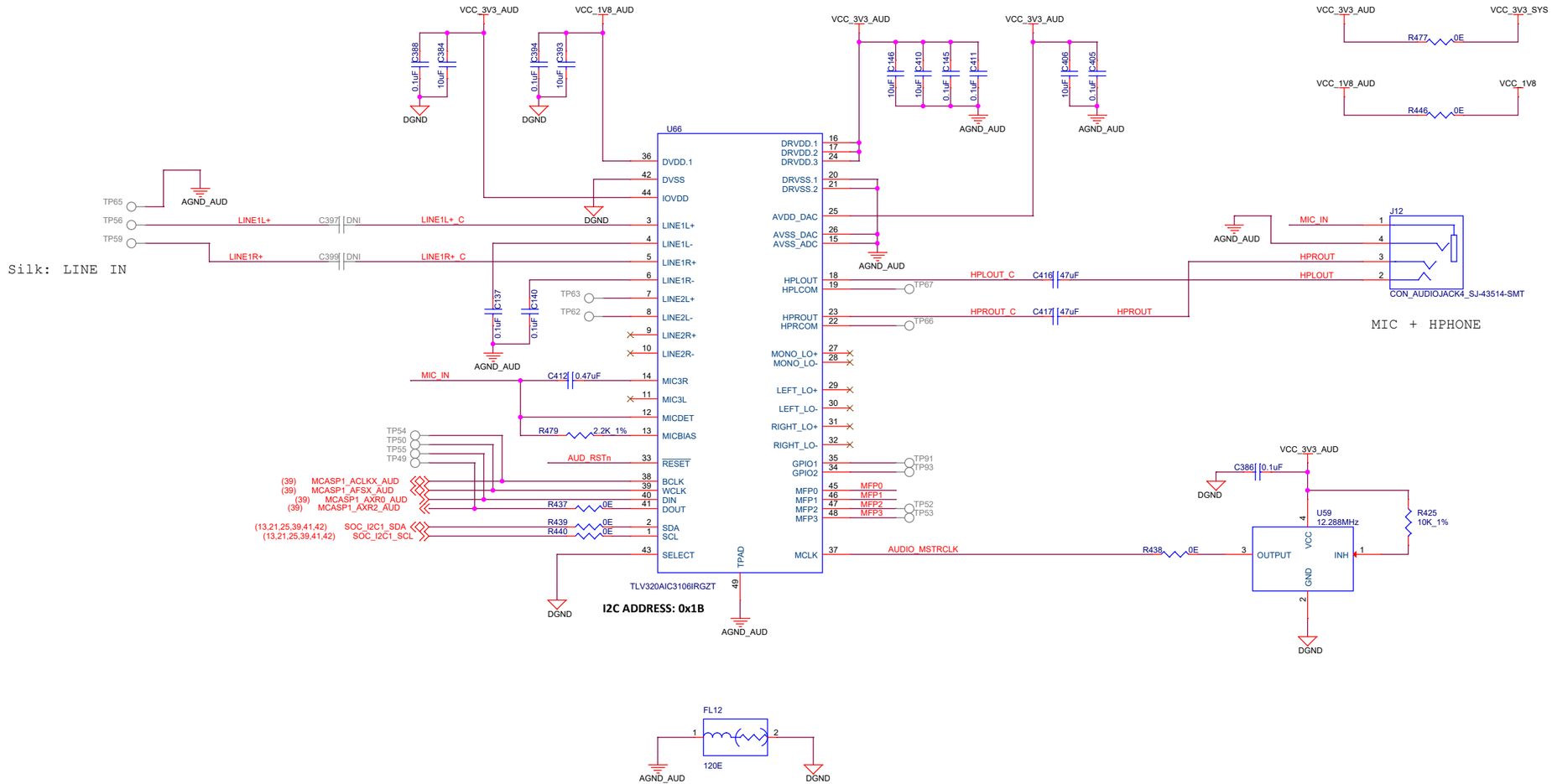
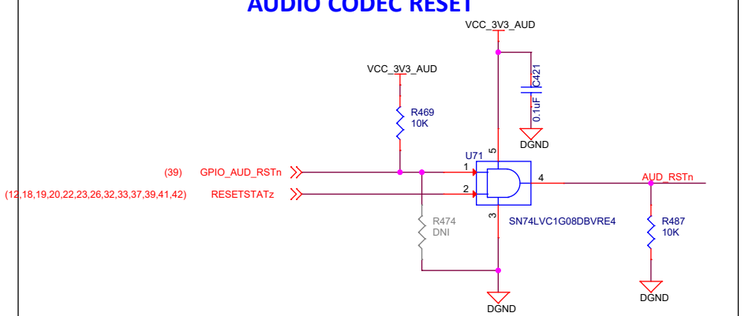
AUDIO CODEC

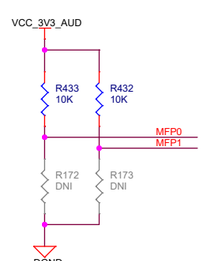


AUDIO CODEC RESET



CODEC I2C ADDRESS SELECTION

MFP0	MFP1	Device Address
0	0	0x18
0	1	0x19
1	0	0x1A
1	1	0x1B



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Title	AUDIO CODEC	
Size C	PROC142A1(002)	Rev A1
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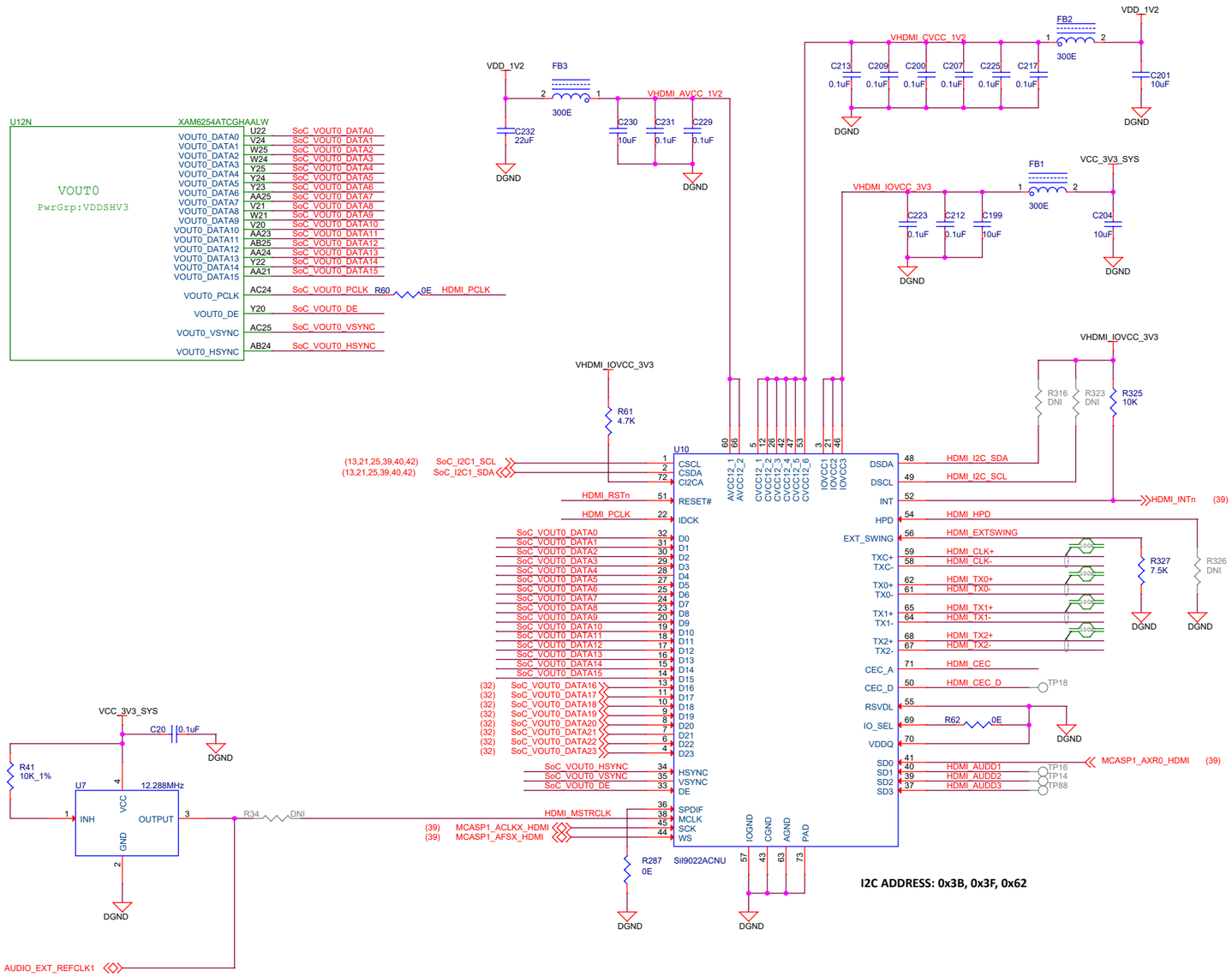
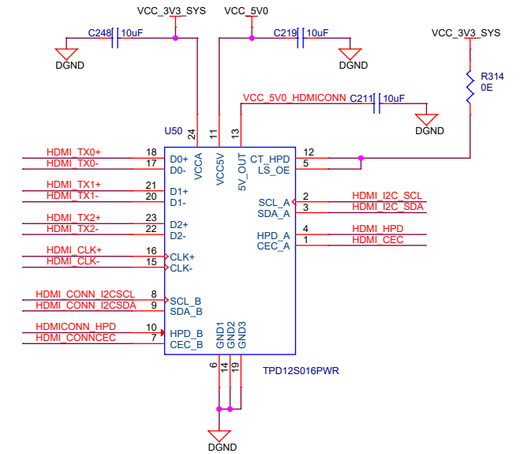
HDMI INTERFACE



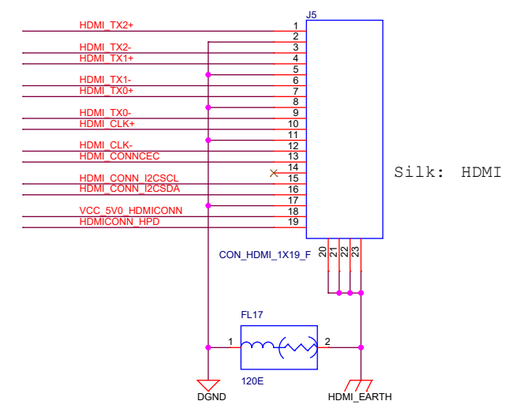
I2C ADDRESS: 0x3B, 0x3F, 0x62

HDMI ESD DEVICE

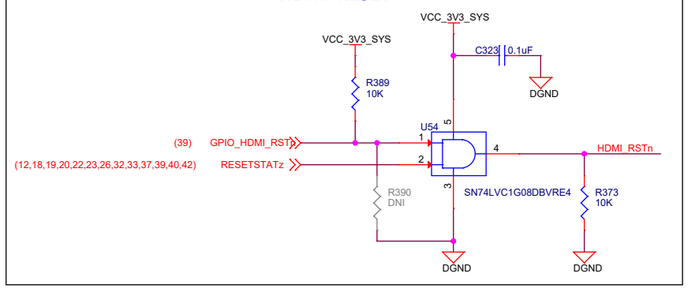


NOTE:
TPD12S016PWR has integrated pullup or pulldown resistors on the I2C and HPD lines hence no external pullup or pulldown required.

HDMI CONNECTOR



HDMI RESET



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Title	HDMI INTERFACE	
Size C	PROC142A1(002)	Rev A1
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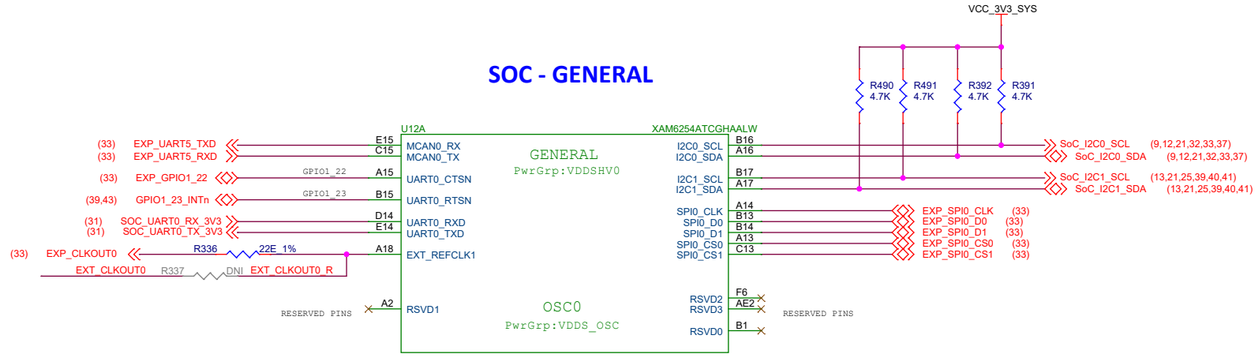
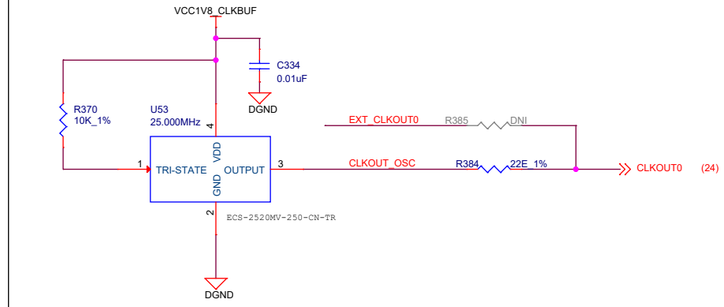
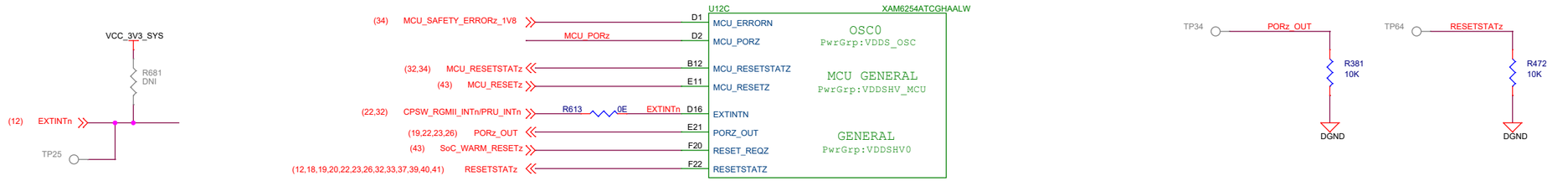
SOC - GENERAL

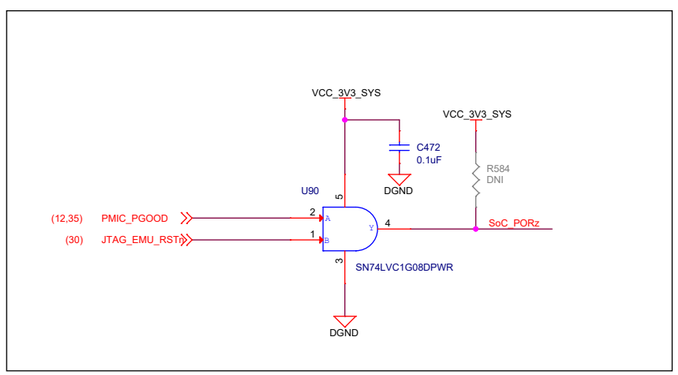


OSCILLATOR

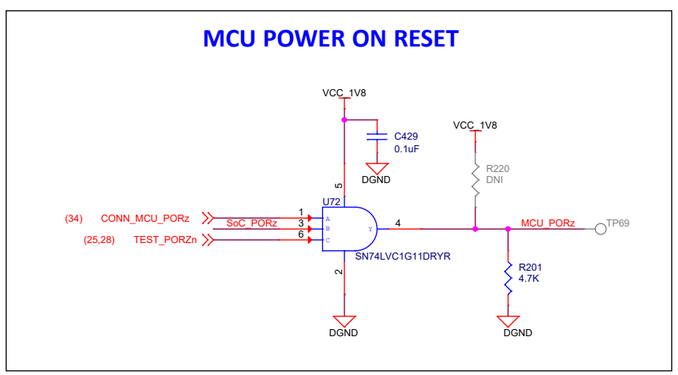


SOC - RESET





MCU POWER ON RESET



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Title	OSCILLATOR		
Size	PROC142A1(002)		Rev
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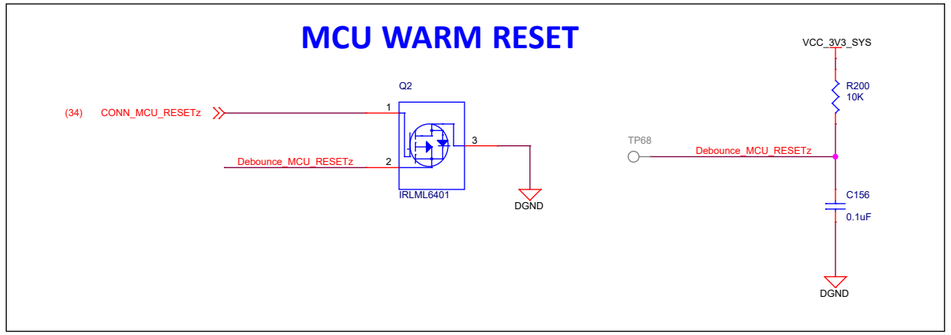
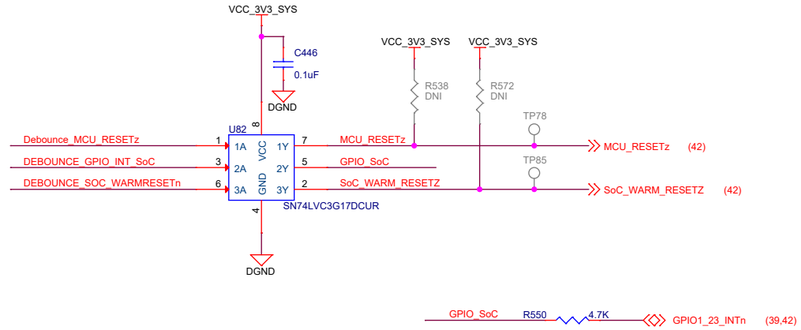
RESET

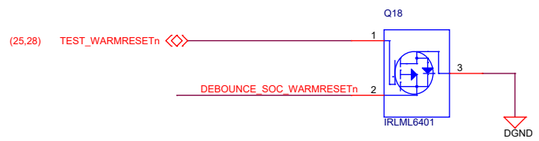
MCU WARM RESET

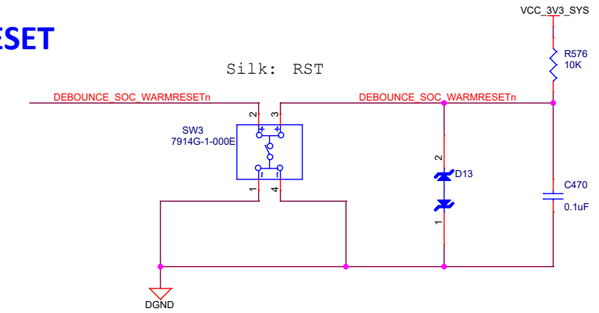


DEBOUNCE CIRCUIT

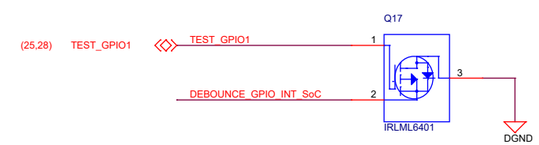


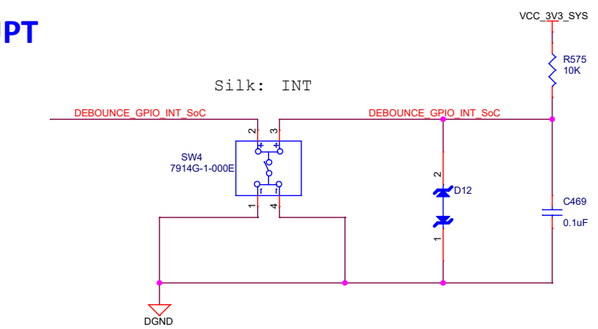
SOC WARM RESET





USER INTERRUPT





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Title	RESET	
Size: C	PROC142A1(002)	Rev: A1
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HARDWARE SCHEMATICS

ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.

2. PCB should be baked at 120 degree for 8 hours.

3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.

4. These assemblies are ESD sensitive, ESD precautions shall be observed.

5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

6. Provide serial numbers to the assembled boards for identification.

7. The assembled board are wrapped in ESD Covers(individual) and
packed securely before shipment.

BARE PCB

PROC142E1

PROC142E1

LOGOs

PCB LOGO DNI
Texas Intruments

PCB LOGO DNI
For Evaluation only; not FCC approved for resale

PCB LOGO DNI
WEEE Mark

PCB LOGO DNI
CE Mark

LABELS

Board Serial No.

LBL1
PCB LABEL
DNI

Assembly Revision

LBL2
PCB LABEL
DNI

STANDOFF,SCREW & WASHER FOR PCIe M.2

ACC1
9774015243R

MH1
FLAT WASHER_M2
3356

MH2
PAN HEAD_M2 X 5
MPMS 002 0005 PH

FIDUCIALS

FID1 DNI
FID2 DNI
FID3 DNI
FID4 DNI
FID5 DNI
FID6 DNI

ORDERABLE PART NO

LBL3
PCB LABEL
DNI

Oderable Part Number	
Variant	**Label Text**
001	SK-AM62-P1
002	SK-AM62B-P1

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Title	HARDWARE SCHEMATICS		
Size C	PROC142A1(002)		Rev A1
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