Choosing the Correct OPA, ADC in Your System

Presenter:
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The Signal Chain

Signal conditioning / Driving:
- Amplification
- Attenuation
- Filtering
- Buffering the signal chain from the input
- Conversion (V to I for example)
  - Linearization

Signal Digitizing:
- Data processing/analyzing
- Data recording
- Data Transmission
- Displaying
Agenda

• OPA Selection
  – Fundamental of Amp
  – Question
  – Spec
  – Tool

• A/D Converters Selection
  – DC & AC Specifications
  – ADC Architectures
    • Overview
    • Delta Sigma
    • SAR
  – Some Other Important Spec
  – Select the right A/D converter for your application
Agenda

• Fundamental of Amp
• Question
• Spec
• Tool
Function of Amp

- Inverting Amp
- Integrator
- Photo Detector
- Summer
- Non-Inverting Amp
- Log Amp
- Current Source
- Absolute Value
- Difference Amp
- Regulator

“Same” Op Amp: Different Functions
Amplifier

- Op-Amp (OPA series)
- Difference Amp (INA series)
  - Integrate feedback resistor
- Instrumentation Amp (INA series)
  - Integrate 3 Op-Amp
  - High Input Impedance
- Programmable Gain Amp (PGA series)
  - Self-gain setting
- Audio Amp (OPA series)
  - Excellent THD+N
Agenda

• Fundamental of Amp
• Question
• Spec
• Tool
Common Question for Choosing Right OP Amp

• Signal Input? Signal Output?
• Supply Voltage(s)? Single or Dual Supply?
• Bandwidth and Slew Rate?
• Accuracy? Vos and Vos drift?
• Need Low Input Bias Current?
• Need Low noise?
• Need RRIO?
• Output Current?
• Is low IQ important? Temperature range?
• How many Channels in one package?
• Package Choice?
• Cost
**Gain Bandwidth Product**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>STANDARD GRADE OPA827AI</th>
<th>HIGH GRADE OPA827AI</th>
</tr>
</thead>
<tbody>
<tr>
<td>FREQUENCY RESPONSE</td>
<td></td>
<td>MIN</td>
<td>TYP</td>
</tr>
<tr>
<td>Gain-Bandwidth Product</td>
<td>GBW</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*GBW = Gain·BW*  
In this example, for any gain from 0dB to $A_{\text{vol}}$.  

where  
GBW -- Gain Bandwidth in Hz  
Gain -- closed loop voltage gain  
BW -- Bandwidth in Hz  

For example  
Gain = 100  

Closed Loop Bandwidth is calculated:  

$$BW = \frac{\text{GBW}}{\text{Gain}} = \frac{22\text{MHz}}{100} = 220\text{kHz}$$  

**Open-Loop Gain and Phase vs Frequency**

- Gain = 100 = 40dB  
- BW = 220kHz
Non-ideal Op-Amp

• Gain Bandwidth Product

\[ G_{\text{linear}} = \frac{10^{20}}{} = 77.179 \]

\[ V_{\text{out}} = 2 \text{mVpp} \cdot 77.179 = 154\text{mVpp} \]
Non-ideal Op-Amp

• Input Offset Voltage

\[ V_{out} = (1 \text{mV} + 0.1 \text{mV}) \times 100 = 110 \text{mV} \]

Vin 1m

Vos 0.1mV

R1 1k

R2 99k

R3 1k
Non-ideal Op-Amp

- **Input Offset Drift**

\[ \text{Example calculations:} \]

\[ V_{osi} = 100 \, \mu N + 1.5 \frac{\mu N}{C} \cdot [(25C) - 25C] = 100 \, \mu N \quad \text{At 25C} \]

\[ V_{osi} = 100 \, \mu N + 1.5 \frac{\mu N}{C} \cdot [(125C) - 25C] = 250 \, \mu N \quad \text{At 125C} \]
Non-ideal Op-Amp

• Input Bias Current

Using nodal analysis

\[
\frac{V_{\text{in}}}{R_1} + \frac{V_{\text{in}} - V_{\text{out}}}{R_f} + I_b = 0
\]

\[
V_{\text{out}} = R_f \left( I_b + \frac{V_{\text{in}}}{R_1} + \frac{V_{\text{in}}}{R_f} \right)
\]

Using superposition set \( V_{\text{in}} = 0 \)

\[
V_{\text{out}} = R_f \left( I_b + \frac{0}{R_1} + \frac{0}{R_f} \right) = I_b \cdot R_f
\]

In this example

\[
V_{\text{out}}_{I_b} = (200\text{nA}) \cdot (99\text{k}\Omega) = 20\text{mV}
\]

\[
V_{\text{out}}_{\text{Vin}} = 1\text{mV} \cdot \left( \frac{99}{1} + 1 \right) = 100\text{mV}
\]

\[
V_{\text{out}}_{\text{total}} = 20\text{mV} - 100\text{mV} = 120\text{mV}
\]
Non-ideal Op-Amp

- Input Bias Current
Non-ideal Op-Amp

- Noise

![Circuit Diagram]

**Input**

- **Ideal Output**
- **Real Output**

**Vin vs Time**

-1.5
-1
-0.5
0
0.5
1
1.5

**Vout Ideal vs Time**

-4
-3
-2
-1
0
1
2
3
4

**Vout with Noise vs Time**

-4
-3
-2
-1
0
1
2
3
4

**Time (mS)**

Vout (mV)

Vout (mV)

Vout (mV)

Time (mS)
Non-ideal Op-Amp

• Input/Output Limitation
Non-ideal Op-Amp

- Input/Output Limitation
Non-ideal Op-Amp

- Slew Rate

\[
\text{Slew Rate} = \frac{\Delta V_{out}}{\Delta \text{Time}} = \frac{V_{out90\%} - V_{out10\%}}{t_{90\%} - t_{10\%}} = \frac{(9V - 1V)}{(0.625\mu s - 0.35\mu s)} = 29 \frac{V}{\mu S}
\]
Non-ideal Op-Amp

- Slew Rate
Non-ideal Op-Amp

- Slew Rate $\rightarrow$ Full Power Bandwidth

For $V_S = +/-15V$
- $10V_{PK}$ $\rightarrow$ Distortion
- $7.5V_{PK}$ $\rightarrow$ No Distortion
Agenda

• Fundamental of Amp
• Question
• Spec
• Tool
Key Specs for Amplifiers
The Operational Amplifier

Key Specifications

- Input Offset Voltage (mV) \( \rightarrow \) Precision
- Noise Density (nV/\sqrt{Hz})
- Gain Bandwidth (MHz) \( \rightarrow \) High Speed
- Slew Rate (V/\mu s) \( \rightarrow \) High Speed
- Temperature Drift (uV/\degree C) \( \rightarrow \) Precision

Power Specifications

- Supply Voltage
  - Rail to Rail I/O
  - Single/Dual Supply
- Operating Current (I_\text{Q})
- Drive Current
- Shut Down Current

Key Question: What is the most important requirement for the design?

Keywords:

- Audio (100 – 20kHz)
- Current Input (Transimpedance)
- Logarithmic (Input Range uV – V)
- Integrating (pairs w/ transimpedance)
OP Amp Checklist

1) Supply Voltage
   Band Width

   > _____
   > _____

2) Offset Voltage < _____
   Offset Voltage Drift < _____
   Voltage Noise < _____
   Input Bias Current < _____

3) $I_q$ per CH < _____
   Slew Rate > _____
   Output Current > _____
   Rail-to-Rail In / Out
   Number of CH = _____

Notes:
Specify Package:
Cost Goal:

Application:  
Project:
Agenda

• Fundamental of Amp
• Question
• Spec
• Tool
Op-Amp Selection Tool

- TI OPA Selguide tool
Some Great OP amps update
### Features

- **High DC Precision**
  - Offset Voltage: **25µV (max)**
  - Offset Voltage Drift: **0.1µV/°C (typ)** (varies with different pkgs and channels)
  - Low Bias Current: **5pA**
  - Low Noise: **5.5nV/√Hz at 1kHz**
- **Rail to Rail Input / Output**
  - 4.5V to +36V or ±2.25V to ±18V
  - High CMRR: **120dB**
  - Short Circuit Current: **65mA**
- **Fast Response**
  - GBW: **10MHz**, Slew Rate: **20V/µs**
  - Settling to 0.01% at 5V Step: **1µs**
  - High Cap Load Drive Capability: **1nF**
  - Low Quiescent Current: **1.2mA (max)**

### Benefits

- **True-Analog Precision**: Great Vos and drift over temperature without the use of internally clocked auto-zero techniques.
- **True-RRIO to 36V** maintains input and output linearity and low drift over the entire supply range.
- **True-Output Drive**: Output current and cap-load enables high stability systems while maintaining high DC precision.
- Wide dynamic range & high throughput into SAR ADC
- Ideal for interfacing with MUXES due to no input diode clamps

### Applications

- Industrial Automation
- Test and Measurement
- Sensors and control
- Multi-channel data acquisition systems
- Precision Comparator

### TI Designs

- **OPAy192**: OPA192 / OPA2192 / OPA4192
- **36V | Low Offset Voltage | RRIO E-Trim™ Op-amp**

**OPAy192**:
- **OPA192 / OPA2192 / OPA4192**
- **36V | Low Offset Voltage | RRIO E-Trim™ Op-amp**
- **36V**
- **Low Offset Voltage**
- **RRIO E-Trim™ Op-amp**
- **OPA192**
  - (SO-8, MSOP-8, & SOT23-5)
- **OPA2192**
  - (SO-8 & MSOP-8)
- **OPA4192**
  - (TSSOP-14 & SO-14)
- **Applications**
  - Industrial Automation
  - Test and Measurement
  - Sensors and control
  - Multi-channel data acquisition systems
  - Precision Comparator
- **Released / Sampling / Preview**
  - OPA192 (SO-8, MSOP-8, & SOT23-5)
  - OPA2192 (SO-8 & MSOP-8)
  - OPA4192 (TSSOP-14 & SO-14)

**TI Designs**
- TIPD128, 140, 151, 119

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**Texas Instruments**
Complete Design Detail

OPAy192 TI Precision Design
Design Theory, Methodology, Simulation, Results

Simulation

Figure 22: TINA-Ti™ – Schematic for Checking Input Driver Noise

Measured Results

ADC 16-bit Linearity Error

Figure 30: Measurement Data – ADC INL Plot (11 Points)
### OPAx172: OPA172 | OPA2172 | OPA4172

36V Single-Supply | 10MHz | RRO Op-Amp

#### Features
- Supply Range: +4.5 V to +36 V, ±2.25 V to ±18 V
- DC performance:
  - Offset Voltage: 1 mV (max)
  - Offset Voltage Drift: 1.5 µV/°C (max)
  - Low Bias Current: 15 pA (max)
- AC performance:
  - GBW: 10 MHz
  - Slew Rate: 10 V/µs
  - Noise Voltage: 7 nV/√Hz
  - Low Quiescent Current: 1.8 mA/ch (max)
- EMI/RFI Filtered Inputs, Rail-to-rail Output
- Short circuit current: 75 mA
- High capacitive load drive: 300 pF
- Superior THD Performance: 0.00005%

#### Benefits
- Support low voltage sensor inputs to high voltage industrial applications
- **High accuracy and precision** over the entire industrial temperature range
- Wide bandwidth and fast response suitable to drive high performance ADCs
- Enable sensing of signals close to supply/ground and maximizes the **dynamic range** and improved SNR of the signal chain
- **Clean signal** with improved noise immunity
- Suitable for driving inductive loads
- Increased **stability and reduced peaking**

#### Applications
- Tracking Amplifier in Power Modules
- Transducer Amplifiers, Bridge Amplifiers
- Temperature Measurements
- Strain Gauge Amplifiers
- Precision Integrators, Test equipment

#### Packaging options:
- Single: SC-70, SO-8, SOT-23
- Dual: SO-8, MSOP-8
- Quad: SO-14, TSSOP-14

(Released / Sampling / Preview)

**TIPD128: Capacitive Load Drive Solution using an Isolation Resistor**
OPAx172: OPA172 | OPA2172 | OPA4172

• Why were these parts developed?
  – The OPAx172 was for customers who needed a cost competitive high bandwidth on wide supply 36V mid performance general purpose op amps.
  – The OPAx172 family (10MHz) is an extension of the OPAx170 (1MHz) and OPA171 (3MHz) families.

• Why is this part so great?
  – Performance/price value: This economical family has wide bandwidth, low offset/drift, low bias current and low noise specifications in the smallest packaging for a 36V op amp.

• Why is this part better than the competition?
  – Lower power consumption for high bandwidth (10MHz)
  – Lower offset/drift and bias current
  – Higher output drive (75mA)
  – Smallest package for single channel (SC-70)
Choosing The Right A/D Converters for Your systems
Agenda

- Basic Knowledge of ADC features
- DC & AC Specifications
- ADC Architectures
- Select the right A/D converter for your application
Basic Knowledge of ADC Features
ADC Analog Input Configurations

Single-Ended Input / Pseudo Differential

- Requires full input swing from $+fs$ to $-fs$
- 2x the swing compared to differential
- Input signal at IN typically requires a common-mode voltage for bias
- Input INN also requires a Vcm for correct dc-bias

Differential Input

- Combined Differential inputs result in full-scale input of $+fs$ to $-fs$
- Each input only requires 0.5x the swing compared to single-ended
- Both inputs require a Vcm for correct dc-bias
How do we know what input mode of a given ADC?

### Single-ended

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>ADS7924</th>
</tr>
</thead>
<tbody>
<tr>
<td>ANALOG INPUT</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Full-scale input span</td>
<td>(CHX – AGND)</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AVDD</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

### Pseudo differential

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>ADS7924</th>
</tr>
</thead>
<tbody>
<tr>
<td>ANALOG INPUT</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Full-scale input voltage</td>
<td>+IN – (–IN)</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{\text{ref}}$</td>
</tr>
<tr>
<td>Absolute input voltage</td>
<td>+IN</td>
<td>−0.2</td>
</tr>
<tr>
<td></td>
<td>−IN</td>
<td>−0.2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

### Fully differential

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>ADS7924</th>
</tr>
</thead>
<tbody>
<tr>
<td>ANALOG INPUT</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Full-scale input span</td>
<td>AINP – AINN</td>
<td>$-V_{\text{REF}}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{\text{REF}}$</td>
</tr>
<tr>
<td>Operating input range</td>
<td>AINP</td>
<td>−0.1</td>
</tr>
<tr>
<td></td>
<td>AINN</td>
<td>−0.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{\text{REF}} + 0.1$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>
Unipolar vs Bipolar Input

- **Unipolar ADC:**
  - Only positive voltage (typical digital output straight binary)

- **Bipolar ADC:**
  - Negative and positive voltage (typical digital output 2’s complement)
Unipolar vs Bipolar (digital output)

Typical Formats

<table>
<thead>
<tr>
<th>Straight Binary</th>
<th>Code 0000</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Code 0111</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>Code 1000</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>Code 1111</td>
<td>15</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>2’s Complement</th>
<th>Code 1000</th>
<th>-8</th>
</tr>
</thead>
<tbody>
<tr>
<td>Code 1111</td>
<td>-1</td>
<td></td>
</tr>
<tr>
<td>Code 0000</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>Code 0111</td>
<td>7</td>
<td></td>
</tr>
</tbody>
</table>

Normally used for **unipolar or Pseudo differential ADCs**

Normally used for **bipolar or fully differential ADCs**
Frequent Ask Question when selecting ADC

Key Specifications

- **Input Mode**
  - Single-ended or differential
  - Input Impedance (Ohms)

- **Resolution - bits**
  - SNR, THD, SFDR, SINAD, ENOB

- **Accuracy**
  - INL, DNL, Offset, Gain, Drift

- **Conversion Rate** (Samples/s)

- **Interface** (Parallel/Serial)

- **Reference** – ext or int

Power Specifications

- **Supply Voltage** (Analog / Digital)

- **Power consumption**

Key note:
ADC Conversion Rate usually needs 10x faster than system input bandwidth for better signal re-construction
DC Specifications

- Offset / Full-scale / Gain
- Differential Non-linearity (DNL) /
- Integral Non-linearity (INL)
Offset Error

Offset error is the difference in voltage between the ideal first code transition and the actual code transition of an ADC, respectively the difference to the reference at code 000xxx in case of a DAC.
Gain Error (Full Scale Error)

Gain Error = Full-scale Error - Offset Error

Digital Output Code

Analog Output Voltage

Ideal Transfer Function

Actual Transfer Function

Ideal full-scale range

Actual full-scale range

FS

3/4 FS

1/2 FS

1/4 FS

Positive Gain error

Negative Gain error

Digital Input Code

000

001

010

011

100

101

110

111
A DNL error beyond +/-1LSB can cause missing codes in an ADC or Non-Monotonic behavior of a DAC.
An **INL** error is the maximum deviation of a transition point from the corresponding point of the ideal transfer curve, with the measured offset and gain errors zeroed.
AC Specifications

- SNR (signal-to-noise ratio)
- THD (total harmonic distortion)
- SINAD (signal-to-noise-and-distortion ratio)
- ENOB (effective number of bits)

ps. Those are popular specifications for quantifying ADC dynamic performance
SNR (Signal to Noise Ratio)
SNR definition

\[ SNR = 20 \log_{10} \left( \frac{\text{rms value of signal amplitude}}{\text{rms value of quantization noise}} \right) \]

\[ SNR = 20 \log_{10} \left( \frac{A / \sqrt{2}}{q / \sqrt{12}} \right) = 6.02N + 1.76 \text{ dB} \]

A = Signal amplitude
q = LSB

Measured over the Nyquist Bandwidth: DC to Fs/2

Ideal ADC system, only consists quantization noise
THD (Total Harmonic Distortion)
THD = Total Harmonic Distortion is the sum of power in the first ten harmonics relative to the fundamental signal power (dBc)

Spurious Free Dynamic Range (SFDR)

H9 - H10 have aliased back to the first Nyquist zone
The rms sum of powers of harmonic components (Spurs) rationed to input signal power

$$THD = 20 \log_{10} \frac{\sqrt{H_2^2 + H_3^2 + H_4^2 + \ldots + H_n^2}}{V_s^2}$$

Where

- $V_s$ is fundamental amplitude
- $H_2$ is second Harmonic amplitude
SINAD (Signal to Noise Ratio + Distortion) or SNDR (Signal-to-noise and distortion ratio)

\[ ENOB = \frac{(SINAD - 1.76)}{6.02} \]

SINAD = the sum of all power except DC and the fundamental relative to the signal power (dBc)
Signal-to-Noise-and-Distortion (SINAD, or SNDR) - definition

\[
SINAD = 20 \log_{10} \frac{V_s}{\sqrt{H_2^2 + H_3^2 + H_4^2 + \ldots + H_n^2 + \text{noise}^2}}
\]

Where

- \(V_s\) is fundamental amplitude
- \(H_2\) is second Harmonic amplitude

- Signal-to-Noise-and-Distortion (SINAD, or SNDR) is the ratio of the rms signal amplitude to the mean value of the root-sum-square (rss) of all other spectral components, *including harmonics*, but excluding dc. SINAD is a good indication of the overall dynamic performance of an ADC because it includes all components which make up noise and distortion.
ENOB (Effective Number of Bits)

ENOB specifies the dynamic performance of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists only of quantization noise. As the input frequency increases, the overall noise (particularly in the distortion components) also increases, thereby reducing the ENOB and SINAD.

\[
\text{ENO} = \frac{\text{SINAD}_{\text{MEASURED}} - 1.76 \, \text{db} - 20 \log \left( \frac{\text{Fullscale Amplitude}}{\text{Input Amplitude}} \right)}{6.02}
\]

EXAMPLE – ADS1148

Table 6. Effective Number of Bits From Peak-to-Peak Noise
At V_{\text{REF}} = 2.048V, AVDD = 5V, and AVSS = 0V

<table>
<thead>
<tr>
<th>DATA RATE (SPS)</th>
<th>1</th>
<th>2</th>
<th>4</th>
<th>8</th>
<th>16</th>
<th>32</th>
<th>64</th>
<th>128</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
</tr>
<tr>
<td>10</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
</tr>
<tr>
<td>20</td>
<td>15</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>15.8</td>
</tr>
<tr>
<td>40</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>15.4</td>
</tr>
<tr>
<td>80</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>15.8</td>
<td>15.0</td>
</tr>
<tr>
<td>160</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>15.1</td>
<td>14.3</td>
</tr>
<tr>
<td>320</td>
<td>16</td>
<td>15.8</td>
<td>15.8</td>
<td>15.8</td>
<td>15.8</td>
<td>15.4</td>
<td>14.7</td>
<td>13.7</td>
</tr>
<tr>
<td>640</td>
<td>15.4</td>
<td>15.5</td>
<td>15.7</td>
<td>15.3</td>
<td>15.3</td>
<td>14.9</td>
<td>14.1</td>
<td>13.2</td>
</tr>
<tr>
<td>1000</td>
<td>13.8</td>
<td>13.9</td>
<td>14.0</td>
<td>13.9</td>
<td>13.9</td>
<td>13.8</td>
<td>13.5</td>
<td>12.7</td>
</tr>
<tr>
<td>2000</td>
<td>13.9</td>
<td>13.9</td>
<td>13.9</td>
<td>13.8</td>
<td>13.7</td>
<td>13.7</td>
<td>13.2</td>
<td>12.3</td>
</tr>
</tbody>
</table>

- Smaller Vin scale
- Faster Fs
ENOB cont’d

Example: ADS1601, SNR factors
ADC Architectures
Real World vs. Bandwidth

Bandwidth (Hz)

Noise Free Resolution (bits)

Temp
Pressure
Load
Flow
Level
Displacement/Proximity
Photo Sensing
Communications
Defense
Imaging
Test & Measurement

Real World vs. Bandwidth
ADC Technologies - $\Delta \Sigma$

Advantages
- High Resolution
- Low Noise
- High Stability
- Low Power
- Low cost

Disadvantages
- Cycle-Latency

$\Delta \Sigma$ – Delta Sigma
Or Sigma Delta
(Oversampling)

Converter Resolution (bits)

Conversion Rate

SAR
Successive Approximation

Pipeline

Texas Instruments
ADC Technologies - SAR

ΔΣ – Delta Sigma
Or Sigma Delta
(Oversampling)

Advantages
• Zero-cycle Latency
• Low Latency-time
• High Accuracy
• Typically Low Power
• Easy to Use

Disadvantages
• Max Sample Rates 2-5 MHz

Converter Resolution (bits)

Conversion Rate
10  100  1K   10K  100K  1M  10M  100M  1G  SPS

8  12  16  20  24  28  32

SAR
Successive Approximation

Pipeline

TEXAS INSTRUMENTS
ADC Technologies - Pipeline

### Delta Sigma

- **Advantages**
  - Higher Speeds
  - Higher Bandwidth

- **Disadvantages**
  - Lower Resolution
  - Pipeline Delay/Data Latency
  - More power

**ΔΣ** - Delta Sigma
Or Sigma Delta
(Oversampling)

**SAR**
Successive Approximation

<table>
<thead>
<tr>
<th>Converter Resolution (bits)</th>
<th>Conversion Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>32</td>
<td>1G SPS</td>
</tr>
<tr>
<td>24</td>
<td>100M</td>
</tr>
<tr>
<td>20</td>
<td>10M</td>
</tr>
<tr>
<td>20</td>
<td>1M</td>
</tr>
<tr>
<td>16</td>
<td>100K</td>
</tr>
<tr>
<td>16</td>
<td>10K</td>
</tr>
<tr>
<td>12</td>
<td>1K</td>
</tr>
<tr>
<td>12</td>
<td>100</td>
</tr>
<tr>
<td>8</td>
<td>10</td>
</tr>
<tr>
<td>8</td>
<td>1</td>
</tr>
</tbody>
</table>

**Pipeline**
Select the right A/D converter for your application
## Selecting Suitable ADC Topology

<table>
<thead>
<tr>
<th>ADC Topology</th>
<th>F Conversion</th>
<th>Resolution</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>SAR</td>
<td>≤ 4Msps</td>
<td>≤ 16-bit</td>
<td>Simple operation, low cost, low power.</td>
</tr>
<tr>
<td></td>
<td>≤ 1.25Msps</td>
<td>≤ 18-bit</td>
<td></td>
</tr>
<tr>
<td>Delta-Sigma</td>
<td>≤ 4ksps</td>
<td>≤ 32-bit</td>
<td>Moderate cost.</td>
</tr>
<tr>
<td></td>
<td>≤ 4Msps</td>
<td>≤ 24-bit</td>
<td></td>
</tr>
<tr>
<td></td>
<td>≤ 10Msps</td>
<td>≤ 16-bit</td>
<td></td>
</tr>
<tr>
<td>Pipeline</td>
<td>≤ 200Msps</td>
<td>≤ 16-bit</td>
<td>Fast, expensive, higher power requirements.</td>
</tr>
<tr>
<td></td>
<td>≤ 250Msps</td>
<td>≤ 14-bit</td>
<td></td>
</tr>
<tr>
<td></td>
<td>≤ 1000Msps</td>
<td>≤ 12-bit</td>
<td></td>
</tr>
</tbody>
</table>
What Do You Know About Your Signal?

• Desired Bandwidth?
  – up to 4MSPS SAR,
  – up to 10MSPS Delta Sigma,
  – above Pipeline

• Is DC precision important?
  – YES  -> look at Delta Sigmas at first choice
  – alternative SAR Converters with DC Precision

• Does your signal have frequency content above Nyquist?
  – YES, and it needs to be detected -> SAR or Pipeline with external Bandpass Filter -> Undersampling
  – YES, but can be removed -> SAR or Pipeline or Delta Sigma with Sinc Filter plus an external Anti Aliasing Filter (AAF)
  – YES, but no external filter possible -> Delta Sigma with FIR
  – NO -> Delta Sigma with Sinc or FIR filter or SAR or Pipeline
What To Find Out About Your Signal?

• A specific point in time needs to be frozen?
  – YES -> Sample and hold Stage is needed like in SAR, Pipeline (no Delta Sigma)

• Can an average of your signal be used as long as the constant phase relation does exist?
  – YES -> Delta Sigmas can be used as they average the signal

• Do you need to convert multiple signals in phase relation to each other?
  – YES -> multiple synchronous S/H are needed or synchronous Delta Sigma Modulators – Multi Channel converters exist for all three types SAR, Delta Sigma, Pipeline
  – NO -> Multiplexing can be used. Exists for SAR and Delta Sigma.
Input Voltage Range?

• Does it fit directly to an available ADC?
  – single ended or differential inputs exist
  – SAR ADCs offer unipolar or bipolar
  – Delta Sigmas offer unipolar and bipolar, can have build in PGA

• Can it be adapted externally by OPAs / INAs / resistors?
  – Sometimes external driving circuit is needed anyway – SAR and Pipeline: signal can be adapted with this for saving cost and power
  – Consider signal conditioning in combination with single supply converter
Power Consumption

• Power consumption and/or dissipation is generally a concern, but performance needs may demand certain power

• Delta-sigma: allows nice trade-off between resolution, speed and power-consumption

• SARs: are generally the low-power option

• Pipeline ADCs: are relatively power-hungry to achieve their high performance-levels
Some Great A\D Converters update
**Features**

- **Highest Resolution ADC:**
  - 27 bit ENOB, 7nV Noise (@5SPS)
- **11 Flexible, Multiplexed Inputs:**
  - 10 Single-Ended OR 5 Differential
- **Highly Specified Performance:**
  - Offset Drift: 1nV/°C
  - Gain Drift: 1ppm/°C
  - INL: 3ppm
- **Highly Integrated Device:**
  - Low Drift Internal Reference: 2.5V
  - GPIOs (8)
  - Internal Clock: 7.3728MHz
  - High Impedance PGA: 1/2/4/8/16/32
  - SINC + 50/60Hz Digital Filter
- **Fault Detection/Input Diagnostics**

**Benefits**

- Wide dynamic range 32-bit ADC enables direct digitization of low level sensors
- High-resolution, low-drift architecture provides the industry's best performing ADC
- A high level of integration eliminates the need for several typical discrete components, decreasing necessary PCB space and reducing costs
- Wide sample rate allows this device to be adaptable to a variety of applications
- On-chip sensor bias current sources make the ADS1262 RTD-ready
- Fault detection improves system reliability

**Applications**

- Industrial PLC
- High-End Panel Meters and Process Controllers
- High Precision Weigh Scales
- Industrial Strain Gauge Analyzers
- Analytical Equipment
- RTD Measurement
### Industry’s Highest Resolution ADC

- Industry’s only **32-bit** ADC
- $8.5 \text{nV}_{\text{RMS}}$ noise @ G=32 & 5SPS
- Programmable Digital Filter offers 96dB NMR @ 50Hz

### Industry’s Best Specified ADC

<table>
<thead>
<tr>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
</tr>
</thead>
</table>
- Industry’s best drift specifications
- Internal reference with specified long term drift
- Widest operating temperature range: -40°C to +125°C

### Highly Integrated ADC

- Includes: Burnout Current Sources; Self-Calibration; Dual Matched IDACs, “any combination you want” MUX, Temperature Sensor, GPIOs, Error Detection, Self-Test DAC
**Features**

- HV Unipolar/Bipolar inputs *with single 5V supply*
- **Input Structure:**
  - 8-SE channel MUX with auto/manual scan
  - Constant Resistive 1MΩ Input Impedance
  - Input Over Voltage Protection of ±20V
  - S/W programmable input range (per channel):
    - ±10.24V | ±5.12V | ±2.56V
    - 0-10.24V | 0-5.12V
- $V_{\text{REF}} = 4.096V$
  - Accuracy = 0.025% | Drift = 7ppm/°C (Typ)
- Precision SAR ADC Performance
  - 500kSPS (aggregate)
  - ±2 LSB INL and 16-bit NMC DNL
  - AC Performance: SNR = 92dB; THD < -100dB
  - DC Performance: Gain < 0.05%; Offset < 1mV
  - 65mW power at 500KSPS
  - SPI interface with Daisy-Chain
- Enhanced Features:
  - Auxiliary channel
- Industrial Temperature Range: -40°C to 125°C
- 38 pin leaded package

**Benefits**

- Supports bipolar input signals *with single 5V supply*
- **Analog Front End integration for direct sensor interface**
- Low-drift reference enables accurate conversions
- **Exceptional AC and DC performance;** making product ideal for industrial applications
- Small Footprint with Extended Industrial Temp range makes the ADS8688 suitable for various industrial applications

**Applications**

- Power Monitoring
- Low Cost Industrial Data Acquisition
- Protection Relays
- Metrology
ADS8688 Family
Multi-bit | 4-/8-Channel | Integrated AFE with MUX | Single +5V Supply

Features

- HV Unipolar/Bipolar Inputs *With Single 5V Supply*
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  - ±10.24V | ±5.12V | ±2.56V
  - 0-10.24V | 0-5.12V
- Input Structure Optimized For Direct Sensor Interface
  - 8-SE channel MUX with auto/manual scan
  - Constant Resistive 1MΩ Input Impedance
- Best-in-Class Reference Voltage:
  - \( V_{\text{REF}} = 4.096V \)
  - Accuracy = 0.025% | *Drift = 7ppm/°C* (Typ)

Discovery Questions
ADS8688 Family
Multi-bit | 4-/8-Channel | Integrated AFE with MUX | Single +5V Supply
ADS8688 Family
Multi-bit | 4-/8-Channel | Integrated AFE with MUX | Single +5V Supply

**Features**

- Do you have high-voltage signals you need to convert?
- How do you handle converting some high-voltage signals (0V-10V), high-voltage bipolar signals (±10V), and nominal signals (0V-5V)?
- What sampling data rate do you need?
- What is the operating temperature range you need?
- How do you design your front-end to interface with a sensor?

**Discovery Questions**

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- What is the operating temperature range you need?
- How do you design your front-end to interface with a sensor?
Device Family for ADS8688

- ADS8688 has a family of devices with variable:
  - Channel Count
  - Resolution
Questions?

alexyeh@ti.com

Thank-You for your time!