Application Report
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MSP430F5xx Overview and Comparison to MSP430F2xx and MSP430F4xx

MSP430 Applications

ABSTRACT

The MSP430F5xx series of devices is the latest addition to the MSP430™ family of microcontrollers. Although there are many common features between the MSP430F5xx and MSP430F2xx and MSP430F4xx offerings, there are also several differences. This document gives a brief overview of differences between the device families. Detailed information regarding specific differences can be found in the respective module chapters in the MSP430F5xx and MSP430F6xx Family User's Guide.

Contents

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1 Introduction

This document is a snapshot of major functional differences between the MSP430F5xx family of devices and its predecessor device families, MSP430F2xx and MSP430F4xx.

In this document, the term *core* refers to the key subsystem modules that are common to all MSP430F5xx devices. These include the central processing unit (CPUX), the Power Management module (PMM), the Unified Clock System module (UCS), the System module (SYS), as well as memory mapping and allocation.

Most of the core changes to the MSP430F5xx were required primarily to support the growing demands of microcontroller applications, which include higher levels of integration, higher performance levels at lower power, increased flexibility, and extensions for future enhancements. Although these changes were necessary, the intent was to maintain as much look and feel, as well as compatibility, with earlier MSP430 generations.

This application report contains three major sections. The first section describes the memory mapping present on the MSP430F5xx. The second section describes the core modules and any key differences from existing MSP430F2xx and MSP430F4xx devices. The last section describes each of the peripheral modules that exists on the first MSP430F5xx offerings along with any key differences from similar modules found on MSP430F2xx and MSP430F4xx devices.

2 Memory Mapping

The MSP430F5xx family memory space has changed significantly from the MSP430F2xx and MSP430F4xx device families. Changes were required to support future peripheral expansion, increased memory options, and future extensions.

The peripheral space has been expanded up to 4KB to support current peripheral set and future additions. There is no longer byte-only peripheral space. In general, most peripheral registers can be accessed in byte or word formats, however, there are some exceptions.

RAM space now begins at 01C00h for all MSP430F5xx devices. There is a moving boundary between RAM and program space depending on the size of the RAM.

The interrupt vector space still resides up to the upper boundary of the 64-KB address space, however, the number of vectors has been increased to support up to 64 interrupt vectors. All interrupt vectors should be used with symbolic programming, because the order and number of vectors can change from device to device. See the device-specific data sheet for allocated vectors and their priorities.

The bootloader (BSL) memory allocation has been increased to 2KB to support various BSL options, including the capability for a user-generated BSL.

3 Core Modules

The core modules consist of the CPUX, PMM, UCS, SYS, JTAG, and EEM modules. The core remains consistent among all devices in the MSP430F5xx family.

3.1 Central Processing Unit (CPUX)

The MSP430F5xx is based on the CPUX central processing unit that was first introduced on the MSP430xG461x family. The CPUX supports the MSP430X instruction set, which extends the addressable memory range up to 1MB without paging. The CPUX hardware implementation on the MSP430F5xx has slight differences in terms of cycle count compared to the CPUX MSP430F2xx and MSP430F4xx versions. See the CPUX chapter of the MSP430F5xx and MSP430F6xx Family User's Guide for details regarding specific cycle counts.

3.2 Power Management Module (PMM)

The Power Management module is a completely new module. Its primary purpose is to generate a regulated internal core supply voltage from the external primary supply voltage. The majority of the logic on the MSP430F5xx is supplied from this regulated internal core supply, which is restricted on its maximum voltage due to process technology. The MSP430F2xx and MSP430F4xx devices are manufactured using a different process technology, and an onboard regulator is not necessary.

The PMM handles all supervisory and monitoring roles on the primary supply side and the core supply side, and it also provides brownout protection. The supervisors and monitors are highly programmable and can be tailored to the specific application needs with tradeoffs between response time and power dissipation.

The PMM also can be used to set one of four core supply voltages dynamically. This gives the application the capability to reduce power consumption when maximum processing performance is not required or when minimal standby power consumption is critical.

3.3 Unified Clock System (UCS)

The UCS is most similar to the MSP430F4xx FLL+ Clock module. Like the MSP430F4xx module, the UCS is based on a frequency locked loop (FLL). Although the FLL can be run open loop like its predecessor, it is normally run closed loop. The MSP430F5xx introduces a new low-frequency on-board oscillator called REFO. REFO is a trimmed 32-kHz source and can be used as a reference source into the FLL. This gives the user a very flexible, crystal-less system.

The UCS contains several clock sources that can be used as inputs into the clock system. This includes XT1, similar to LFXT1 in the MSP430F4xx, which can accept external watch crystals (32768 Hz) in low-frequency mode or 4-MHz to 32-MHz crystals in high-frequency mode. In addition, XT1 can accept a digital input source in bypass mode. Many devices contain an optional XT2 that is identical in function and performance to XT1 in high-frequency mode. Inherited from the MSP430F2xx family, the MSP430F5xx UCS contains the VLO, which is a very low-power oscillator (12 kHz typical) that can be used as a crystal-less alternative for less time-critical applications.

As in all MSP430F2xx and MSP430F4xx devices, there are three system clocks available – ACLK, MCLK, and SMCLK. For the MSP430F5xx, there is no differentiation between these three system clocks in that any of the clock sources available can be used as a source to any or all of the three system clocks. For example, ACLK can be sourced by XT1, XT2, or the DCO. Therefore, the clock system is very orthogonal with respect to clock sources and their distribution into the clock system. ACLK, MCLK, and SMCLK behave the same as in the MSP430F2xx and MSP430F4xx with respect to their enabling/disabling across the low-power modes.

Fault logic is available for XT1 and XT2 as in the MSP430F2xx and MSP430F4xx. One major difference is the handling of a low-frequency crystal fault. For the MSP430F5xx, any 32-kHz crystal fault causes the respective system clock that is sourced by the crystal to switch automatically to the REFO clock source. This allows for the system to continue to behave as close as possible prior to the fault condition. Fault flags detected in the UCS are not automatically cleared as in previous MSP430F2xx and MSP430F4xx devices and must be cleared by the user, even if the fault condition ceases to exist.

It is important to note that on all MSP430F5xx devices, the crystal input and outputs of XT1 and XT2 (when available) are shared with general-purpose I/O ports. The default reset condition on these pins is general-purpose input ports. This differs from the MSP430F4xx, which does not share the crystal pins, and the MSP430F2xx, which defaults to crystal operation when shared.

3.4 System Module (SYS)

The System module is a new module and consolidates several system-related functions available on older families with the addition of some new features. Also included in SYS is the watchdog timer, WDT_A.

SYS handles all reset and NMI functions. Reset sources include BOR, POR, and PUC as found on previous device families. Resets now share a single interrupt vector word generator to ease the handling of these events, which is new to the MSP430F5xx family. The NMI function is further divided into User NMI and System NMI, where there is no such classification on the MSP430F2xx and MSP430F4xx families.

System NMI events include those associated with the PMM, vacant memory access, and JTAG mailbox. System NMI share a single interrupt vector word generator to ease the handling of these events. All of these are new to the MSP430F5xx family.

User NMI events include those associated with the $\overline{\text{RST}}$/NMI, oscillator faults, and flash access violations. User NMI share a single interrupt vector word generator to ease the handling of these events, which is new to the MSP430F5xx family.

The SYS module also handles device descriptors. Device descriptors are tables that can be accessed that completely describe the device (for example, its type, revision, and available peripherals) This is useful for embedded systems that may adjust its drivers pending what is available in the system. These tables can also be used by various tool sets to configure tools appropriately based on a particular device feature set.

The watchdog timer, WDT_A has been expanded to a 32-bit timer. A change was made in the fail-safe logic so that if the ACLK or SMCLK watchdog timer clock source fails, the VLO automatically becomes the WDT timer source. All other functionality behaves the same as the MSP430F2xx and MSP430F4xx WDT+.

All MSP430F5xx devices contain boot code that is executed any time a BOR condition exists. The purpose of the boot code is to perform any device calibration such as oscillator or reference adjustment, as well as checking for user-defined BSL sequences. The boot code is fully protected from inadvertent access.

The JTAG mailbox system is new to the MSP430F5xx. The mailbox system provides a simple means of communication to the CPU via the standard JTAG interface. Messages can be transferred to and from the application via JTAG in and out boxes. The mailbox system can be used for many purposes, but primary usages include password entry for software security fuse, fast flash programming, and runtime data exchange.

3.5 JTAG Enhanced Emulation Module (JTAG/EEM)

The MSP430F5xx supports both four-wire JTAG and two-wire Spy-Bi-Wire modes for interface for testing. As in former devices with Spy-Bi-Wire, a specific sequence on the TEST/SBWTCK and $\overline{\text{RST}}$/NMI/SBWTDIO pins enables four-wire JTAG, Spy-By-Wire, or BSL.

The MSP430F5xx family supports the Enhanced Emulation Module similar to those offered on MSP430F2xx and MSP430F4xx families. It also includes additional features such as cycle counters, state storage to specific memory locations, EEM version number, and event signaling on the TDO pin.

The JTAG pins are shared with general-purpose I/O, which differs in most MSP430F2xx and MSP430F4xx families. The default at power up is general-purpose high-impedance inputs. Care must be used to ensure that if JTAG is not utilized in the end application, these pins be configured properly to prevent floating inputs.

4 Peripheral Modules

4.1 Timer_A

The Timer_A functionality is fully compatible with previous Timer_A offerings on the MSP430F2xx and MSP430F4xx families. An additional register (TAEX0) has been added, which contains three additional control bits, IDEX. The IDEX bit settings divides the timer input clock source (/1 through /8). This was necessary to support selection of clock sources of 25 MHz or higher into the timer module. The default setting is /1 to be compatible with the older Timer_A module.

A slight change was made to the interrupt vector generator. The vector associated with TAIFG now resides at offset of 0Eh regardless of the number of capture compare channels available for a given Timer_A module. This provides consistency across all timer modules in that the TAIFG always is at the same offset location.

4.2 Timer_B

The Timer_B functionality is fully compatible with previous Timer_B offerings on the MSP430F2xx and MSP430F4xx families. An additional register (TBEX0) was added, which contains three additional control bits, IDEX. The IDEX bit settings divides the timer input clock source (/1 through /8). This was necessary to support selection of clock sources of 25 MHz or higher into the timer module. The default setting is /1 to be compatible with the older Timer_B module.

A slight change was made to the interrupt vector generator. The vector associated with TBIFG now resides at offset of 0Eh regardless of the number of capture compare channels available for a given Timer_B module. This provides consistency across all timer modules in that the TBIFG is always at the same offset.

4.3 RTC_A

The RTC_A module is based on the MSP430F4xx RTC module. The RTC_A module combines the Basic Timer 1 module and the RTC module into one module. The primary purpose of the RTC_A module is for real-time clock operation, but it can be used as general-purpose timer.

Enhancements include a user programmable alarm as well as calibration logic.

4.4 DMA

The DMA functionality behaves as in the MSP430F4xx devices. The DMA module has been expanded to support up to eight DMA channels. For the MSP430F5xx, the triggers and their locations can change depending on the device, so the trigger list and locations are in the respective device data sheets. Also, the DMAONFETCH feature has been removed and been replaced with DMARMWDIS feature. When set, DMARMWDIS prevents any DMA transfer from occurring during a read-modify-write operation of the CPU. All other features of the DMA remain the same as previous devices.

4.5 MPY32

The MPY32 is an expansion of the MPY module seen on MSP430F2xx and MSP430F4xx devices and can support 32-bit multiplication. The MPY32 continues to support all the operations available on the MPY module, as well as maintaining its original register set. The MPY32 expansion includes the capability to handle fractional multiplication using Q formats. In addition, saturation mode was added to prevent overflows and underflows.

4.6 Universal Serial Communication Interface (USCI)

The USCI retains the same functionality as in previous offerings. Changes were made to the register mapping to support byte and word access. Additionally, the interrupts were enhanced to include two interrupt vector generator words, one for the USCI_A and one for the USCI_B. This eases the interrupt handling for each of these modules. Additionally, all interrupt enables and associated flags are logically grouped together. All other features remain the same as previous USCI modules.

4.7 Digital I/O

The Digital I/O has been expanded to include the pullup and pulldown features of the MSP430F2xx family. Each port now contains resistor enable registers (PxREN) for this feature. In addition, the MSP430F5xx supports two output drive settings – low or high drive strength. The output drive strength is set using the PxDS registers. Using low drive strength, whenever possible, helps to reduce unwanted noise. The default setting is low drive strength.

All ports are grouped as pairs of byte-wide ports. Ports can be accessed in byte-wide or word-wide formats. This capability is not available on most MSP430F2xx and MSP430F4xx families.

Interrupt vector generators for Port 1 and 2 have been added, P1IV and P2IV. The interrupt vector generator behaves the same as those seen on MSP430F2xx and MSP430F4xx families on various modules (Timer_A, Timer_B), only now applied to Port 1 and Port 2. This feature is not available on MSP430F2xx and MSP430F4xx families. Any Port 1 or 2 interrupt event that is enabled generates a PC offset that resides in the P1IV or P2IV. This offset can be added to the PC to create a form the basis for simple interrupt handler. Future MSP430F5xx offerings will include additional interrupts on ports other than Ports 1 and 2.

It is important to note that on all MSP430F5xx devices, the crystal input and outputs of XT1 and XT2 (when available) are shared with general-purpose I/O ports. The default reset condition on these pins in general-purpose input ports. This differs from the MSP430F4xx, which does not share the crystal pins, and the MSP430F2xx, which defaults to crystal operation when shared.

4.8 Cyclic Redundancy Check (CRC-CCITT)

The CRC-CCITT module is a new module in the MSP430F5xx and can produce a signature for a given sequence of memory data bus values. This can be used to check memory contents or to create checksums for data validation.

4.9 ADC12_A

The ADC12_A is an improved version of the ADC12 found on many MSP430F2xx and MSP430F4xx devices. Functional enhancements include an improved reference with burst mode (similar to the ADC10) and support of different output formats. Parametric performance including power and linearity have been improved. All other features remain the same as the ADC12.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from June 5, 2008 to September 26, 2018	Page
• Formatting and editorial changes throughout document	1

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