

Smart Selection of ADC/DAC Enables Better Design of Software-Defined Radio

Sanjay Pithadia

HPA - High-Speed Data Converters

ABSTRACT

This application report explains different aspects of selecting analog-to-digital and digital-to-analog data converters for Software-Defined Radio (SDR) applications. It also explains how ADS61xx ADCs and the DAC5688 from Texas Instruments fit properly for SDR designs.

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1 Introduction to Software-Defined Radio

A Software-Defined Radio (SDR) system is a radio communication system, a combination of hardware and software technologies, that allows reconfiguration of wireless network architectures. The Joint Tactical Radio System (JTRS) program sponsored by the U.S. Department of Defense to develop the next generation of military communication devices envisions the use of SDR technology with standardized hardware capable of handling multiple protocols used by the military today.

SDR is a design philosophy that has been in existence for a long time and is going through a rebirth as a result of advanced semiconductor components now available, including high-performance digital signal processors and gate arrays, and high-speed data converters as well as advanced radio technologies. Although advances in DSP technologies have accelerated SDRs development, the main component that enables SDR is in the analog domain of high-speed data converter technologies.

A software-defined radio receiver uses an analog-to-digital converter (ADC) to digitize the analog signal in the receiver as close to the antenna as practical, generally at an intermediate frequency (IF). Once digitized, the signals are filtered, demodulated, and separated into individual channels. Similarly, a software-defined radio transmitter performs coding, modulation, etc. in the digital domain. In the final output IF stage, a digital-to-analog converter (DAC) is used to convert the signal back to an analog format for transmission.

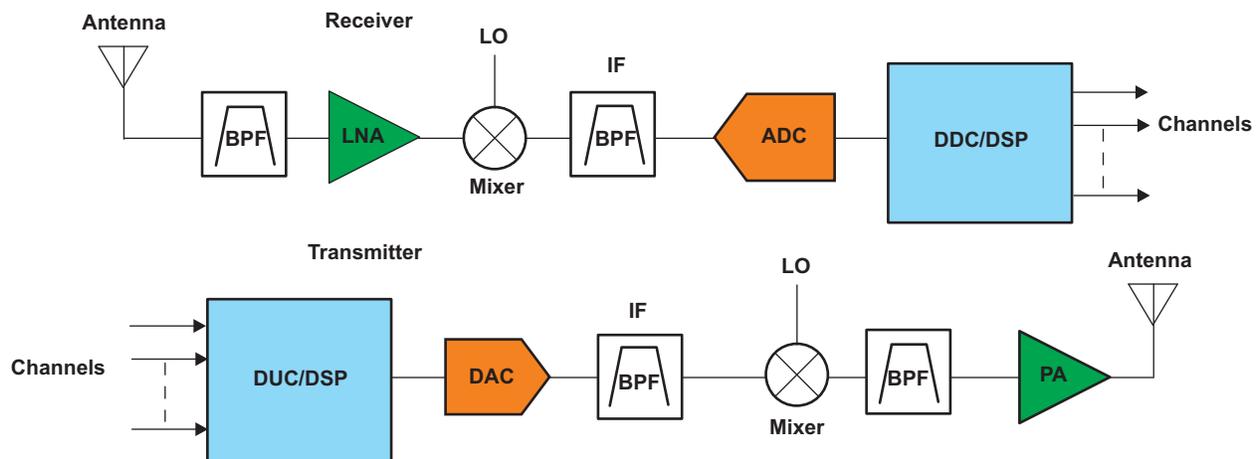


Figure 1. Software-Defined Radio Receiver and Transmitter

ADC and DAC components often make or break an SDR system. In general, as speed goes up, resolution goes down. Higher conversion rates allow more bandwidth to be digitized, but higher-resolution converters provide more dynamic range (the difference in amplitude between the strongest and weakest signals that can be simultaneously digitized). A communications system designer may want to carry as much bandwidth as possible, but high usage of the spectrum of interest is likely to include strong interfering signals as well as weaker signals of interest. The dynamic range requirement imposed by the different signal amplitudes likely defines the number of bits required. For example, suppose a small signal (carrier) needs to be recovered in the presence of a much larger signal (interference) and all signals of interest lie in a 40-MHz bandwidth (Figure 2). The dynamic range required to do this is the difference in signal amplitudes (60 dB) plus an adequate operating margin to demodulate the signal, perhaps 10 dB. Sampling theory dictates that the sampling frequency must be at least twice the signal bandwidth. These requirements can be satisfied by a good quality, 14-bit ADC which, when sampled at 100 MHz, provides a dynamic range of at least 80 dB.

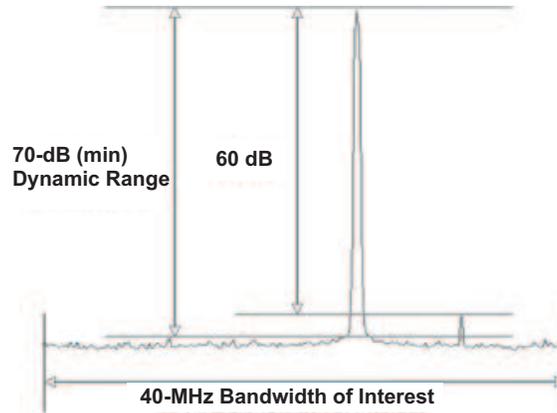


Figure 2. Dynamic Range When Carrier and Interference Both Are in Band of Interest

Converter performance can be divided into Nyquist zones. The Nyquist criterion states that the sample rate must be at least twice the signal bandwidth in order to faithfully represent the signal when sampled. With this in mind, one can see that an ADC has many different analog input ranges that can be used to satisfy Nyquist. The most common is the first Nyquist zone, which goes from DC (0 dB) to one half of the clock rate. Any signal or group of signals residing wholly within this range when sampled meets the Nyquist criterion. However, the same is true for signals that reside between one half of the clock rate and the clock rate. This is called the second Nyquist zone. This pattern continues for each multiple of one half of the clock rate. A unique and useful effect of using the higher Nyquist zones is that signals sampled in the higher zones are mirrored down to the first Nyquist zone once digitized, thus forming the basis of a mixer and a digitizer.

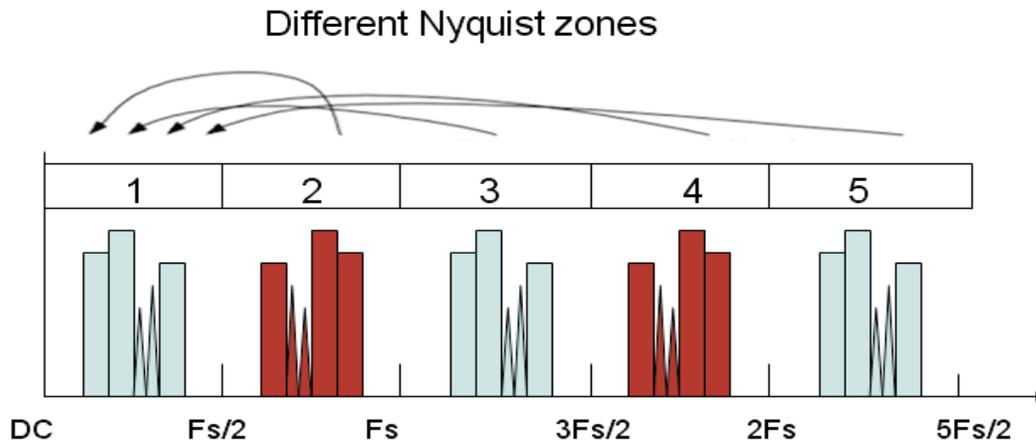


Figure 3. Nyquist Zones

2 Selection of Analog-to-Digital Converters

Intermediate Frequency sampling is the process of sampling signals that are not at baseband, i.e., not centered around DC. Depending on the system involved, IF frequencies can be up to several hundred megahertz. Current ADC technology allows sampling of these frequencies with each generation of converters providing improvements in performance. In general, converter performance begins to degrade with increasing input frequency. Converter performance limitations occur in two primary areas. Within the converter, performance is limited by the slew rate of the on-chip analog circuitry. Analog slew rate limitations result in a reduced SFDR performance as the input frequency is increased (see Figure 4). The other limitation to IF sampling is jitter on the sample clock. This limitation is due to external factors, so the combination of internal and external factors results in reduced SNR performance as the input frequency is increased.

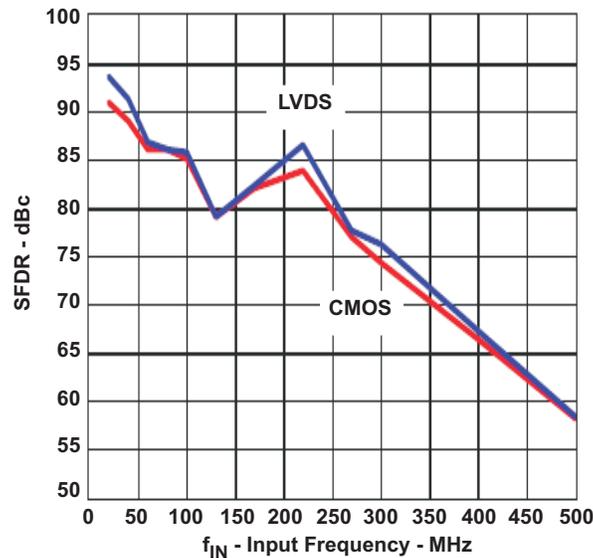


Figure 4. SFDR Degradation vs Analog Input Frequency

2.1 SFDR and SNR Considerations

Two of the most important performance requirements to consider are the noise contribution and the Spurious Free Dynamic Range (SFDR) of the ADC. A high-IF architecture is desirable from a receiver-hardware commonality perspective, but it places an added burden on the ADC for wide dynamic range, which typically determines the performance of the system. In a cellular infrastructure, for example, receivers must process very low-level signals (≤ 100 dBm) in the presence of high-power blockers (-13 dBm or -26 dBm in the case of GSM 800/900 and 1800/1900, respectively). Thus, the ADC must have wide SFDR and SNR to meet the receiver's needs for this protocol.

As the signal moves through the receiver signal chain leading up to the ADC, one thing that must be considered is how the amplifiers and the mixers of the receiver signal chain contribute to the overall noise of the system. The noise requirements placed on the ADC are very high.

For an ADC, SFDR is defined as the ratio between the rms amplitude of the single tone and the rms amplitude of the worst spur. Because the SFDR requirements for narrowband air standards are so demanding, it is desirable to achieve the best possible SFDR from the ADC. One technique that is used to improve SFDR is dither. Dither is pseudo-random noise injected into the analog input of the converter. Also, new analog structures using cutting-edge BiCMOS process technologies have enabled the inclusion of an analog input buffer, capable of delivering high levels of SFDR across many hundreds of MHz and isolating input from kick-back and disturbances.

2.2 How to Select the Sampling Rate

The selection of sampling rate is also important for ADCs. Fast encode clocks offer the advantage of making analog filtering significantly easier. Given a fixed signal bandwidth, a higher encode rate increases the allowable transition band. This allows lower order filters to be used to reduce cost, or, if higher order filters are still used, greater stop band rejection can potentially be realized (see [Figure 5](#)).

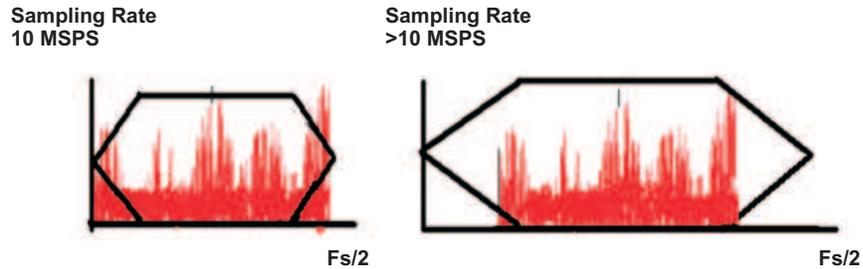


Figure 5. Transition Band Increases as Sampling Rate Increases

Another advantage with increasing clock speeds is processing gain. Processing gain is achieved when the signal of interest is oversampled and then digitally filtered. Processing gain occurs when noise outside the band of interest is digitally removed, which results in improved in-band SNR. Processing gain can be easily determined using Equation 1. This equation determines the increase in SNR over and above the SNR of the converter alone.

$$\text{Processing Gain} = 10\log_{10} (\text{Half of the sample rate} / \text{filter BW}) \quad (1)$$

Also, when selecting the sampling rate, the user must consider the second and third harmonics (HD2 and HD3). These harmonics must lie outside the band of interest. These can be filtered using the digital filter inside the DDC/DSP. That means, frequency planning also becomes important when designing a SDR system.

2.3 Jitter Effect

A significant consideration for any high-speed communications system is the generation of ultralow-jitter, high-speed sampling clocks, and their effect on the data conversion process. Clock jitter is defined as the random variation of the clock position compared to its ideal position with respect to time. Clock jitter has two basic components. One originates from the external clock source; the ADC's clock circuitry creates the other internally. When the position of the clock varies slightly, it alters the position of the sampling point, which in turn samples the input waveform at an imprecise location. This error manifests itself as SNR degradation:

$$\text{SNR} = -20\log_{10} (2 \pi f_{in} t_{\text{jitter}}) \quad (2)$$

where f_{in} is the incoming signal's frequency to be sampled by the data converter, and t_{jitter} is the sampling system's rms jitter. Figure 6 shows the comparison of measured and calculated (using Equation 2) SNR.

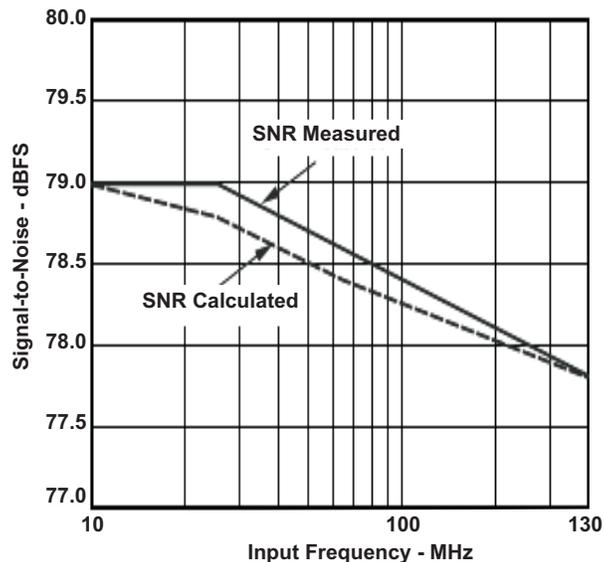


Figure 6. Comparison of Measured and Calculated SNR

2.4 Two-Tone Intermodulation Distortion (IMD)

The Software-Defined Radio may be used in military applications where it is possible that the application uses two different sine wave tones with different phases and amplitudes. These two tones can generate Intermodulation Distortion (IMD), which can override the smaller amplitude signals of the application. These distortions cannot be removed.

When selecting an ADC, the IMD of ADC must be very low as IMD directly gives an idea of Adjacent Channel Power Ratio (ACPR) of the device.

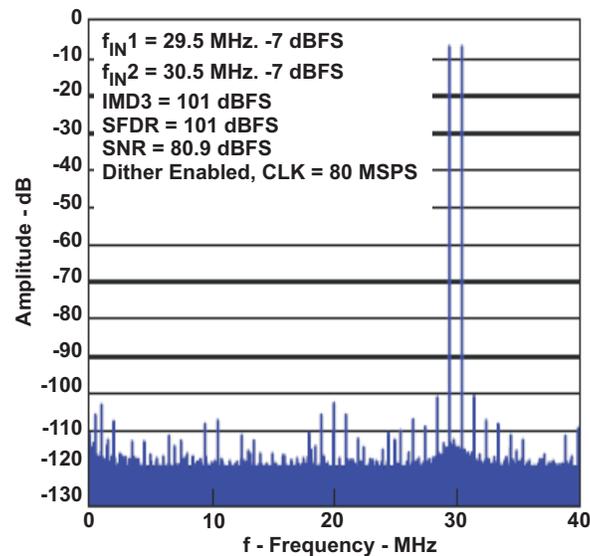


Figure 7. Two-Tone IMD

2.5 Use of ADS61xx ADC in SDR Application

The ADS61xx series of ADCs are dual-channel, 14-bit and 12-bit analog-to-digital converters with sampling rates up to 250 MSPS. It combines high dynamic performance and low power consumption which makes it suitable for multicarrier, wide bandwidth communications applications like SDR. The ADS61xx has fine gain options that can be used to improve the SFDR performance at low full-scale input ranges. The analog input bandwidth is as high as 700 MHz. The SNR value reaches a number of ~73 dB whereas SFDR is also high up to 88dBc. The main characteristic of two-tone IMD is typically 91dBc.

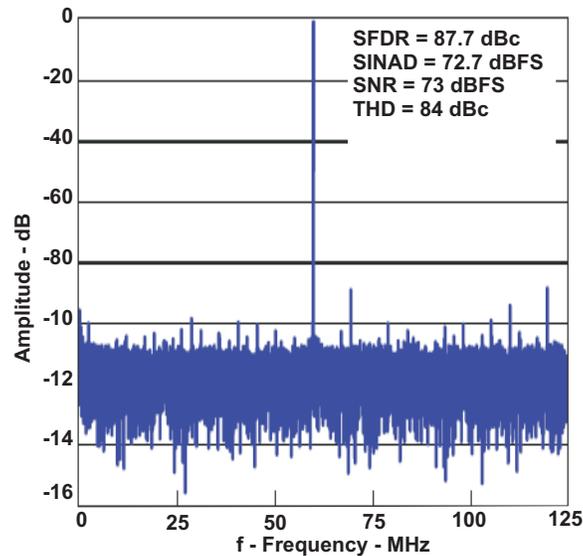


Figure 8. ADS6149 Performance at Input Frequency = 60 MHz

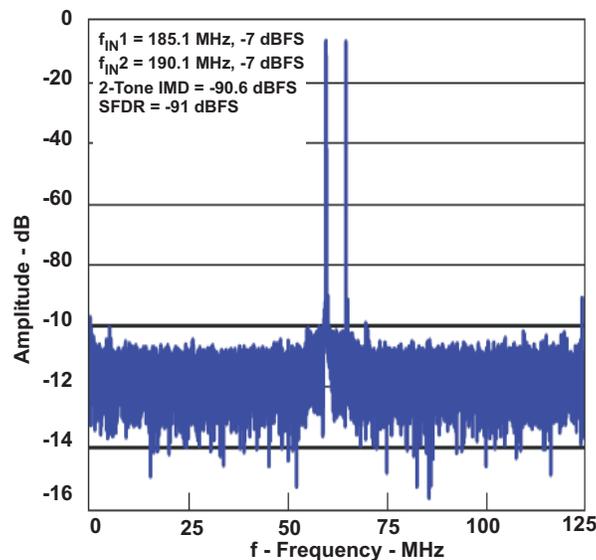


Figure 9. Two-Tone IMD Performance for ADS6149

3 Selection of Digital-to-Analog Converters

As the ADC may be thought of as the heart of an SDR receiver, in like manner, the DAC may be seen as having the same importance in the transmitter section of the SDR. Key specifications to consider when selecting the DAC are SNR, ACLR (Adjacent Carrier Leakage Ratio), and multitone intermodulation. If the DAC also has digital functionalities that is an added bonus. Finally, the designer must consider low power consumption when designing any system to improve the system power efficiency.

3.1 SNR and ACLR Considerations

When considering the performance of a DAC used in SDR applications, the first specification of interest is the signal-to-noise ratio (SNR). SNR is primarily determined by quantization and thermal noise. If either is too large, then the noise figure of the DAC begins to contribute to the overall signal chain noise. Although noise is not necessarily a concern spectrally, the issue becomes important when the DAC is used to

reconstruct multiple signals. In this case, the DAC output signal swing (*power*) is shared among the carriers. The Adjacent Carrier Leakage Ratio (ACLR) of any general-purpose RF device (whether a mixer, amplifier, isolator, or other device) is frequently dominated by the third-order intermodulation distortion (IM3) of the device. That means, the IMD3 components must be lower for the DAC for better SDR design. This specification becomes more important when multiple carrier signals are considered, e.g., a 3GPP W-CDMA signal.

3.2 Bandwidth Requirements

Considering the transmitter architecture in detail (as shown in the [Figure 10](#)), one sees that the digital mixing of I (in-band) and Q (quadrature) signals takes place, and then the modulated signals are sent to the DAC. In this case, the bandwidth requirements of DAC are more stringent. To get good performance from the transmitter, the bandwidth must be very high.

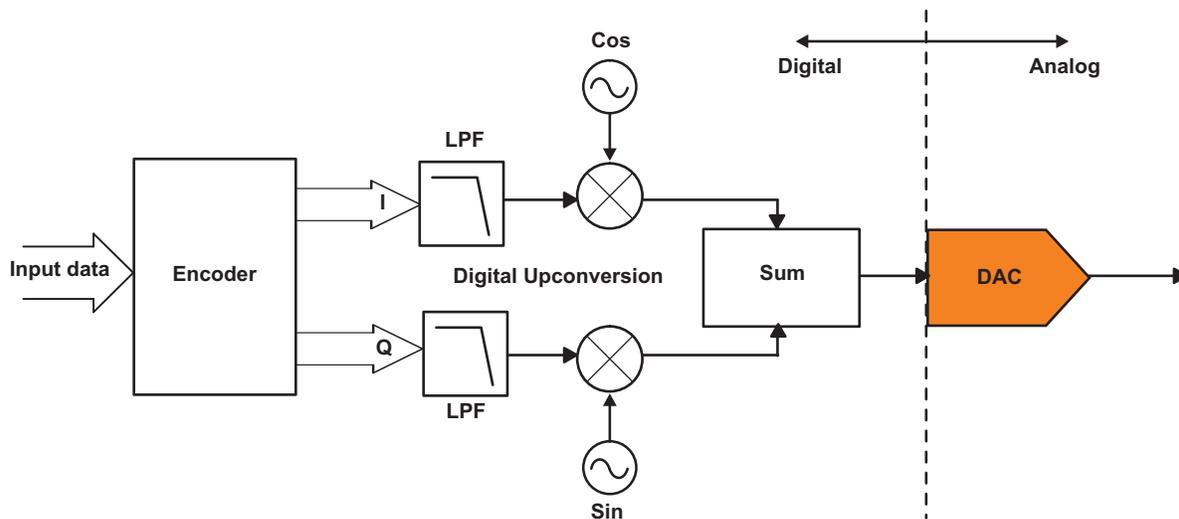


Figure 10. Digital Upconversion Takes Place Before the Data Goes into DAC

If multiple digital I and Q modulators are fed into a single DAC, the system becomes a wideband multicarrier transmit architecture, for which the superior multitone performance of the DAC is a major factor.

3.3 Digital Functionalities in High-Speed DACs

High-performance DACs with digital functionalities provide an increased level of flexibility when implementing common IF schemes. Some of the important functionalities include interpolation filters, fine and coarse digital mixers, $\sin(x)/x$ compensation, quadrature modulation compensation, etc.

1. Interpolation allows increased sampling rates in the digital domain while driving the input data at a lower rate, but it also adds undesired spectral images to the signal at multiples of the original sampling rate. So, interpolation filters attenuate the images created by up-sampling which results in an improved update rate-to-output frequency ratio for DAC and more accurate waveform reconstruction. Interpolation also helps in getting lower overall cost by oversampling the signal to reduce DACs in-band aliased images, thus easing the complexity of analog band-pass filter.
2. The fine (NCO controlled) and coarse (F_{clk}/n) mixers can be combined to span a wider range of frequencies with fine resolution. Also, they result in an increased degree of frequency-placement freedom while signals still are in the digital domain.
3. The sample-and-hold circuits in DAC sets the output current of DAC and holds it for one DAC clock cycle until the next sample, resulting in the well-known $\sin(x)/x$ or $\text{sinc}(x)$ frequency response. The inverse sinc filter flattens the frequency response of sample-and-hold output. It runs at DAC update rate (f_{DAC}). Although $\sin(x)/x$ compensation allows for higher frequency placement, it slightly reduces power in the bandwidth of interest and SNR performance.
4. The IQ compensation in digital domain allows optimization of phase, gain, and offset to maximize

sideband rejection (further reducing filters) and minimize LO feedthrough for an analog quadrature modulator. (A complex IF architecture allows for quadrature signals, and it eases analog-domain filtering requirements. During the mixing process, if the phase information is available, then it permits the arithmetic cancellation of signals. This process highly reduces the power of mixing products. The real IF implementations have full power mixing images, unlike complex IF type).

3.4 Use of DAC5688 in SDR Applications

The DAC5688 is dual-channel, 16-bit, 800-MSPS, digital-to-analog converter (DAC) with dual CMOS digital data bus, integrated 2x-8x interpolation filters, a fine frequency mixer with 32-bit complex numerically controlled oscillator (NCO), onboard clock multiplier, IQ compensation, and internal voltage reference. The user can either enable or bypass various signal processing blocks in different modes of operation.

The DAC5688 input data can be interpolated 2x, 4x or 8x by onboard digital interpolating FIR filters with over 80 dB of stop-band attenuation. The DAC5688 allows both complex and real outputs. An optional 32-bit NCO/mixer in complex mode provides frequency upconversion and the dual DAC output produces a complex Hilbert Transform pair. A digital inverse sinc filter compensates for natural DC $\sin(x)/x$ frequency rolloff. The digital Quadrature Modulator Correction (QMC) feature allows IQ compensation of phase, gain, and offset to maximize sideband rejection and minimize LO feedthrough of an external quadrature modulator performing the final single sideband RF upconversion.

The functional block diagram of DAC5688 is shown in Figure 11.

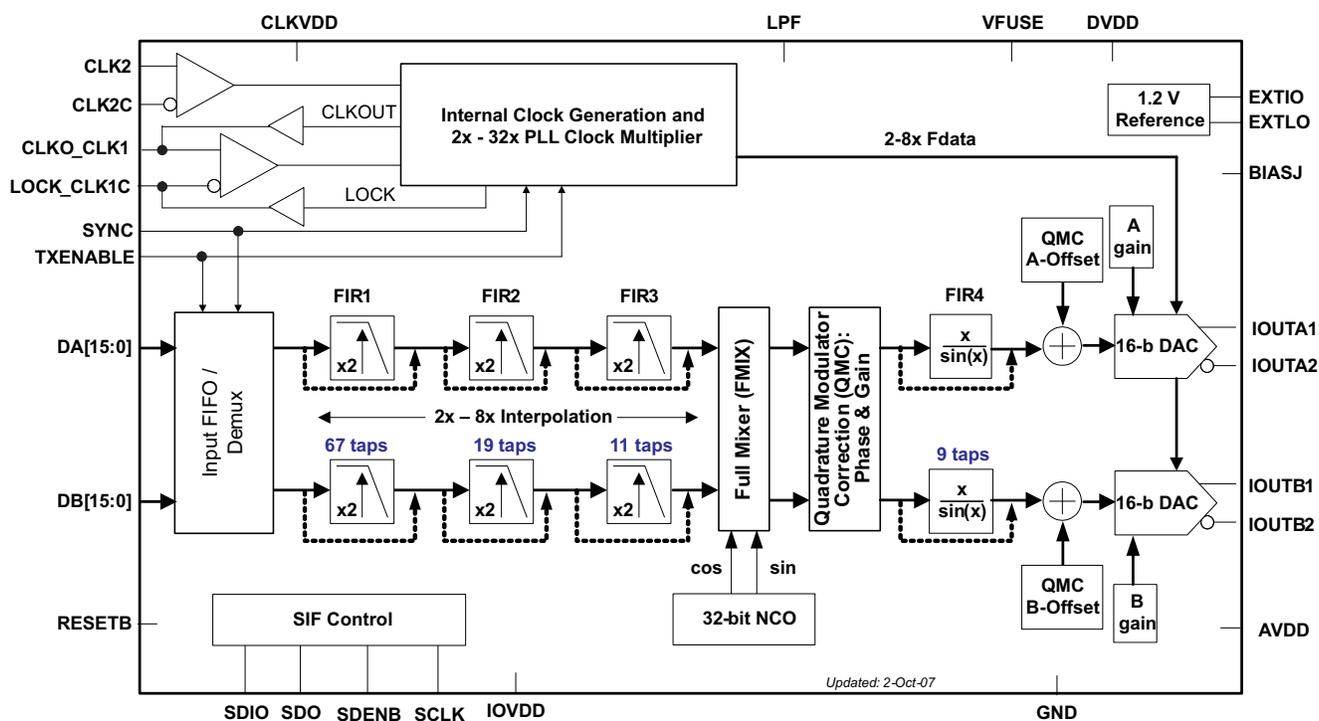


Figure 11. Functional Block Diagram of DAC5688

The DAC5688 has a noise floor of -161 dBm/Hz. The SNR is as high as 72 dBc (for 4x interpolation and PLL off condition). The in-band and out-of-band SFDR graphs for DAC5688 are shown in Figure 12.

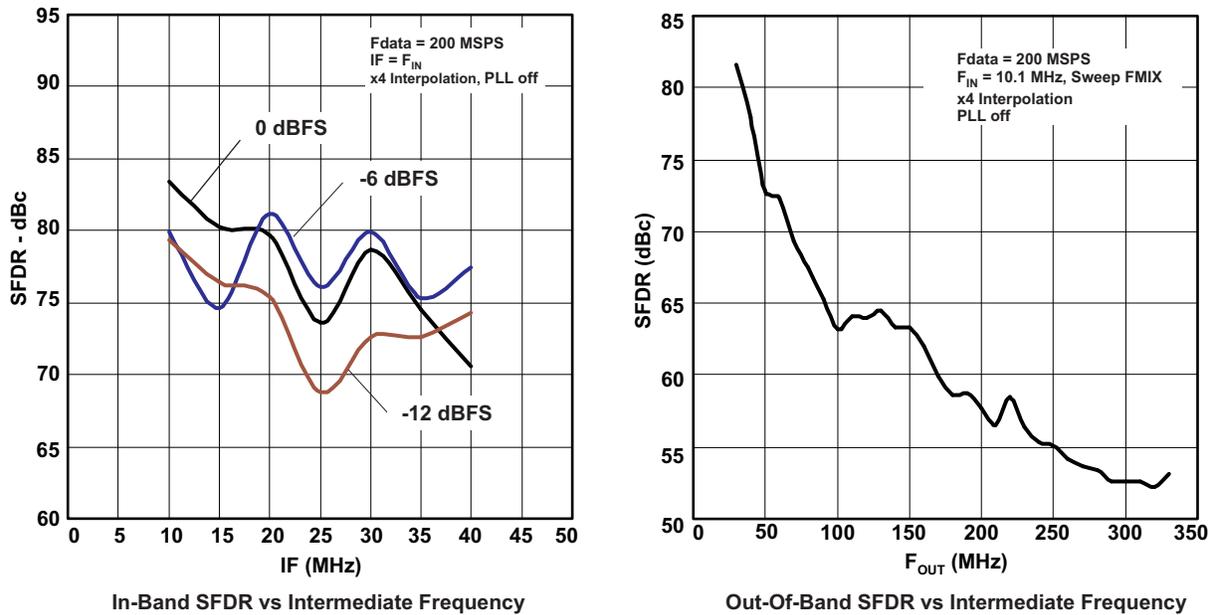


Figure 12. In-Band and Out-of-Band SFDR

The third-order, two-tone intermodulation is 85 dBc and four-tone intermodulation to Nyquist is 73 dBc. The powers versus frequency spectrums for four-carrier signals are shown in Figure 13.

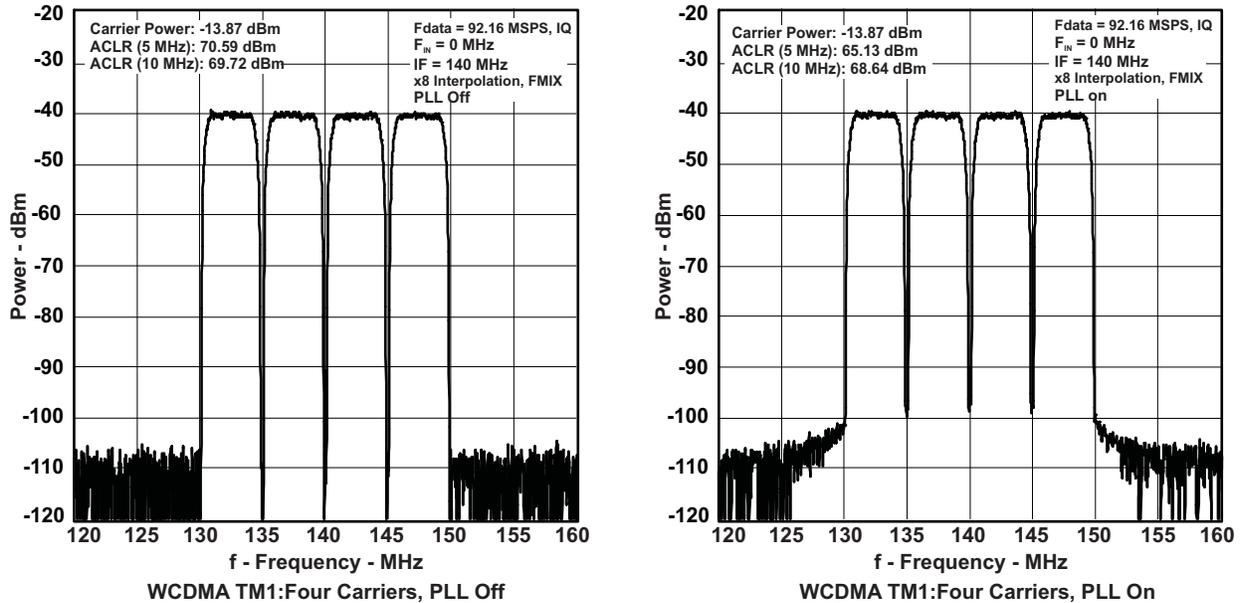


Figure 13. Four-Tone Intermodulation of DAC5688

A ratio in dBc between the measured power within a channel relative to its adjacent channel is known as ACLR (Adjacent Channel Rejection Ratio). For the DAC5688, ACLR with PLL on and PLL off conditions is as given in Figure 14. Here it is defined for a 3.84-Mcps, 3GPP W-CDMA input signal measured in a 3.84-MHz bandwidth at a 5-MHz offset from the carrier with a 12-dB peak-to-average ratio.

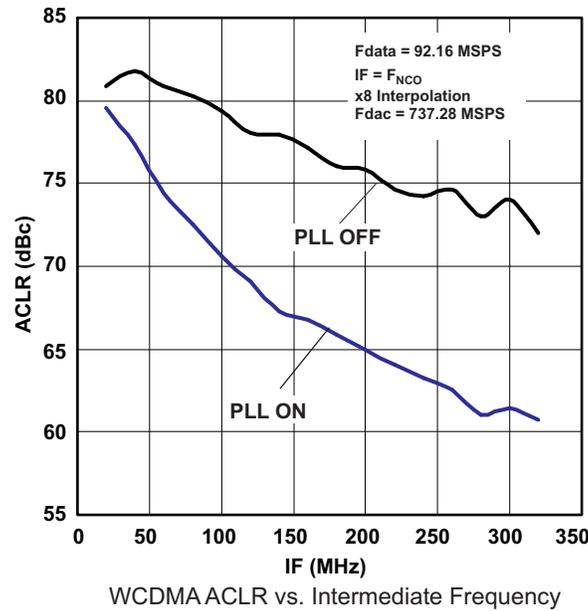


Figure 14. ACLR vs Intermediate Frequency for DAC5688

All the digital functionalities explained previously are included in the DAC5688. The DAC5688 provides many different modes of operation. Single-sideband mode provides an alternative interface to the analog quadrature modulators. Channel carrier selection is performed at baseband by mixing in the ASIC/DUC. Baseband I and Q from the ASIC/DUC are input to the DAC5688, which in turn performs a complex mix resulting in Hilbert transform pairs at the outputs of the DAC5688's two DACs. An external RF quadrature modulator then performs the final single-sideband up-conversion. The DAC5688's complex mixing frequencies are flexibly chosen with the 32-bit programmable NCO. In quadrature modulation mode, on-chip mixing provides baseband-to-IF upconversion. Mixing frequencies are flexibly chosen with a 32-bit programmable NCO. Channel carrier selection is performed at baseband by complex mixing in the ASIC/DUC. Baseband I and Q from the ASIC/FPGA are input to the DAC5688, which interpolates the low data-rate signal to higher data rates. The DAC output from the DAC5688 is the final IF single-sideband spectrum presented to RF.

The example system diagram using TI's DAC5688, CDCM7005, TRF3703, TRF3761-X, and GC5016 is as shown Figure 15.

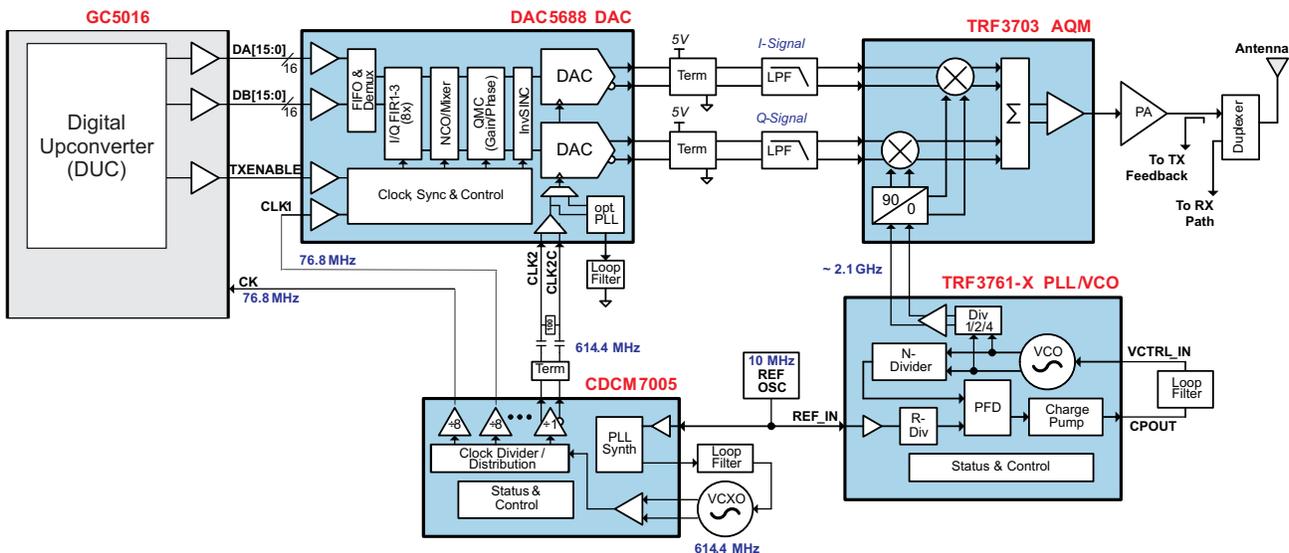


Figure 15. Example System Diagram

3.5 Conclusion

Located at the heart of both the receiver and the transmitter of a Software-Defined Radio system, the ADC and DAC set the performance for the entire radio. As ADC and DAC technologies improve, they will continue to lead the way for higher efficiency, reconfigurable, and multistandard radios.

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