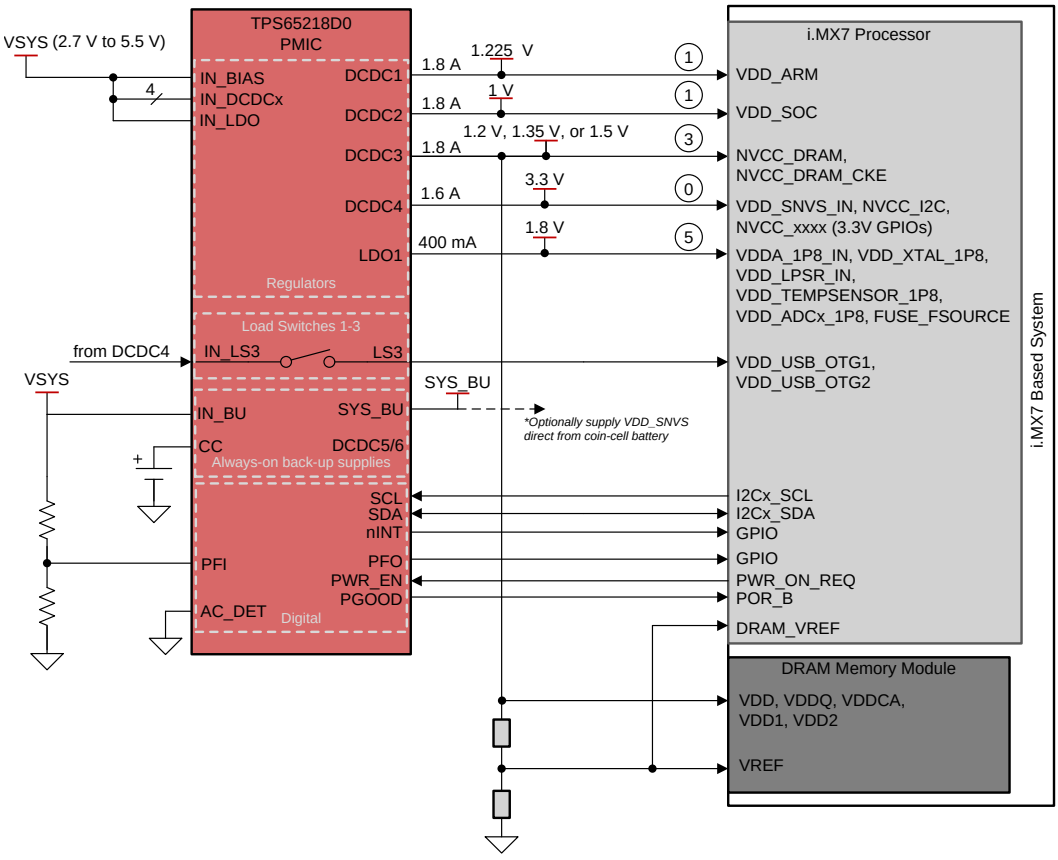
Powering the NXP i.MX 7 processor with the TPS65218D0 PMIC

System Power Block Diagram



Can you change PMICs?

Using a multi-rail power management IC (PMIC) for an applications processor is common, but typically the vendor recommends the PMIC that should be used for each processor. Even if the suggested PMIC is not ideal for the needs of the processor, often the complexity makes it difficult to swap out the PMIC for another solution. The purpose of this tech note is to show that the TPS65218D0 PMIC can provide power for the i.MX 7Solo and 7Dual processors.

Why the TPS65218D0?

The TPS65218D0 device has an input range from 2.7 to 5.5 V, making it appropriate for system-on-module applications powered from a 3.3-V or 5-V DC supply or a Li-Ion battery. The device has four step-down converters that provide the 1.225-V and 1-V power rails required for the ARM® and SoC cores, the 1.2-V (or 1.5-V, 1.35-V) rail required for DDR4 (or DDR3/DDR3L) memory, and a 3.3-V rail required for VDD_SNVS and I/Os. A low-dropout (LDO) regulator provides 1.8-V for VDD_LPSR, the analog domain, and additional I/Os. Three load switches allow for saving battery power in portable applications. The TPS65218D0 automatically sequences these rails in the correct power-up sequence for the i.MX 7Solo and 7Dual processors.

How do you make the switch?

The TPS65218D0 output voltages and sequencing order are determined by an EEPROM-backed register map, which can be programmed using the BOOSTXL-TPS65218 socketed booster pack. Samples of the TPS65218D0RSLR can be programmed during the prototype phase of product development and soldered down on the TPS65218EVM-100 or the prototype PCB of the final product to evaluate the performance of the PMIC. To order pre-programmed samples of the TPS65218D0RSLR for the NXP i.MX 7Solo, 7Dual processor that match this tech note, contact the programming services organization at ARROW.

Table 1. i.MX 7Solo and 7Dual Power Requirements

TPS65218D0				i.MX 7Solo/7Dual		
POWER-UP SEQUENCE	POWER SUPPLY (OUTPUT)	OUTPUT CURRENT [mA]	OUTPUT VOLTAGE [V]	POWER SUPPLY (INPUT)	VOLTAGE RATING [V]	MAX CURRENT [mA]
1	DCDC1	1800	1.225	VDD_ARM	Minimum: 1.2 Maximum: 1.25	500
1	DCDC2	1800	1.00	VDD_SOC	Minimum: 0.95 Maximum: 1.155	1000
3	DCDC3	1800	1.2, 1.35, or 1.5	NVCC_DRAM, NVCC_DRAM_CKE	1.14 (min), 1.3 (max) 1.283 (min), 1.45 (max) 1.425 (min), 1.575 (max)	1000
0	DCDC4	1600	3.3	VDD_SNVS_IN, NVCC_I2C, NVCC_GPIOx, NVCC_SDx, NVCC_xxxx(1)	3.3 V ± 9.09%	I/O current
5	LDO1	400	1.8	VDDA_1P8_IN, VDD_XTAL_1P8, VDD_LPSR_IN, VDD_TEMPSENSOR_1P8, VDDA_ADCx_1P8, FUSE_FSOURCE	1.8 V ± 5%	400
N/A	LS3	500	3.3	VDD_USB_OTG1, VDD_USB_OTG2	3.3 V ± 9.09%	100

(1) NVCC_GPIOx, NVCC_SDx, and NVCC_xxxx represents all processor rails that can operate at 1.8 V and 3.3 V, including NVCC_GPIO1, NVCC_GPIO2, NVCC_SD1-3, NVCC_ENET1, NVCC_EPDC1-2, NVCC_SAI, NVCC_LCD, NVCC_SPI, NVCC_ECSPI, NVCC_I2C, NVCC_UART

Table 2. Adjacent Tech Notes

Processor	Title
i.MX 6Solo and 6DualLite	Powering the NXP i.MX 6Solo, 6DualLite with the TPS65218D0 PMIC
i.MX 8M Mini	Powering the NXP i.MX 8M Mini with the TPS65218D0 and LP8733-Q1 PMICs

References

Texas Instruments, *TPS65218D0 Power Management for ARM® Cortex™-A8/A9 SOCs and FPGAs* Data Sheet

Texas Instruments, *Power Supply Design for NXP i.MX 7 Using the TPS65023* Application Report, Sept. 2017

NXP Semiconductors, *i.MX 7Solo Family of Applications Processors Data Sheet* (IMX7SCEC), Rev. 6, 03/2019

NXP Semiconductors, *i.MX 7Dual Family of Applications Processors Data Sheet* (IMX7DCEC), Rev. 6, 03/2019

NXP Semiconductors, *i.MX 7DS Power Consumption Measurement* Application Note (AN5383), Rev. 0, 11/2016

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