Application Report
SPRA651 - April 2000

Programmable DSP Platform for Digital Still Cameras

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Digital Still Camera Business Unit

ABSTRACT

This article presents a programmable digital signal processor (DSP) platform for digital still cameras based on the Texas Instruments TMS320C54x family. One major advantage of this platform is that, after capturing an image from a charged coupled device (CCD) sensor, processing the raw image, and compressing the image for storage are performed on the DSP. This provides a short shot-to-shot delay and a high degree of flexibility. The system realized also allows instant viewing and selective storing of captured images. This article outlines the various processing stages necessary to take the raw CCD data and produce a JPEG compressed bit stream, and highlights the advantages of DSPs for this application. The programmable nature of this platform allows for the exploration of different image processing and compression techniques. The low-power nature of the DSP provides long battery life.

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This document was originally published in the Texas Instruments Technical Journal, January-March 2000, Volume 17, Number 1.

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1 Digital Photography Market Overview

Digital imaging, capturing, transferring, manipulation, and printing photos digitally came into its own in the early 90's thanks to the foundation laid a decade earlier by desktop publishing. Consumer-friendly printers, scanners, and digital cameras began to hit the market in 1993. Early versions of the Digital Still Camera (DSC) were expensive, poor in quality, and difficult to use.

This scenario has changed in the past few years. Today, dozens of manufacturers produce a variety of compelling solutions. In 1997, the total number of digital cameras sold worldwide reached over 1 million units. This was due to several factors, such as the drop in PC prices, the explosion of the internet and the ability to transfer and share pictures instantaneously, and the advances in VLSI technology.

1.1 Market Segments of Digital Cameras

Initially, digital photography was adopted in the commercial applications: badge printing, Web publishing, real estate, insurance companies, etc. Lately, however, this trend has changed dramatically and the casual home photographers clicking away at baby showers, birthday parties and wedding receptions are becoming the real mother lode. This is due to the drop in price of digital cameras, improved image quality, and a growing infrastructure.

The DSC market has four major segments. Spatial resolution is the major classification for these segments (see Figure 1). These segments are defined as follows:

- **Soft display (PC camera):** These mobile cameras feature spatial resolution around 320x240, making them suitable primarily for soft display-based applications. They offer a limited set of camera features.
- **Basic point-and-shoot (low-end consumer):** These units offer spatial resolution in the VGA range. They deliver a limited set of camera features, equivalent to an entry-level "point-and-shoot" film camera. In addition, various models offer one or more of the following "premium" features: zoom lens, autofocus, autoflash, removable storage, and color LCD screen. The resolution of these cameras ranges from 800 kpixels to 1.0 Mpixels.
- **Photo-quality point-and-shoot (high-end consumer):** These cameras aim to provide the closest possible approximation to 35-mm film image quality at mass-market prices. The units in this category have resolution specifications ranging from 0.8 million to 3 million pixels.
- **Professional:** These cameras are intended to replace 35-mm film cameras in professional news and documentation-gathering applications with high output quality requirements. They feature interchangeable lenses, standard high-end camera bodies and professional controls. Spatial resolution is in the range of 4–8 Mpixels.

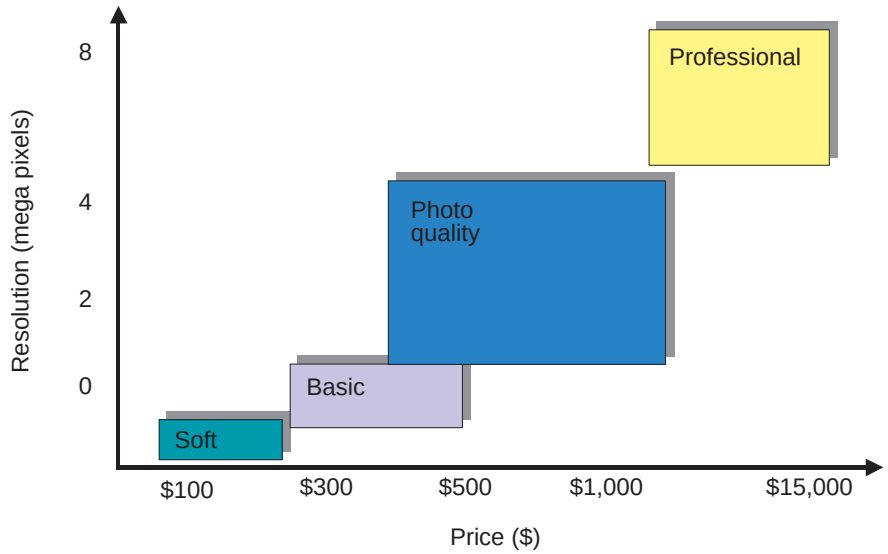

Figure 1. DSC Market Segments

1.2 DSC Market Size and Growth

The worldwide digital camera market grew by 46% in 1998, shipping almost 3.1M units. This growth was driven by the United States and Japan; the two comprised 80% of worldwide shipments in 1998. The United States shipped over 1.1M units while Japan shipped almost 1.4M units in 1998. Western Europe comprised 12% of the market in 1998, shipping just under 400,000 units. Rest-of-the-World (ROW) shipments reached almost 170,000 units and Asia Pacific (excluding Japan) shipped just over 60,000 in 1998. The growth of the consumer segment of the market was driven by megapixel camera shipments in both the U.S. and Japan. It is expected that the worldwide digital camera market will show a 56% shipment compound annual growth rate (CAGR) from 1998–2003 as shown in Figure 2.

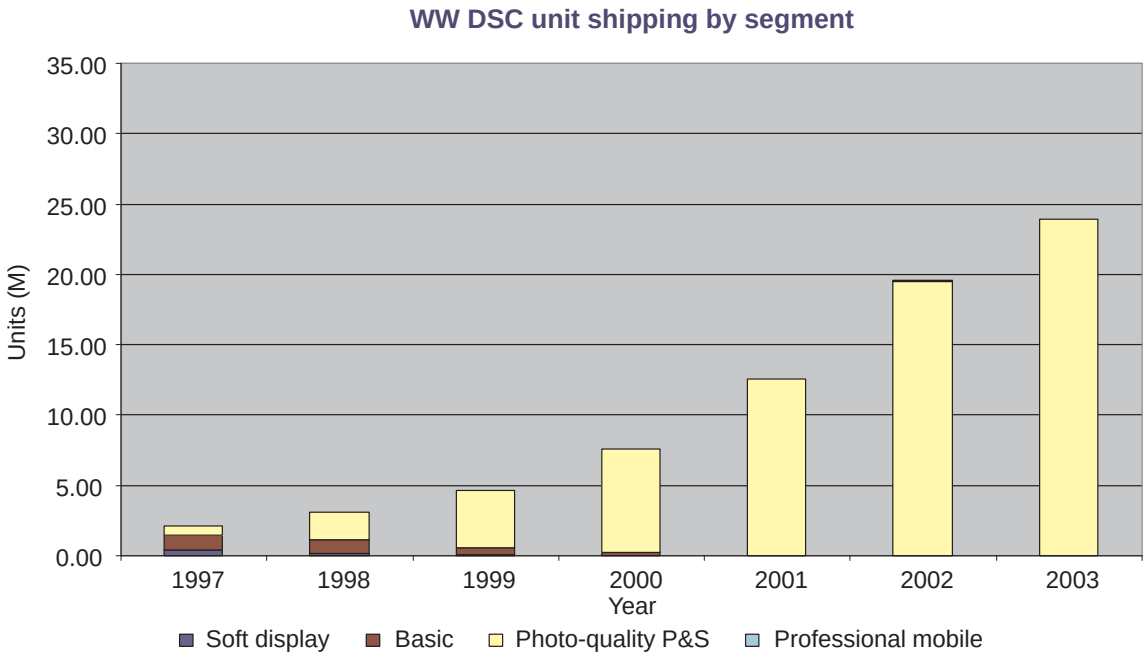

Figure 2. Worldwide DSC Unit Shipment Projection by Technology Segments

2 DSC System

Digital still cameras require a significant amount of silicon contents, including the sensor (CCD or CMOS), the analog components (ADC, NTSC encoder, …) and the engine (DSP), which is the brain of the camera and is responsible for performing all the computations needed to process and compress the image

Figure 3 shows the various functional blocks in a typical DSC system. Most DSCs use a CCD imager to sense the images. The driver electronics and the Timing Generator circuitry generate the necessary signal to clock the CCD. Correlated Double Sampling and Automatic Gain Control electronics are used to get a good-quality image signal from the CCD sensor. This CCD data is then digitized and fed into the DSC engine. All the image-processing and image-compression operations are performed in the DSC engine. On most DSCs, the user has the ability to view the image to be captured on the LCD display. The compressed images are stored in Flash memory for later use. Most DSC systems also provide an NTSC/PAL video signal to view the captured images (also the preview images) on a TV monitor. The current DSCs also provide ways to connect to the external PC or printer through an RS-232 or a USB port. Future DSC systems are expected to be even more versatile with the ability to annotate images with text/speech. Including a modem and TCP/IP interface provides the ability to connect directly to the internet. Future DSCs will also run more complex multitasking operating systems to schedule the various real-time tasks.

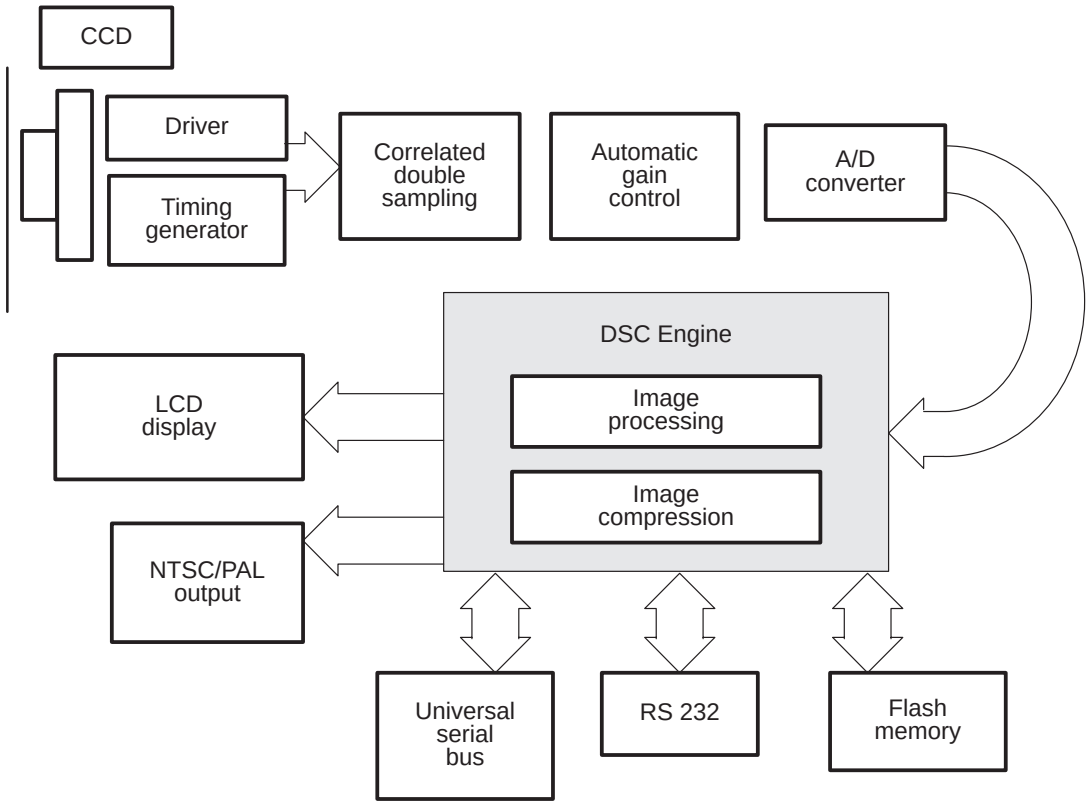

Figure 3. Digital Still Camera Block Diagram

3 Image Acquisition

A typical DSC has to perform multiple processing steps before a high-quality image can be stored. The first step is image acquisition. The intensity distribution reflected from the scene is mapped by an optical system onto the imager. Nowadays, most cameras use CCDs although CMOS imagers are also used in some. The image captured by the CCD sensor has each pixel masked by a color filter to provide a color image. This raw CCD image is normally referred as a Color Filtered Array (CFA). The masking pattern of the CCD array, as well as the filter color primaries, vary among different manufacturers. In DSC applications, the CFA pattern that is most commonly used is an RGB Bayer pattern that consists of 2x2 cell elements that are tiled across the entire CCD-array. Figure 4 depicts a subset of this Bayer pattern in the matrix block following the CCD camera. The output signal of the CCD is digitized with a 10- or 12-bit A/D converter.

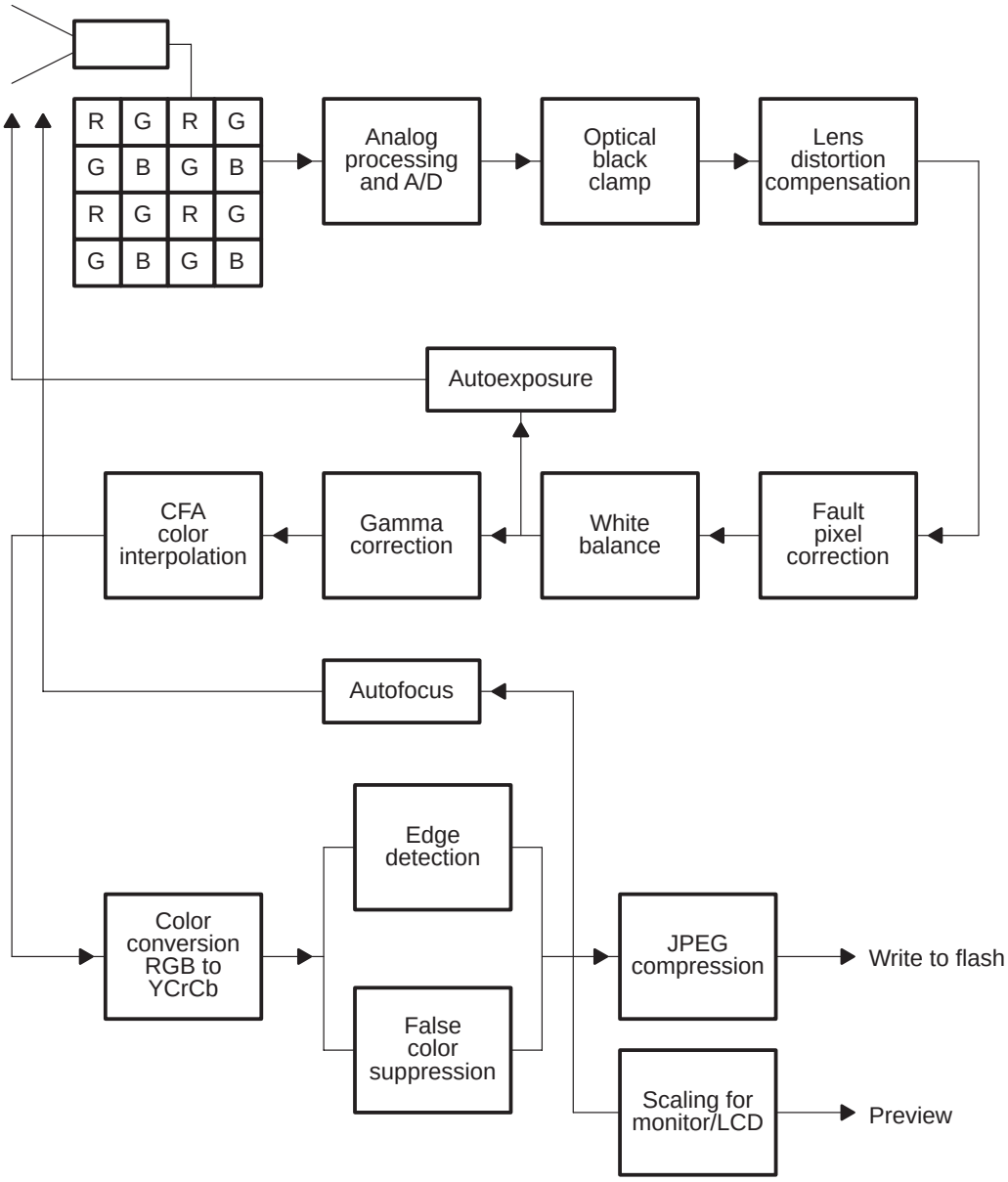

Figure 4. DSC Image Pipeline

4 Image Pipeline

The CFA data needs to undergo significant amount of image processing before the image can be finally presented in a usable format for compression. All these processing stages are collectively called the “image pipeline.” A typical image pipeline in a DSC is shown in Figure 4. As can be seen, a typical DSC has to perform multiple processing steps before a high-quality image can be stored. Most of these tasks are multiply-accumulate (MAC) intensive operations. The TMS320C54x DSP is well suited to perform these tasks efficiently and generate a high-quality image that is close to the image quality offered by traditional film from the raw CCD data. We outline the various image pipeline processing stages below.

4.1 Black Clamp

To optimize the dynamic range of the pixel values represented by the CCD imager, the pixels representing black need to be corrected since the CCD cell still records some non-zero current at these pixel locations. The black clamp function adjusts for this difference by subtracting an offset from each pixel value, but clamping/clipping to zero to avoid a negative result.

4.2 Lens Distortion Compensation

Imperfections in the lens introduce nonlinearities in the brightness of the image. These nonlinearities reduce the brightness between the center of the image to the border of the image. The image pipeline compensates for the lens by adjusting the brightness of each pixel, depending on its spatial location.

4.3 Fault Pixel Interpolation

Large-pixel CCD arrays may have defective pixels. The missing pixels are interpolated with an interpolation scheme to provide the rest of the image processing data values at each pixel location. The manufacturer of the CCD sensor typically provides the locations of the missing pixels. The faulty pixel locations can also be computed by the DSC engine off-line by first capturing an image with the lens cap closed. The faulty pixels are imaged as ”white spots” and the rest of the image is dark. The faulty pixel locations can then be identified with a simple threshold detector and stored in memory. During the normal operation of the DSC, the image values at the faulty pixel locations are computed by an interpolation technique.

4.4 White Balance

The illumination during the recording of a scene is different from the illumination when viewing a picture. This results in a different color appearance that is typically seen as the bluish appearance of a face or the reddish appearance of the sky. Also, the sensitivity of each color channel varies such that grey or neutral colors are not represented correctly. To compensate for these unbalances in colors, the gain of the red, green, and blue channels is equalized. This is accomplished by computing the average brightness of each color component and by determining a scaling factor for each color component. Since the illuminants are unknown, a frequently used technique just balances the energy of the three colors. This equal energy approach requires an estimate of the unbalance between the color components.

4.5 CFA Interpolation

Due to the nature of a color filtered array, at any given pixel location, we only have one color pixel information (R, G, or B in the case of a Bayer pattern). However, the image pipeline needs full color resolution (R, G, and B) at each pixel in the image. Therefore, the two missing pixel colors are reconstructed by interpolating the neighboring pixels.

4.6 Gamma Correction

Display devices used for image-viewing and printers used for image hardcopy have a nonlinear mapping between the image gray value and the actual displayed pixel intensities. The gamma correction stage compensates for the differences between the images generated by the CCD sensor and the image displayed on a monitor or printed into a page.

4.7 Color Space Conversion

Typical image-compression algorithms such as JPEG operate on the YCbCr color space. Therefore, a color space conversion is performed to transform the image from an RGB color space to a YCbCr color space. This conversion is a linear transformation of each Y, Cb, and Cr value as a weighted sum of the R, G, B values at that pixel location.

4.8 Edge Enhancement

The nature of CFA interpolation filters introduces a low-pass filter that smoothes the edges in the image. To sharpen the images, the image pipeline uses an edge detector to compute the edge magnitude in the Y channel at each pixel. The edge magnitude is then scaled and added to the original luminance (Y) image to enhance the sharpness of the image.

4.9 False Color Suppression

Note that the edge enhancement is only performed in the Y channel of the image. This leads to misalignment in the color channels at the edges, resulting in rainbow-like artifacts. Suppressing the color components, Cb and Cr, at the edges reduces these artifacts.

4.10 Autofocus

It is also possible to automatically adjust the lens focus in a DSC through image processing. These autofocus mechanisms operate in a feedback loop. They perform image processing to detect the quality of lens focus and move the lens motor iteratively until the image comes sharply into focus.

4.11 Autoexposure

Due to varying scene brightness, to get a good overall image quality, it is necessary to control the exposure of the CCD. This is also accomplished in the DSC by sensing the average scene brightness and appropriately adjusting the CCD exposure time and/or gain. Similar to autofocus, the DSP performs this operation also in a closed-loop feedback fashion.

4.12 Image Compression

Most DSCs are limited in the amount of memory available on the camera; hence, image compression is employed to reduce the memory requirements of captured images. Typically, compression ratios of about 10:1 to 15:1 are used. Most of the existing DSCs use JPEG compression. The DCT and Huffman encoding stages dominate the computations in JPEG. Our current implementation is capable of performing an 8×8 DCT in 1220 cycles or 12.20 msec.

Future DSC will likely migrate to the JPEG2000 standard which employs a wavelet-coding scheme.

5 TMS320C54x DSC Implementation

This image pipeline was implemented on a C5409 DSP. Figure 5 shows a picture of the prototype TMS320C54x DSC system. This system interfaces to the CCD/CMOS module directly. The DSP reads the data from the sensor, processes the raw sensor data, and writes it to the SDRAM. The built-in NTSC/PAL encoder chip on the board allows direct display of the processed picture on the TV monitor. In implementing the image pipeline on the DSP, we designed an SDRAM controller that efficiently fetches the image data from the external memory to the on-chip memory in 16 x 16 blocks. All image pipeline operations, including JPEG compression, can be performed on the TMS320C54x on this 16 x 16 block of pixels and then the compressed bit stream is written out to the SDRAM.

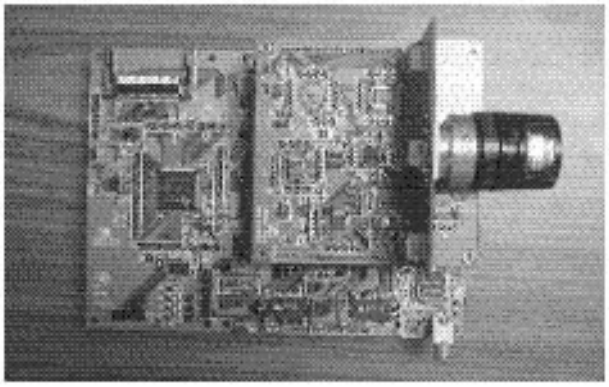

Figure 5. TMS320C54x DSC System

On this system, all image pipeline operations can be executed on chip since only a small 16 x 16 block of the image is used. Therefore, the TMS320C549 is well suited due to its large on-chip memory (32K x 16-bit RAM and 16K x 16-bit ROM). In this way, the processing time is kept short, because there is no need for external high-speed memory. Furthermore, this device offers high performance (100 MIPS) at low power consumption (0.45mA/MIPS).

Table 1 illustrates a detailed cycle count for the different stages of the image pipeline software. Due to the efficiency of the TMS320C54x instruction set and architecture, the entire image pipeline, including JPEG, takes about 150 cycles/pixel. Hence, a 1-Mpixel CCD image can be processed in 1.5 seconds on a 100-MHz TMS320C54x. This offers about a 2-second shot-to-shot delay, including data movement from external memory to on-chip memory.

Current DSCs also provide the ability for the user to view the captured images on the LCD screen on the camera or on an external TV monitor. Since the captured images are stored on a Compact Flash Card as JPEG bit streams, a playback-mode software is also provided on the DSP. This playback-mode software decodes the JPEG bit stream, scales the decoded image to the appropriate spatial resolution, and displays it on the LCD screen and/or the external TV monitor. Our TMS320C54x playback-mode software executes in 100 cycles/pixel. This offers a 1-second playback of a Mega-pixel image.

Table 1. TMS320C54x Performance

Task	Cycles/Pixel
Preprocessing (Black Clamping, Gain, White Balance, Gamma Correction)	22
Color Space Conversion	10
Interpolation	41
Edge Enhancement & False Color Suppression	27
Total	90
4:1:1 Decimation & JPEG Encoding	62
Total	152

Table 2 shows the program and data memory requirements to process the image pipeline and compress the image with JPEG standard. This code density allows the complete image pipeline software to reside on-chip. Having the complete software on-chip reduces external memory accesses and allows the use of slower external memory. This reduces overall system cost and lowers system power consumption.

Table 2. TMS320C54x Memory Requirements

Memory	K Bytes
Program	1.7
Data	4.6

Currently, most of the image pipeline operations are nonstandardized. Having a programmable DSC engine offers the ability to upgrade the software to conform to new standards or improve image pipeline quality. Unused performance can be dedicated to other tasks, such as human interface, voice annotation, audio recording/compression, modem, wireless communication, etc.

6 Conclusions

In this article, the authors have demonstrated an innovative approach to implementing a digital still camera image pipeline software on the TMS320C5000 platform. Our results show the feasibility of implementing the image pipeline on a TMS320C5409. Also, the programmable nature of this approach offers the flexibility needed in the DSC engine to allow the incorporation of innovative image-processing algorithms. Finally, the proposed approach offers the performance and low power that is crucial in the development of photo-quality images on a portable, battery-operated digital camera.

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This article is based on the IEEE publication, *Programming DSP Platform for Digital Still Cameras,* IEEE International Convention on Acoustics, Speech, and Signal Processing, March 1999.

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