Application Report
SPRAC90C–June 2017–Revised December 2018

PRU-ICSS Feature Comparison

Catalog Processors

ABSTRACT

This application report documents the feature differences between the PRU subsystems available on different TI processors.

Contents

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1 Introduction

TI Sitara devices offer two flavors of PRU subsystems-- PRU-ICSS and PRU_ICSSG. PRU-ICSS is available on AM335x, AM437x, AM57x family, and K2G devices. PRU_ICSSG is available on AM65x.

Table 1 shows a high-level feature comparison of the two PRU subsystems. The subsequent sections show the feature differences between each device that supports the given subsystem flavor. For a more detailed comparison, see the *PRU-ICSS/PRU_ICSSG Migration Guide*.

Table 1. PRU-ICSS and PRU_ICSSG Feature Comparison

Feature	PRU-ICSS	PRU_ICSSG
PRU cores	Yes	Yes
RTU_PRU (Auxiliary PRU) cores	No	Yes
IRAM (per PRU / RTU_PRU core)	Yes	Yes
DRAM (per PRU / RTU_PRU core)	Yes	Yes
Shared DRAM	Yes	Yes
INTC	Yes	Yes
General Purpose Inputs		
Direct Input	Yes	Yes
16-bit Parallel Capture	Yes	Yes
28-bit Shift	Yes	Yes
3 Ch. Peripheral Interface (EnDAT)	Device dependent	Yes
9 Ch. Sigma Delta	Device dependent	Yes
General Purpose Outputs		
Direct Output	Yes	Yes
Shift out	Yes	Yes

Table 1. PRU-ICSS and PRU_ICSSG Feature Comparison (continued)

Feature	PRU-ICSS	PRU_ICSSG
Accelerators: Data Processing		
MPY/MAC	Yes	Yes
CRC 16/32	Device dependent	Yes
Scratch Pad	Yes	Yes
IPC Scratch Pad	No	Yes
Broadside RAM	No	Yes
BSWAP	No	Yes
SUM32	No	Yes
Task Manager	No	Yes
Spinlock	No	Yes
Filter Data Base (FDB)	No	Yes
Accelerators: Data Movement		
XFR2VBUS	No	Yes
PSI TX & RX	No	Yes
XFR2TR	No	Yes
Peripherals		
UART	Yes	Yes
eCAP	Yes	Yes
IEP	Yes	Yes
MII_RT or MII_G_RT	Yes (MII)	Yes (MII/RGMII)
MDIO	Yes	Yes
SGMII	No	Yes
PWM	No	Yes

2 PRU-ICSS Feature Comparison

Table 2. PRU-ICSS Feature Comparison

Features	AM335x	AM437x		AM570x	AM571x	AM572x	AM574x	K2G
	PRU-ICSS1	PRU-ICSS1	PRU-ICSS0	2x PRU-ICSS (1)	2x PRU-ICSS (1)	2x PRU-ICSS (1)	2x PRU-ICSS (1)	2x PRU-ICSS (1)
Number of PRU cores	2	2	2	2	2	2	2	2
Max Frequency	200 MHz	225 MHz (2)	225 MHz (2)	200 MHz	200 MHz	200 MHz	200 MHz	200 MHz
IRAM size (per PRU core)	8 KB	12 KB	4 KB	12 KB	12 KB	12 KB	12 KB	16 KB
DRAM size (per PRU core)	8 KB	8 KB	4 KB	8 KB	8 KB	8 KB	8 KB	8 KB
Shared DRAM size	12 KB	32 KB	0 KB	32KB	32KB	32KB	32 KB	64KB w/ ECC
General Purpose Input (per PRU core)	Direct; or 16-bit parallel capture; or 28-bit shift	Direct; or 16-bit parallel capture; or 28-bit shift; or 3ch EnDat 2.2; or 9ch Sigma Delta	Direct; or 16-bit parallel capture; or 28-bit shift; or 3ch EnDat 2.2; or 9ch Sigma Delta	Direct; or 16-bit parallel capture; or 28-bit shift; or 3ch EnDat 2.2; or 9ch Sigma Delta	Direct; or 16-bit parallel capture; or 28-bit shift; or 3ch EnDat 2.2; or 9ch Sigma Delta	Direct; or 16-bit parallel capture; or 28-bit shift	Direct; or 16-bit parallel capture; or 28- bit shift; or 3ch EnDat 2.2; or 9ch Sigma Delta	Direct; or 16-bit parallel capture; or 28-bit shift; or 3ch EnDat 2.2; or 9ch Sigma Delta
General Purpose Output (per PRU core)	Direct; or Shift out	Direct; or Shift out	Direct; or Shift out	Direct; or Shift out	Direct; or Shift out	Direct; or Shift out	Direct; or Shift out	Direct; or Shift out
GPI Pins (PRU0, PRU1)	17, 17	13, 0	20, 20	0/21(3), 21/17	0/21(3), 21/21	21, 21	21, 21	20, 20
GPO Pins (PRU0, PRU1)	16, 16	12, 0	20, 20	0/21(3), 21/17	0/21(3), 21/21	21, 21	21, 21	20, 20
MPY/MAC	Y	Y	Y	Y	Y	Y	Y	Y
Scratchpad	Y (3 banks)	Y (3 banks)	N	Y (3 banks)	Y (3 banks)	Y (3 banks)	Y (3 banks)	Y (3 banks)
CRC16/32	0	2	2	2	2	2 (4)	2	2
INTC	1	1	1	1	1	1	1	1
Peripherals								
UART	1	1	1	1 / not pinned out (5)	1	1	1	1
eCAP	1	1	not pinned out	1 / not pinned out (5)	1	1	1	1
IEP	1	1	not pinned out	1 / not pinned out (5)	1	1	1	1
MII_RT	2	2	not pinned out	2	2	2	2	2
MDIO	1	1	not pinned out	1	1	1	1	1

(1) The name PRU-ICSS and PRUSS are used interchangeably throughout the AM57xx and K2G documentation to describe the Programmable Real-Time Unit (PRU) and Industrial Communication Subsystem.

(2) The default frequency for AM437x is 200 MHz. However, the max frequency 225 MHz is achievable through display PLL CLKOUT. For DSS limitations when configuring this PLL for frequencies >200 MHz, see the *AM437x Sitara Processors Technical Reference Manual*.

(3) AM571x and AM570x PRU-ICSS1 does not pin out the PRU0 core GPIs/GPOs. The other AM571x and AM570x PRU cores (PRU-ICSS1 PRU1, PRU-ICSS2 PRU0, PRU-ICSS2 PRU1) each pin out the number of GPIs/GPOs is listed in Table 2.

(4) AM572x SR1.1 does not have CRC16/32. Within the AM57x family, this feature is only available in AM572x SR2.0, AM571x, and AM570x.

(5) AM570x PRU-ICSS2 does not pin out these submodules. However, they are pinned out on the other AM570x subsystem (PRU-ICSS1).

3 PRU_ICSSG Feature Comparison

Table 3. PRU_ICSSG Feature Comparison Across Devices

Feature	AM65x
	3x PRU_ICSSG
Number of PRU cores	2
Number of RTU_PRU (Auxiliary PRU) cores	2
Max Frequency	250 MHz
IRAM Size (per PRU / RTU_PRU core)	12 KB / 8 KB (w/ ECC)
DRAM Size (per PRU / RTU_PRU pair)	8 KB (w/ ECC)
Shared DRAM Size	64 KB (w/ ECC)
INTC	Yes
General Purpose Inputs (per PRU core)	Direct; or 16-bit parallel capture; or 28- bit shift; or 3ch EnDat 2.2; or 9ch Sigma Delta
General Purpose Outputs (per PRU core)	Direct; or Shift out
GPI Pins (PRU0, PRU1)	PRU_ICSSG0: 19/19
	PRU_ICSSG1: 19/19
	PRU_ICSSG2: 17/17
GPO Pins (PRU0, PRU1)	PRU_ICSSG0: 19/19
	PRU_ICSSG1: 19/19
	PRU_ICSSG2: 17/17
Accelerators: Data Processing	
MPY/MAC	Yes
CRC 16/32	Yes
Scratch Pad	Y (4 banks)
IPC Scratch Pad	Yes
Broadside RAM	4 KB
BSWAP	Yes
SUM32	Yes
Task Manager	Yes
Spinlock	Yes
Filter Data Base (FDB)	Yes
Accelerators: Data Movement	
XFR2VBUS	Yes
PSI TX & RX	Yes
XFR2TR	Yes
Peripherals	
UART	Yes
eCAP	Yes
IEP	Yes
MII_G_RT (MII/RGMII)	PRU_ICSSG0: MII/RGMII
	PRU_ICSSG1: MII/RGMII
	PRU_ICSSG2: RGMII
MDIO	Yes
SGMII	PRU_ICSSG2 instance (only)
PWM	Yes

4 References

- *AM437x Sitara Processors Technical Reference Manual*
- *PRU-ICSS/PRU_ICSSG Migration Guide*

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from B Revision (August 2018) to C Revision	Page
• Update was made in Section 1.	1
• Updates were made in Section 2.	3
• Added new Section 3.	4

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