

# Processor-SDK RTOS Power Management and Measurement

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## ABSTRACT

Processor-SDK RTOS provides out-of-the-box power management examples that empower customers to tailor Sitara processors' (ARM and DSP) power-performance points per use case. You can configure all supported operating points and run CPU Idle and Dhrystone benchmarking workloads while employing a minimal kernel with real-time assurance. This application report provides an overview of the Processor-SDK RTOS power management library and power consumption data on Sitara processors.

## Contents

1	Introduction .....	1
2	Processor-SDK-RTOS Power Management .....	2
3	Processor-SDK-RTOS Power Consumption .....	4
4	References .....	5

## List of Figures

1	Power Management Software Stack .....	3
2	SOC-PMIC Communication Over I2C Bus .....	3
3	Dhrystone Processor-SDK RTOS Power Measurement Data for AM335x GP EVM .....	5

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## 1 Introduction

With the advent of real-time automation and sensing, power management is proving to be increasingly important in system-on-chip (SoC) devices used in industrial and building or home automation applications.

The discussion topics are applicable for Sitara™ processors such as AM335x, AM437x and AM57x. This paper provides an introduction to Processor-SDK RTOS power management and measurement using AM335x as a vehicle for discussion.

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**NOTE:** It is important to note that the measurements are within datasheet recommendations. Extreme operating conditions that may have an effect on device lifetime have not been considered. For example, operating the device under extreme operating conditions such as high voltage and frequency over high temperatures while running heavy applications involving PCIe or HDMI may shorten the lifetime of the device.

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### 1.1 Why is Power Management Important?

Wherever possible, system engineers are shying away from bulky thermal solutions and cooling fans due to reliability concerns. Heat sinks and cooling fans become unavoidable when device power consumption exceeds 5W, posing serious reliability concerns over time. Thermal management is the main focus of the mechanical design for industrial applications such as programmable logic controllers or motor control.

## 1.2 Power Management on Linux and RTOS

Linux users have had a variety of out of box power management features at their fingertips for complex systems where power management is mostly controlled in kernel space. Systems engineers that use RTOS as their choice of operating system are frequently looking for a solution where the application has more control. RTOS power management features are perfect for systems that require a minimal kernel while giving autonomous control to the application and providing real-time guarantees. Legacy RTOS devices also stand to benefit from the new RTOS power management features in Texas Instruments' Processor Software Development Kit (SDK) RTOS, based on TI-RTOS. TI-RTOS provides application program interfaces that can be used to easily configure operating points for desired power and performance.

## 1.3 Which Applications Benefit From RTOS Power Management?

In building automation applications, such as meeting room controllers that may be idle up to 99% of the time, low power devices are preferred, thereby reducing power consumption. In factory automation, when a factory worker uses a handheld battery powered controller, longer period between charges is preferred. Similarly, in defense applications, battery operated radios need low power devices.

In military applications as well as factory automation, users want real time guarantees. In such applications RTOS may be preferable.

## 1.4 Low Power Sitara Processors

Sitara Processors, such as AM335x, provide low power consumption which prolongs battery life and reduces heat emissions, enabling convenient, compact, fan-less applications. Currently, AM335x supports various operating points for active and sleep states as well as heavy workload operating modes.

## 2 Processor-SDK-RTOS Power Management

The Texas Instruments Processor Software Development Kit (Processor-SDK) is a single scalable software platform that offers streamlined development across [TI processors, including both Sitara ARM and DSP devices](#). The Processor-SDK for TI-RTOS provides fundamental platform software and tools for development, deployment and execution of RTOS-based applications.

Processor-SDK-RTOS provides power management features for Sitara devices. The Power Management (PM) software APIs supply a basic power management framework. PM APIs are supported for ARM on AM335x GP EVM and AM437x GP EVM as well as M4, DSP and ARM on AM572x GP EVM. In general, the key features supported by this framework include:

- CPU Operating Performance Points
- Low Power CPU Idle
- Enable/Disable Control of Device Modules and Clocks
- Thermal Management
- Power Event Notification Infrastructure

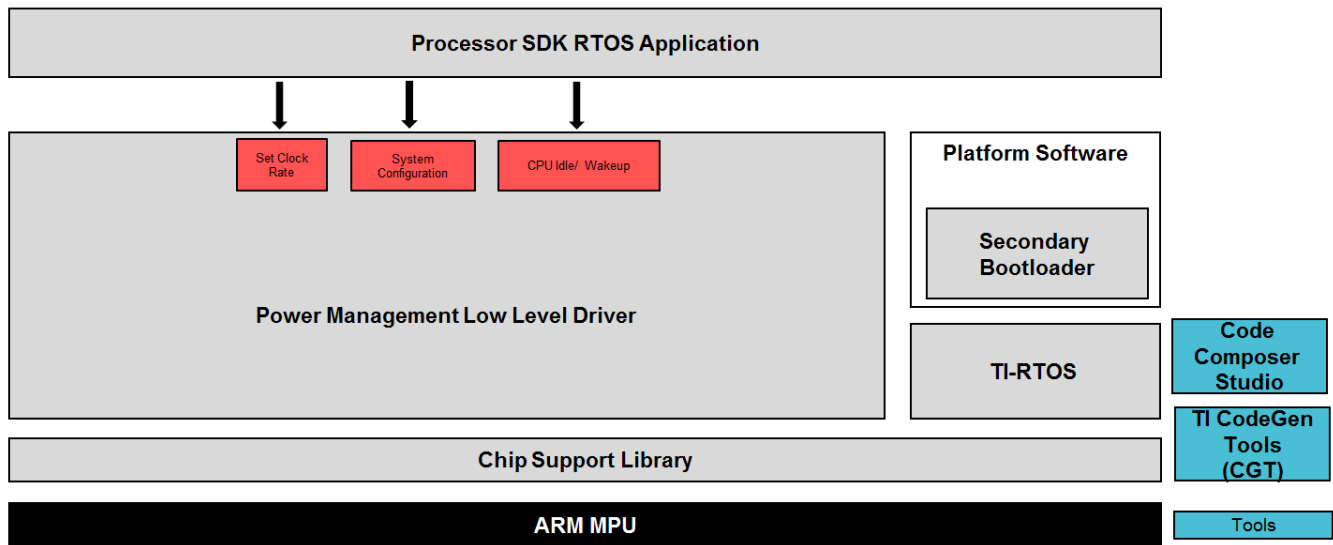


Figure 1. Power Management Software Stack

## 2.1 CPU Operating Performance Points

The PM framework has the capability to switch devices between different Operating Performance Points (OPP) at run time. These OPP are aligned with the device specifications. When the PM framework's OPP modification API is invoked, the PM software stack changes the voltage level and frequency. The PM software stack modifies the voltage level by accessing the device's Power Management Integrated Chip, or PMIC, driver via the I2C bus.

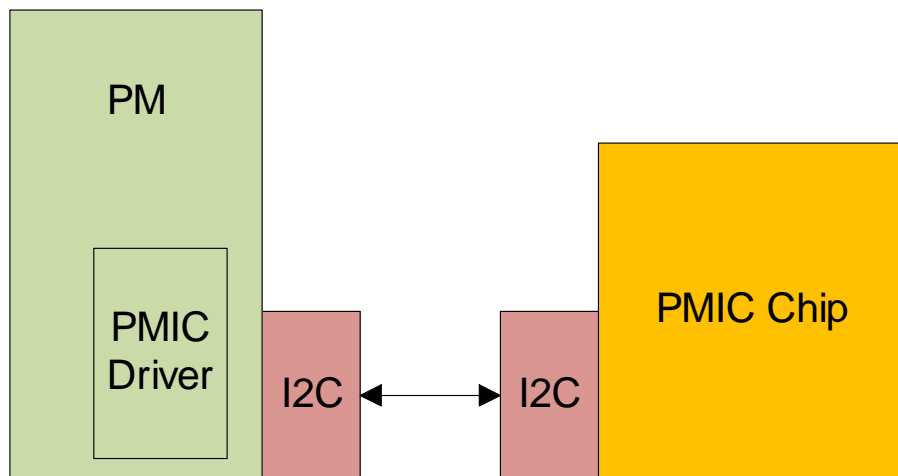


Figure 2. SOC-PMIC Communication Over I2C Bus

PM adjusts the processor frequency by updating the multiplier and divider settings of the Phased Lock Loop, or PLL, feeding the processor. Detailed information of OPP voltage and frequency settings for the ARM master core, MPU, on Sitara devices can be found in the datasheets for [AM335x](#), [AM437x](#) and [AM572x](#) GP EVM.

**NOTE:** Currently, AM571x and AM570x are not supported.

## 2.2 Low Power CPU Idle

The PM framework enables Sitara processor low power modes when the system is idle. PM provides instrumentation through which the Operating System (OS) can invoke the CPU to go into an idle mode to save power. Typically, the low power capabilities are invoked during OS idle. When the low-power capabilities are invoked a couple things happen:

- The CPU clock state is moved to the auto-clock gate. As a result, when the CPU itself enters a low power state the device hardware will clock gate the CPU clock.
- CPU local memory retention is enabled (AM572x MPU only)
- CPU power domain configured to go to off state on CPU transition to low power state (AM572x MPU, M4, and C66x only)
- CPU WFI instruction is executed putting the CPU into a low power state and, as described above, clock gating the CPU

The CPU can be brought out of low power idle via any interrupt source configured for wakeup.

## 2.3 Device Module and Clock Enable/Disable Control

PM has a set of application program interfaces (APIs) that provide system control of individual device modules, including peripherals and clocks. The APIs can be used to enable and disable subsections of the device and its clock tree on demand. This capability allows customization of the device's power profile based on the needs of the use case.

## 2.4 Thermal Management

The PM framework also provides a set of thermal management capabilities, currently supported only for the AM572x device family.

The AM572x devices contain on-die temperature sensors with high and low temperature threshold alerts. PM ties to these alerts and provides a basic temperature threshold interrupt handler that can be expanded upon by the OS through a callback functionality implemented within PM's interrupt handler. The OS can use the callback registration functionality to take actions specific to which threshold was hit, high or low, in order to bring the temperature in line with what is expected for the use case. In other words, if a high temperature is detected the CPU can move the device into a low power consumption state to reduce the temperature. You can specify which mode the device should move to, for example, using PM APIs to lower OPP or enter idle mode.

## 2.5 Power Event Notification Infrastructure

Most actions taken by the PM framework are tracked and instrumented with an event notification scheme. The PM event notification scheme allows the OS to register callback functions with the PM infrastructure which the OS can specify be invoked during certain power events. Through these means the OS can gain feedback on the actions taking place within the PM infrastructure. A system designer can also supplement PM events with additional focused device actions based on the use case the system designer is targeting.

## 3 Processor-SDK-RTOS Power Consumption

The Sitara RTOS Power Measurement metrics contained in this document serve to give users a better understanding of AM335x active power behaviors -- making it easier to determine a suitable configuration to meet a given power budget. If you are interested in power measurement information about other Sitara devices such as AM437x and AM572x, please post your question on the [Sitara™ Processors Section of the TI E2E Support Community](#).

Power consumption is highly dependent on the individual user's application; however, this document focuses on providing AM335x power measurement data during OS idle (WFI, wait for interrupt) mode.

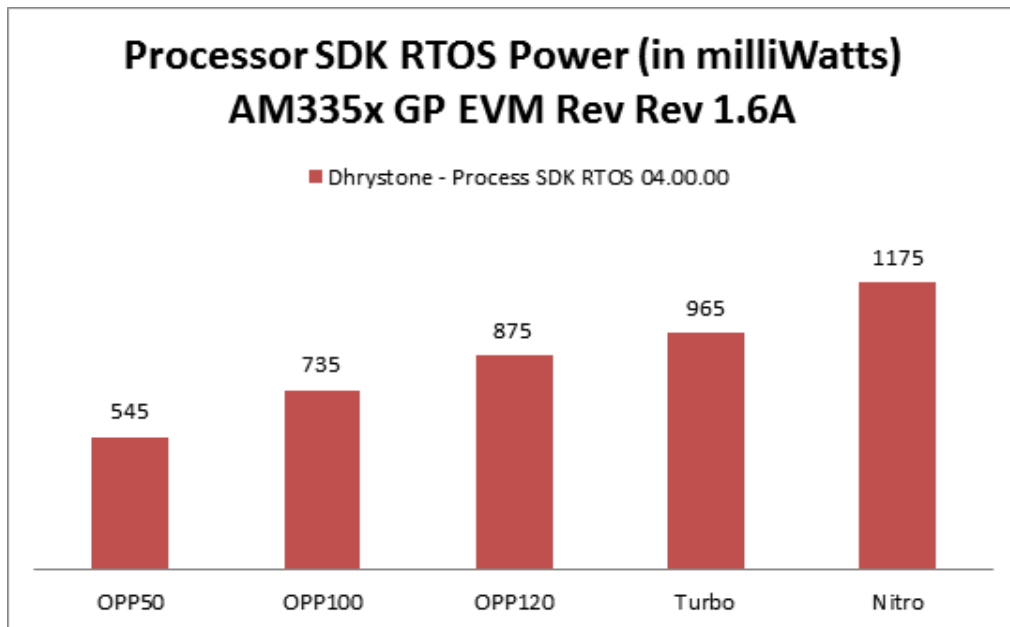
[AM335x Power Estimation Tool](#) wiki: The Power Estimation Tool (PET) provides insight into gaining power consumption of select Sitara processors. The tool includes the ability to choose multiple application scenarios and understand the power consumption as well as how advanced power saving techniques can be applied to further reduce overall power consumption.

Figure 3 shows how a collection of real total power measurements (all power rails) were measured on an AM335x GP EVM with a high-precision digital multimeter. All tests were not conducted in a controlled environment. The ambient room temperature was approximately 25°C.

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**NOTE:** These test cases have not been optimized for low power.

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**Figure 3. Dhrystone Processor-SDK RTOS Power Measurement Data for AM335x GP EVM**

For additional details about the AM335x processor, please visit the [TI.com product page](#).

#### 4 References

- [AM335x Sitara™ Processors Data Manual](#)
- [AM335x and AMIC110 Sitara™ Processors Technical Reference Manual](#)
- [AM335x Sitara™ Processors Silicon Revisions 2.1, 2.0, 1.0 Silicon Errata](#)
- [AM335x Linux Power Management User Guide wiki page](#)
- [AM335x Evaluation Module](#)
- [AM335x General Purpose EVM HW User Guide wiki page](#)
- [AM335x General Purpose EVM Board Design Files wiki page](#)
- [AM335x Low Power Design Guide](#)
- [AM335x Power Estimation Tool wiki page](#)
- [Linux Core Power Management User's Guide \(v4.4\) wiki page](#)
- [AM335x Schematic Checklist wiki page](#)
- [Thermal Design Guide for DSP and ARM Application Processors](#)
- [Demonstrating Manual Power Measurements on the AM335x GP EVM using Shunt Resistors How-To Video](#)

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