20V P 通道 NexFET™ 功率金属氧化物半导体场效应晶体管 (MOSFET)

查询样片: **CSD25402Q3A**

特性

- 超低 Q_g 和 Q_{gd}
- 低热阻
- 低 $R_{DS(on)}$
- 无铅且无卤素
- 符合 **RoHS** 环保标准
- 小外形尺寸无引线 **(SON) 3.3mm × 3.3mm** 塑料封装

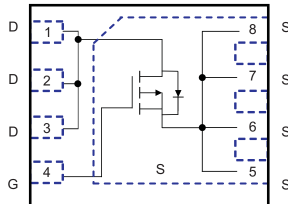
应用范围

- 直流-直流转换器
- 电池管理
- 负载开关
- 电池保护

说明

这款 -20V，7.7mΩ NexFET™ 功率 MOSFET 被设计成最大限度地减少 SON 3 × 3 封装内的功率转换负载管理应用中的损耗，此封装类型针对器件的尺寸提供出色的热性能。

顶视图



产品概述

V_{DS}	漏源极电压	-20		V
Q_g	栅极电荷总量 (-4.5V)	7.5		nC
Q_{gd}	栅极电荷漏极	1.1		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = -1.8V	74	mΩ
		V_{GS} = -2.5V	13.3	mΩ
		V_{GS} = -4.5V	7.7	mΩ
V_{th}	阀值电压	-0.9		V

订购信息

器件	封装	介质	数量	出货
CSD25402Q3A	SON 3 × 3 塑料封装	13 英寸卷带	2500	卷带封装

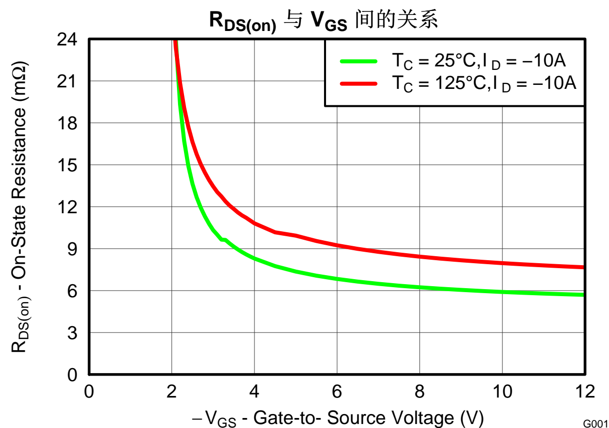
绝对最大额定值

T_A = 25°C		值	单位
V_{DS}	漏源电压	-20	V
V_{GS}	栅源电压	+12 或 -12	V
I_D	持续漏极电流，T_C = 25°C 时测得	-72	A
	持续漏极电流（受封装限制）	-35	A
	持续漏极电流(1)	-15	A
I_{DM}	脉冲漏极电流(2)	-82	A
P_D	功率耗散(1)	2.8	W
T_J, T_{STG}	运行结温和储存温度范围	-55 至 150	°C

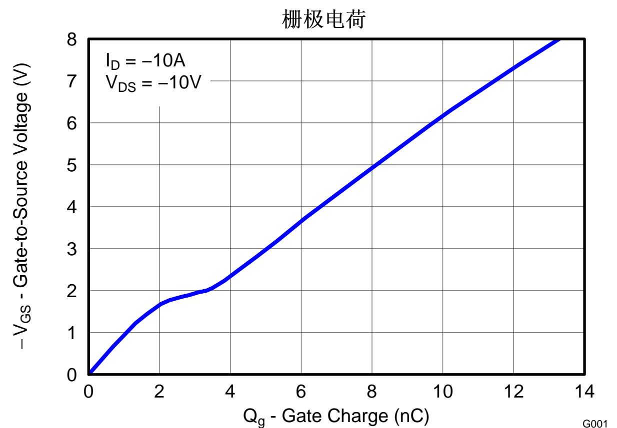
(1) $R_{\theta JA}$ = 55°C/W，这是在厚度为 0.060" 的环氧树脂 (FR4) 印刷电路板 (PCB) 上的 1 英寸^2 铜过渡垫片（2 盎司）上测得的典型值。

(2) 脉宽 ≤ 300μs，占空比 ≤ 2%

$R_{DS(on)}$ 与 V_{GS} 间的关系



栅极电荷



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English Data Sheet: SLPS454

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = –250 μA	–20			V
I_{DSS}	Drain-to-Source Leakage Current	V_{GS} = 0 V, V_{DS} = –16 V			–1	μA
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = ±12 V			–100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{DS} = V_{GS}, I_D = –250 μA	–0.65	–0.90	–1.15	V
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = –1.8 V, I_D = –1 A		74	300	mΩ
		V_{GS} = –2.5 V, I_D = –10 A		13.3	15.9	mΩ
		V_{GS} = –4.5 V, I_D = –10 A		7.7	8.9	mΩ
g_{fs}	Transconductance	V_{DS} = –10 V, I_D = –10 A		59		S
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = –10 V, f = 1 MHz		1380	1790	pF
C_{OSS}	Output Capacitance			763	992	pF
C_{RSS}	Reverse Transfer Capacitance			39	51	pF
R_G	Series Gate Resistance			3.7	7.4	Ω
Q_g	Gate Charge Total (4.5 V)	V_{DS} = –10 V, I_D = –10 A		7.5	9.7	nC
Q_{gd}	Gate Charge Gate to Drain			1.1		nC
Q_{gs}	Gate Charge Gate to Source			2.4		nC
$Q_{g(th)}$	Gate Charge at V_{th}			1.0		nC
Q_{OSS}	Output Charge	V_{DS} = –10 V, V_{GS} = 0 V		7.6		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = –10 V, V_{GS} = –4.5 V, I_D = –10 A , R_G = 5 Ω		10		ns
t_r	Rise Time			7		ns
$t_{d(off)}$	Turn Off Delay Time			25		ns
t_f	Fall Time			12		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_S = –10 A, V_{GS} = 0 V		–0.8	–1	V
Q_{rr}	Reverse Recovery Charge	V_{DS} = –8.5 V, I_F = –10 A, di/dt = 200 A/μs		10.3		nC
t_{rr}	Reverse Recovery Time			21		ns

THERMAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{θJC}$	Thermal Resistance Junction to Case[(1)]			2.3	°C/W
$R_{θJA}$	Thermal Resistance Junction to Ambient[(1)(2)]			55	°C/W

(1) $R_{θJC}$ is determined with the device mounted on a 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{θJC}$ is specified by design, whereas $R_{θJA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.

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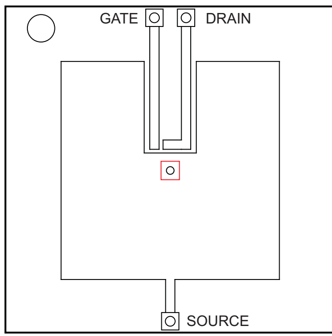
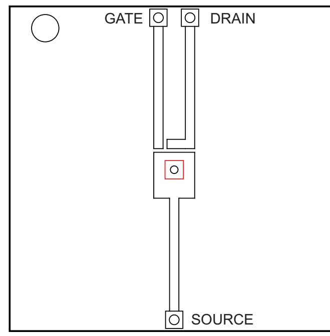


Max $R_{\theta JA}$ = 55°C/W when mounted on 1 inch^2 of 2 oz. Cu.



Max $R_{\theta JA}$ = 175°C/W when mounted on minimum pad area of 2 oz. Cu.

TYPICAL MOSFET CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

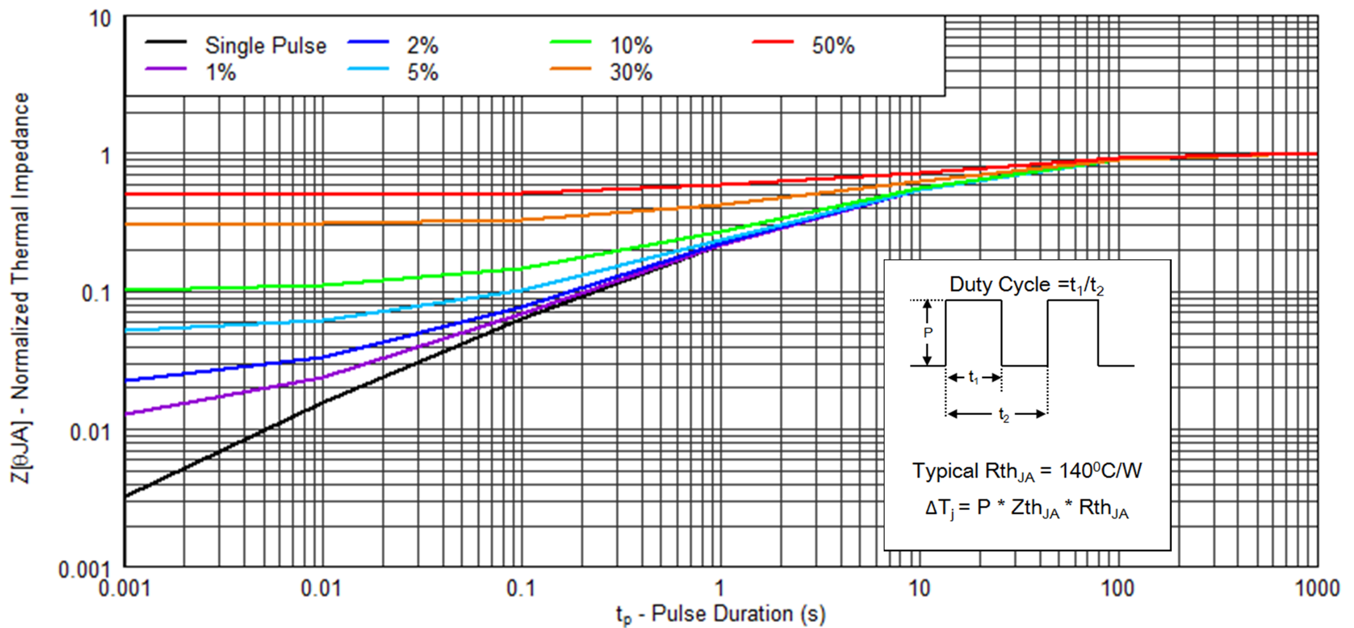


Figure 1. Transient Thermal Impedance

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TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

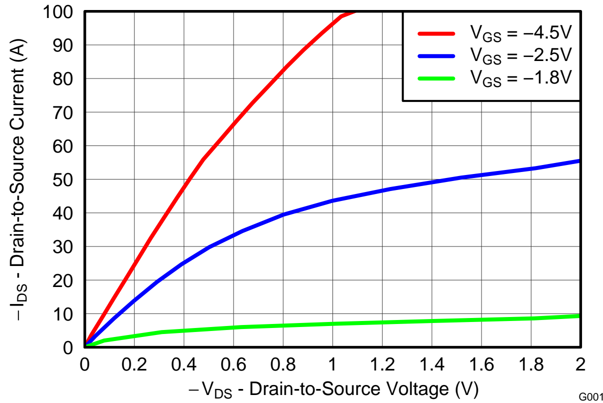

Figure 2. Saturation Characteristics

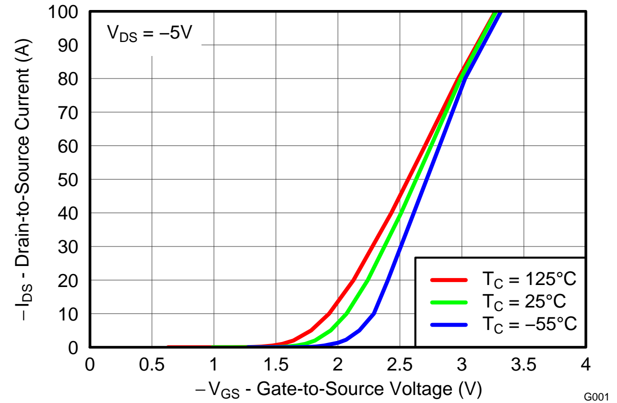

Figure 3. Transfer Characteristics

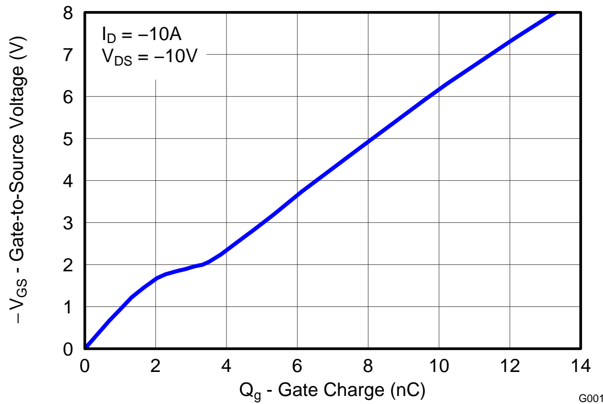

Figure 4. Gate Charge

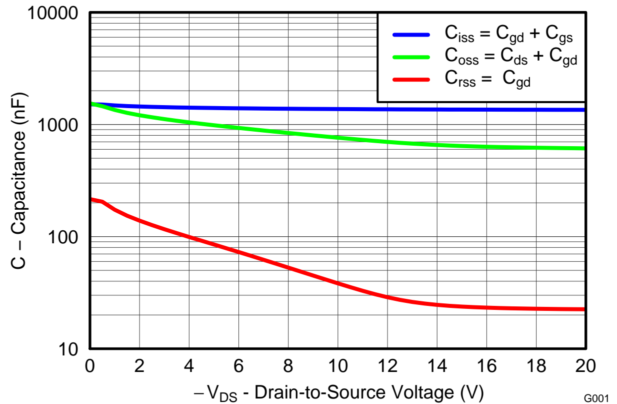

Figure 5. Capacitance

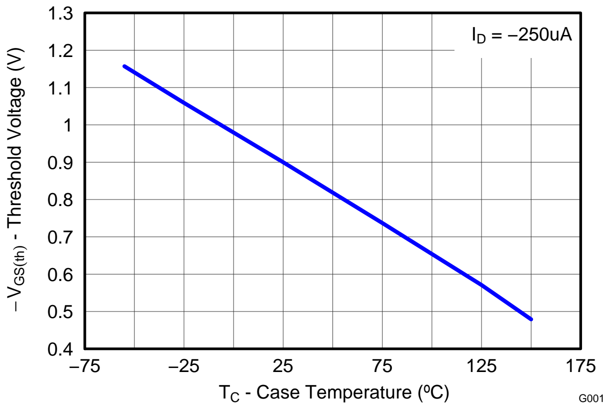

Figure 6. Threshold Voltage vs. Temperature

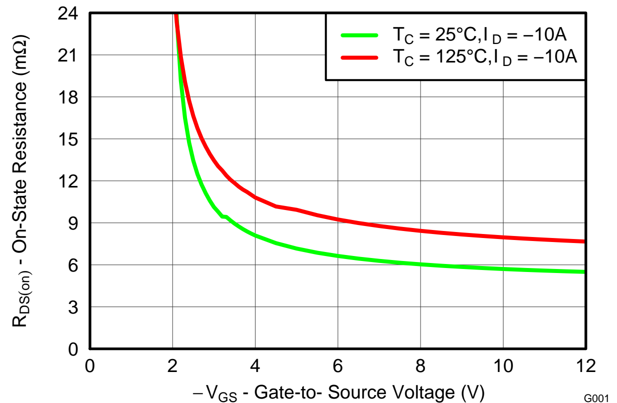

Figure 7. On-State Resistance vs. Gate-to-Source Voltage

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TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

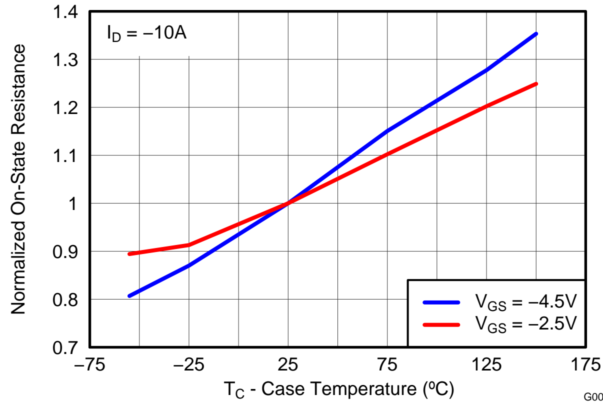

Figure 8. Normalized On-State Resistance vs. Temperature

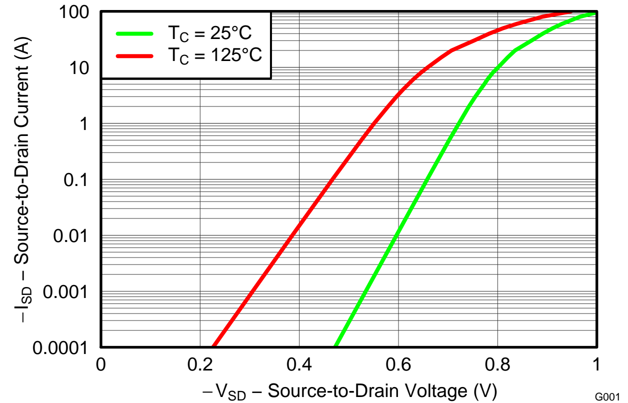

Figure 9. Typical Diode Forward Voltage

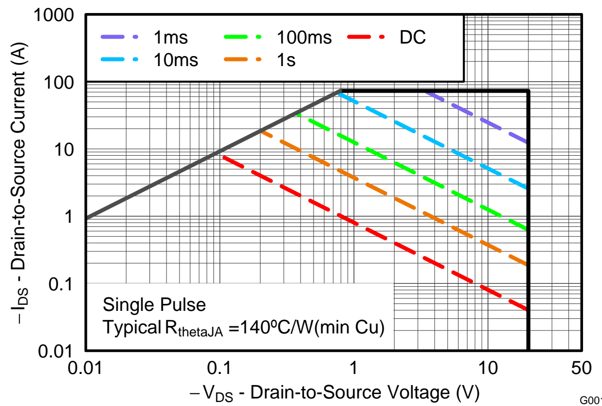

Figure 10. Maximum Safe Operating Area

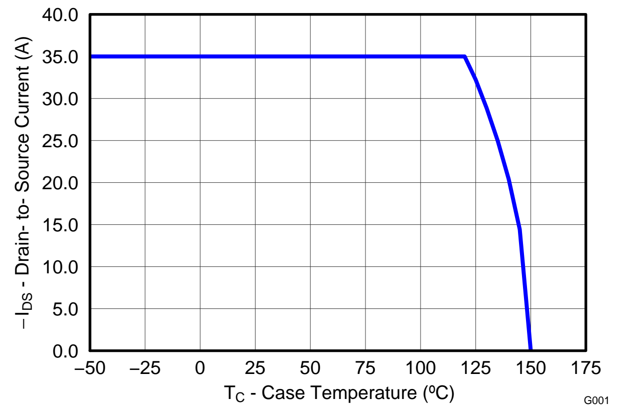

Figure 11. Maximum Drain Current vs. Temperature

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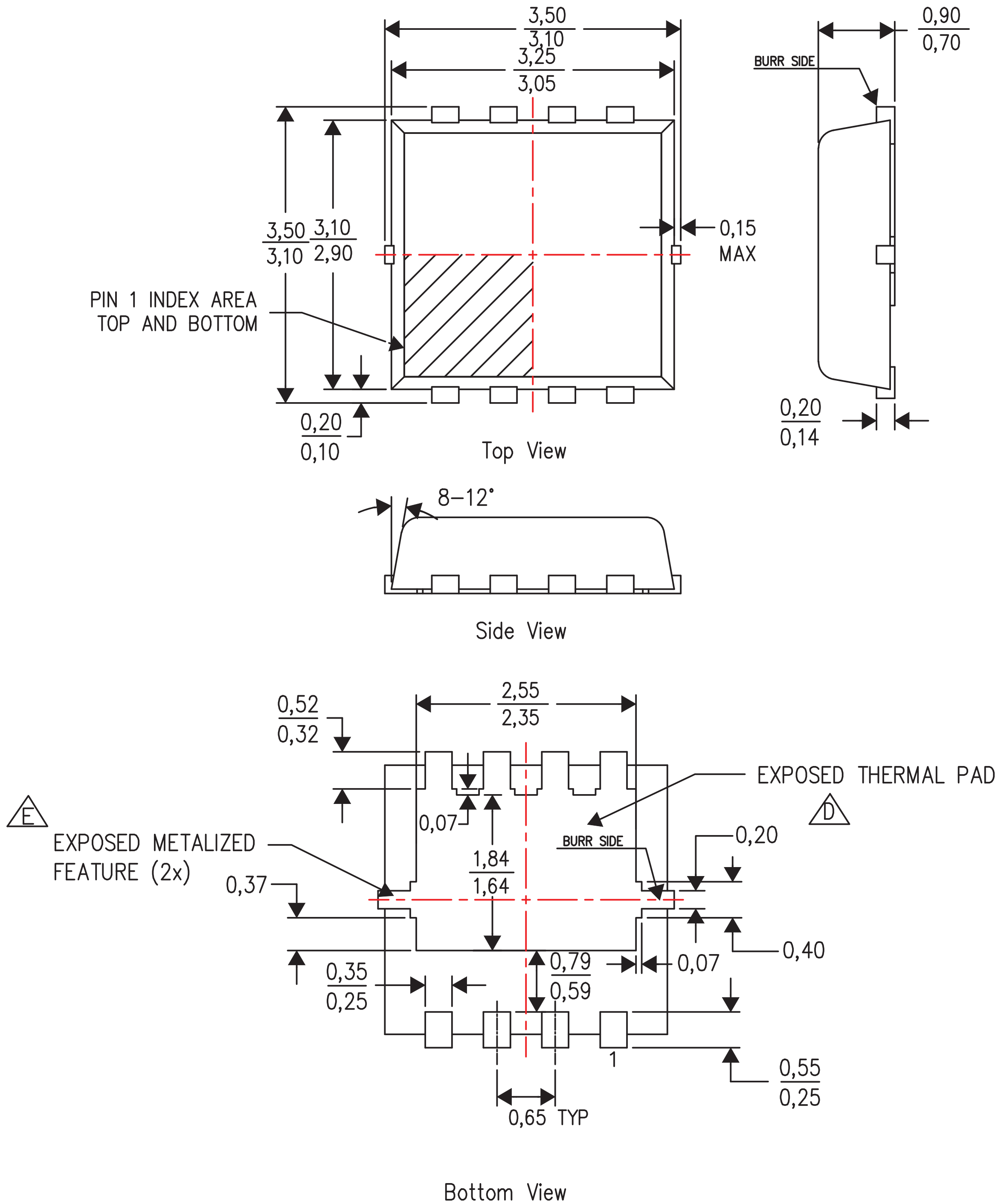
MECHANICAL DATA

Q3A Package Dimensions



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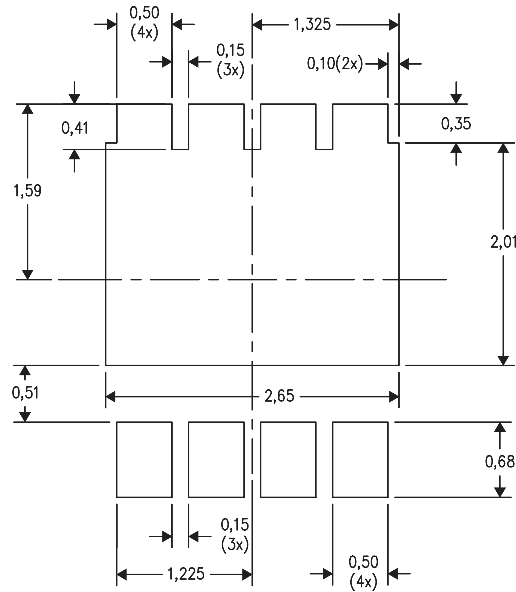
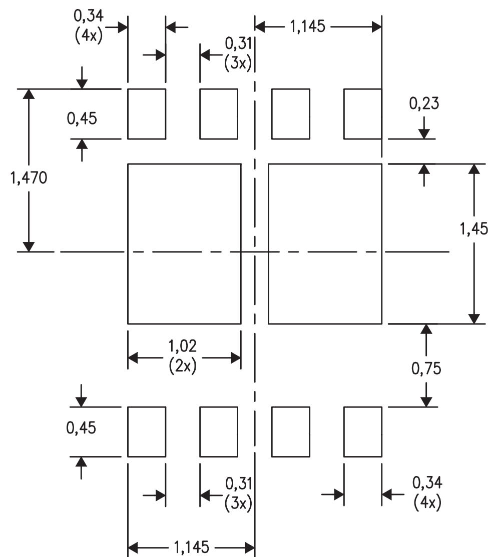
Q3A Recommended PCB Pattern



For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

Q3A Recommended Stencil Pattern



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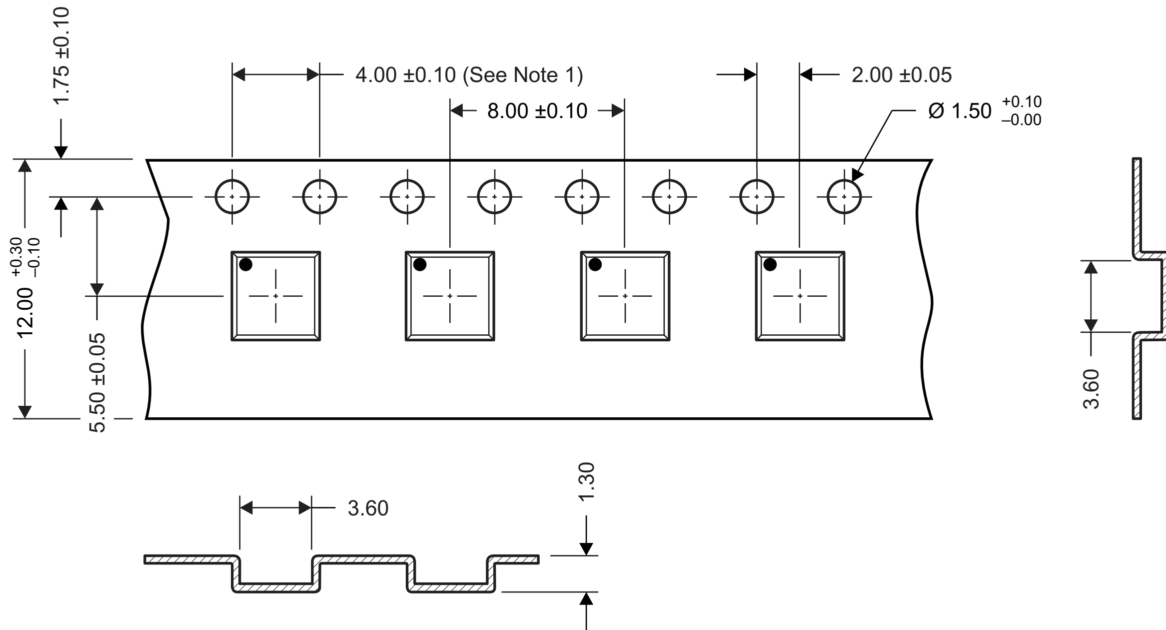
Q3A Tape and Reel Information



Notes:
1. 10-sprocket hole-pitch cumulative tolerance ±0.2
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
3. Material: black static-dissipative polystyrene
4. All dimensions are in mm, unless otherwise specified
5. Thickness: 0.30 ±0.05 mm
6. MSL1 260°C (IR and convection) PbF reflow compatible

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD25402Q3A	ACTIVE	VSONP	DNH	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-55 to 150	25402	Samples
CSD25402Q3AT	PREVIEW	VSONP	DNH	8	250	TBD	Call TI	Call TI	-55 to 150		

[(1)] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[(2)] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[(3)] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[(4)] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[(5)] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[(6)] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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