DLPC120-Q1 汽车 DMD 控制器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
  - 温度等级 2 级：–40°C 至 105°C 环境温度
- 兼容两种 DMD 器件：
  - DLP3000-Q1 - 0.3 WVGA TYPE A100
  - DLP3030-Q1 - 0.3 WVGA S450
- 视频输入接口：
  - 24 位并行接口（RGB888、RGB666 或 RGB565）
  - 60Hz 帧速率
  - 输入分辨率从 QVGA 一直到 WVGA
  - 像素时钟高达 40MHz
- 视频处理：
  - 图像缩放
  - 可编程去伽玛曲线
  - 边框调整
  - 水平和垂直图像翻转
- DMD 接口：
  - 78MHz DDR DMD 接口
  - 在整个工作温度范围内具有一致的 DMD 数据加载和复位控制
  - 断电时自动停止 DMD
  - DMD 温度管理
- 支持外部存储器
  - DDR2：312MHz 时钟（624MHz 数据速率）
  - 串行闪存 39MHz 时钟
- 系统控制
  - I^2C 通信接口
  - 可编程启动界面
  - DMD 电源和复位驱动器控制
  - 基于闪存的可编程配置
- 测试支持
  - 内置测试信号发生器
  - 支持边界扫描的 JTAG
- 采用 216 引脚 1.0mm 间距 BGA 封装

2 应用

- 宽视野和增强现实抬头显示 (HUD)
- 车内投影显示和照明
- 高分辨率前照灯

3 说明

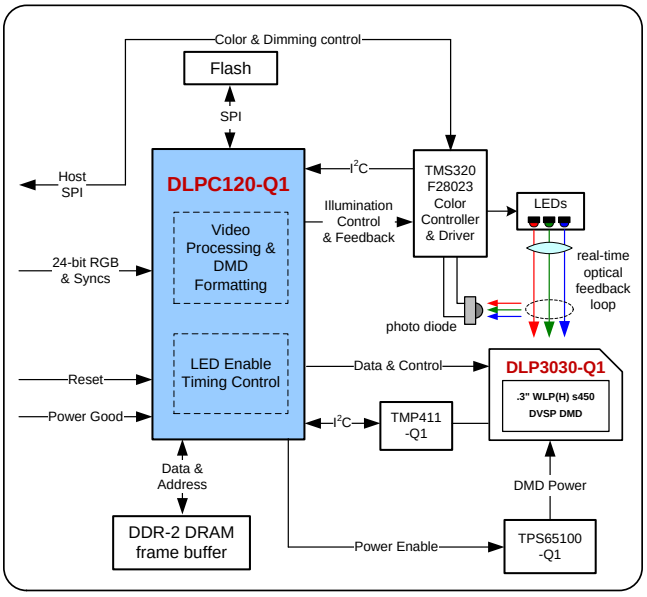
适用于汽车 应用 的 DLPC120-Q1 DMD 显示控制器是一个芯片组的组成部分，可兼容两个 DMD（即 DLP3000-Q1 或 DLP3030-Q1）中的其中一个。DLPC120-Q1 的核心逻辑负责接受视频输入并对数据进行格式化以便在 DMD 上显示，同时还控制 RGB LED 来形成实时图像。DLPC120-Q1 还负责根据外部系统控制或 DMD 温度输入来控制 DMD 的上电和断电事件。通过与外部调光电路和微控制器结合，DLPC120-Q1 支持 HUD 应用的宽调光范围 (> 5000:1)。通常情况下，DLPC120-Q1 是使用 I^2C 接口与主机处理器通信的从属器件。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
DLPC120-Q1	NFBGA (216)	16.00mm × 16.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型系统图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (November 2017) to Revision A **Page**

- 已更改 将器件状态从*高级信息* 更改为*生产数据* ... 1
- Changed Case-to-junction thermal coefficient from 0.77°C/W : to 0.28°C/W in *Thermal Information* table ... 12

5 Pin Configuration and Functions

ZXS Package
216-Pin BGA
Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VSS	VCCIO_2	DMD_SAC_CLK	DMD_SAC_BUS	DMD_DAD_OEZ	DMD_DCLK	DMD_D14	DMD_D11	DMD_D10	DMD_D8	DMD_D5	DMD_D2	DMD_D1	HUD_INTR	AUX BIT_2	VSS	A
B	MEM_A10	VCCIO_1	VSS	DMD_JTCK	DMD_DAD_BUS	DMD_SCTRL	DMD_TRC	DMD_D12	DMD_D9	DMD_D7	DMD_D3	DMD_D0	AUX BIT_7	AUX BIT_1	VCCIO_3	LED_S_EN	B
C	MEM_A1	MEM_WEZ	MEM_RST	DMD_JTDO	DMD_JTMS	VSS	DMD_LOADB	DMD_D13	VSS	DMD_D4	DMD_PWR_EN	VSS	AUX BIT_0	HTR_ENABLE	LED_B_EN	LED_R_EN	C
D	MEM_A11	MEM_A3	MEM_RASZ	VCCIO_1	DMD_JTDI	VCCIO_2	DMD_DAD_STRB	VCCIO_2	DMD_D6	VCCIO_2	AUX BIT_6	VCCIO_2	LED_COMPZ	LED_G_EN	LEDDRV_ON	LED_B_PWM	D
E	MEM_A9	MEM_A12	VSS	MEM_ODT								VCCIO_3	LED_D_EN	LED_R_PWM	FLASH_MOSI	FLASH_SCLK	E
F	MEM_CLKZ	MEM_CLK	MEM_A8	MEM_A2								VSSA (PLL)	LED_G_PWM	FLASH_MISO	FLASH_CSZ	LED_EN	F
G	MEM_A5	MEM_A6	MEM_A7	VCCIO_1			VSS	VDD	VDD	VSS		VCCA (PLL)	PWR GOOD	PLL_REFCLK_O	PLL_REFCLK_I	HW TEST_EN	G
H	MEM_A0	MEM_A4	VSS	MEM_VREF0			VDD	VSS	VSS	VDD		TSTPT_6	RESETZ	TSTPT_7	TSTPT_5	TSTPT_4	H
J	MEM_BA0	MEM_BA1	MEM_CASZ	MEM_ZQ			VDD	VSS	VSS	VDD		VDDQ	JTAG RSTZ	TSTPT_1	TSTPT_2	TSTPT_3	J
K	MEM_CKE	MEM_CSZ	MEM_ATO	VCCIO_1			VSS	VDD	VDD	VSS		VSS	TMP_SDA	JTAG TDO	JTAG TDI	TSTPT_0	K
L	MEM_DQ7	MEM_DQ6	MEM_DQ4	VSS								AST_CLR0	AST_INTR0	VCCIO_3	JTAG TCK	JTAG TMS	L
M	MEM_DQ5	MEM_DQ3	VCCIO_1	MEM_DTO0								AST_CLR1	AST_HLD0	AST_INTR1	I2C_SCL_2	TMP_SCL	M
N	MEM_DQS0	MEM_DQSZ0	VSS	MEM_DTO1	VCCIO_1	MEM_VREF1	VSS	P_DATAEN	PDATA [4]	VCCIO_3	PDATA [14]	PDATA [19]	PDATA [21]	VSS	I2C_SDA_1	I2C_SDA_2	N
P	MEM_DQ2	MEM_DQ0	VCCIO_1	VSS	MEM_DQ12	VSS	P_VSYNC	P_HSYNC	VSS	PDATA [7]	PDATA [10]	PDATA [13]	VCCIO_3	PDATA [22]	PDATA [23]	I2C_SCL_1	P
R	MEM_DQ1	VSS	MEM_DQ15	MEM_DQS1	MEM_DQ11	MEM_DQ9	VCCIO_1	PDATA [0]	PDATA [2]	PDATA [5]	PDATA [8]	PDATA [11]	PDATA [15]	PDATA [18]	PDATA [20]	AST_HLD1	R
T	VSS	MEM_DQ14	MEM_DQ13	MEM_DQSZ1	MEM_DQ10	MEM_DQ8	VSS	PCLK	PDATA [1]	PDATA [3]	PDATA [6]	PDATA [9]	PDATA [12]	PDATA [16]	PDATA [17]	VSS	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

DLPC120-Q1 Device Initialization and Programming Pin Descriptions

PIN		I/O	I/O	CLOCK	
NAME	NO.	POWER	TYPE	SYSTEM	DESCRIPTION
RESETZ	H13	3.30 V	I_2	Async	Functional Reset (Active Low). Resets internal logic and causes PLL startup and PLL locking. Assertion is required after power supplies are within limits. See Power Supply and Reset Timing Requirements for timing requirements.
PWRGOOD	G13		I_2	Async	System Power Good indicator. Should be held low until all DLPC120-Q1 power has been within operating limits. See Power Supply and Reset Timing Requirements for timing requirements. Must be set high to enable normal operation. When set low, the DLPC120-Q1 begins the parking routine for the DMD. Together with pin E14 (LED_R_PWM / PWRGOOD_CNTRL), this signal is critical for DLP3030-Q1 parking as part of the Pre-Conditioning Sequence and subsequent un-parking. See *DLPC120-Q1 Programmer's Guide* for implementation details.
PLL_REFCLK_I	G15		I_2	N/A	Reference Clock Input (16 MHz). Can be driven by crystal across this pin and PLL_REFCLK_O or by external oscillator. See Power Supply and Reset Timing Requirements for timing requirements.
PLL_REFCLK_O	G14		O_6	N/A	Crystal output. Used with PLL_REFCLK_I.
HUD_INTR	A14		O_6	N/A	Interrupt signal. This active high signal indicates one of the interrupt sources in the controller has been triggered.
IIC_SCL_1	P16		B_8	N/A	I^2C Clock for Device configuration and control. Requires external pull-up. Port 1 Slave command/control interface.
IIC_SDA_1	N15		B_8	N/A	I^2C Data for Device configuration and control. Requires external pull-up. Port 1 Slave command/control interface.
IIC_SCL_2	M15		B_8	N/A	I^2C Clock Debug Port. Requires external pull-up. Port 2 Slave command/control interface.
IIC_SDA_2	N16		B_8	N/A	I^2C Data Debug Port. Requires external pull-up. Port 2 Slave command/control interface.
FLASH_MISO	F14		I_2	FLASH_SCLK	Serial Data input from the external SPI Flash device. This provides device logical programming data as well as functional configuration parameter data.
FLASH_CSZ	F15		O_6	FLASH_SCLK	Chip Select output for the external SPI Flash device. Active low.
FLASH_SCLK	E16		O_6	N/A	Clock for the external SPI Flash device.
FLASH_MOSI	E15		O_6	FLASH_SCLK	Serial Data output to the external SPI Flash device. This pin sends address and control information as well as data when programming.

LED Driver Interface

PIN		I/O	I/O	CLOCK	
NAME	NO.	POWER	TYPE	SYSTEM	DESCRIPTION
LED_B_PWM	D16	3.30 V	O_6	N/A	Function reserved for future use.
LED_R_PWM (PWRGOOD_CNTRL)	E14		O_6	N/A	Re-purposed for Power Good control. Together with pin G13 (PWRGOOD), this signal is used for DLP3030-Q1 parking as part of Pre-Conditioning Sequence and subsequent un-parking. See *DLPC120-Q1 Programmer's Guide* for implementation details.
LED_G_PWM	F13		O_6	N/A	Function reserved for future use.
LED_B_EN	C15		O_6	N/A	Blue LED Enable Strobe. Controlled by programmable DMD Sequence Timing (Active High).
LED_R_EN	C16		O_6	N/A	Red LED Enable Strobe. Controlled by programmable DMD Sequence Timing (Active High).
LED_G_EN	D14		O_6	N/A	Green LED Enable Strobe. Controlled by programmable DMD Sequence Timing (Active High).
LED_S_EN	B16		O_6	N/A	LED Shunt Enable. Controlled by programmable DMD Sequence Timing (Active High).
LED_D_EN	E13		O_6	N/A	LED Drive Enable. Controlled by programmable DMD Sequence Timing (Active High).
LEDDRV_ON	D15		O_6	Async	LED Driver Enable. Active high output control to external LED Drive Logic.
LED_EN	F16		I_2	Async	LED Enable (Active high input). A logic low on this signal will force LEDDRV_ON low and RGB Strobes low. These signals will be enabled 100 msec after LED_EN transitions to a high (assuming corresponding SW parameters are also set to enable LED operation).
LED_COMPZ	D13		I_2	Async	LED Threshold Compare (Active low input). A logic low on this signal will indicate a threshold has been reached and in discontinuous mode will control shunt enable (LED_S_EN).
AST_CLR0	L12		O_6	N/A	Function reserved for future use.
AST_HLD0	M13		O_6	N/A	Function reserved for future use.
AST_INTR0	L13		O_6	N/A	Sequence Timer Interrupt port.
AST_CLR1	M12		O_6	N/A	Function reserved for future use.
AST_HLD1	R16		O_6	N/A	Function reserved for future use.
AST_INTR1	M14		O_6	N/A	Function reserved for future use.

DMD Temperature and Heater Control

PIN		I/O	I/O	CLOCK	
NAME	NO.	POWER	TYPE	SYSTEM	DESCRIPTION
TMP_SDA	K13	3.30 V	B_8	Async	Temperature Control Serial Data. This signal is used to communicate with the TMP411 to read the temperature values. Follows I^2C protocol as required by TMP411.
TMP_SCL	M16		B_8	Async	Temperature Control Serial Clock. This signal is used to communicate with the TMP411 to read the temperature values. Follows I^2C protocol as required by TMP411.
HTR_ENABLE	C14		O_6	Async	Heater Enable Control. This PWM signal is used to control the package heater for the DLP3000-Q1 device, and it is not required for the DLP3030-Q1 device.

General Purpose I/O

PIN		I/O	I/O	CLOCK	
NAME	NO.	POWER	TYPE	SYSTEM	DESCRIPTION
AUXBIT_0 (FLICKER_SELECT)	C13	3.30 V	O_6	Async	This pin is configured by default to be asserted at the lowest brightness mode, in order to activate flicker reduction logic in the LED driver circuit. It is de-asserted otherwise, in order to de-active the flicker reduction logic for normal operation. Contact a TI Applications Engineer for implementation details.
AUXBIT_1	B14		O_6	Async	DMD Sequencer Reset AUX Bit 1. Intended for system debug. Can be routed to testpoint or left unconnected.
AUXBIT_2	A15		O_6	Async	DMD Sequencer Reset AUX Bit 2. Intended for system debug. Can be routed to testpoint or left unconnected.
AUXBIT_6	D11		O_6	Async	DMD Sequencer Reset AUX Bit 6. Intended for system debug. Can be routed to testpoint or left unconnected.
AUXBIT_7	B13		O_6	Async	DMD Sequencer Reset AUX Bit 7. Intended for system debug. Can be routed to testpoint or left unconnected.

Main Video and Data Control Interface

PIN		I/O	I/O	CLOCK	
NAME	NO.	POWER	TYPE	SYSTEM	DESCRIPTION
PCLK	T8	3.30 V	I_2	N/A	Pixel Clock(1)
P_VSYNC	P7		I_2	PCLK	Vertical sync(2)
P_HSYNC	P8		I_2		Horizontal sync(2)
P_DATAEN	N8		I_2		Data Valid(2)
PDATA[0]	R8		I_2		Data(3)
PDATA[1]	T9		I_2		
PDATA[2]	R9		I_2		
PDATA[3]	T10		I_2		
PDATA[4]	N9		I_2		
PDATA[5]	R10		I_2		
PDATA[6]	T11		I_2		
PDATA[7]	P10		I_2		
PDATA[8]	R11		I_2		
PDATA[9]	T12		I_2		
PDATA[10]	P11		I_2		
PDATA[11]	R12		I_2		
PDATA[12]	T13		I_2		
PDATA[13]	P12		I_2		
PDATA[14]	N11		I_2		
PDATA[15]	R13		I_2		
PDATA[16]	T14		I_2		
PDATA[17]	T15		I_2		
PDATA[18]	R14		I_2		
PDATA[19]	N12		I_2		
PDATA[20]	R15		I_2		
PDATA[21]	N13		I_2		
PDATA[22]	P14		I_2		
PDATA[23]	P15		I_2		

(1) Pixel clock capture edge is software programmable.
(2) VSYNC, HSYNC, and Data Valid polarity are software programmable.
(3) The 24-bit PDATA bus can be mapped based on pixel format. By default PDATA[23-16]=Red[7-0], PDATA[15-8]=Green[7-0], and PDATA[7-0]=Blue[7-0]. See *DLPC120-Q1 Programmer's Guide* for more information.

DMD Interface

PIN		I/O	I/O	CLOCK	
NAME	NO.	POWER	TYPE	SYSTEM	DESCRIPTION
DMD_D0	B12	1.80 V	O_5	DMD_DCLK	DMD Data Pins. DMD Data pins are DDR (Double Data Rate) signals that are clocked on both edges of DMD_DCLK.
DMD_D1	A13				
DMD_D2	A12				
DMD_D3	B11				
DMD_D4	C10				
DMD_D5	A11				
DMD_D6	D9				
DMD_D7	B10				
DMD_D8	A10				
DMD_D9	B9				
DMD_D10	A9				
DMD_D11	A8				
DMD_D12	B8				
DMD_D13	C8				
DMD_D14	A7				
DMD_DCLK	A6		O_5	N/A	DMD Data Clock (DDR).
DMD_LOADB	C7		O_5	DMD_DCLK	DMD Data Load Signal (Active Low).
DMD_SCTRL	B6		O_5	DMD_DCLK	DMD Data Serial Control Signal.
DMD_TRC	B7		O_5	DMD_DCLK	DMD Data Toggle Rate Control.
DMD_DAD_OEZ	A5		O_5	Async	DMD DAD Output Enable (Active Low). A pull up (10 kΩ to 100 kΩ) to the 1.8 V rail for the DMD interface is needed to keep this signal inactive when tristated.
DMD_DAD_BUS	B5		O_5	DMD_SAC_CLK	DMD DAD Bus Data.
DMD_DAD_STRB	D7		O_5	DMD_DCLK	DMD DAD Bus Strobe.
DMD_SAC_BUS	A4		O_5	DMD_SAC_CLK	DMD SAC Bus Data.
DMD_SAC_CLK	A3		O_5	N/A	DMD SAC Bus Clock.
DMD_JTCK	B4		O_4	N/A	DMD Interface Test Clock. Signal connected to DMD JTAG interface to allow the verification of the interface. Interface is tri-stated when not active.
DMD_JTMS	C5		O_4	N/A	DMD Interface Test Mode. Signal connected to DMD JTAG interface to allow the verification of the interface. Interface is tri-stated when not active.
DMD_JTDI	D5		O_4	N/A	DMD Interface Test Data output. Signal connected to DMD JTAG interface to allow the verification of the interface. This signal connects to the DMD JTAG TDI. Interface is tri-stated when not active.
DMD_JTDO	C4		I_1	N/A	DMD Interface Test Data input. Signal connected to DMD JTAG interface to allow the verification of the interface. This signal connects to the DMD JTAG TDO. Internal Pull down.
DMD_PWR_EN	C11	3.30 V	O_6	Async	DMD Power Regulator Enable (Active High).

Memory Interface

PIN		I/O	I/O	CLOCK	
NAME	NO.	POWER	TYPE	SYSTEM	DESCRIPTION
MEM_CLK	F2	1.80 V	O_S	N/A	DDR memory, Differential Memory Clock.
MEM_CLKZ	F1				
MEM_A0	H1		O_S	MEM_CLK	DDR memory, Multiplexed Row and Column Address.
MEM_A1	C1				
MEM_A2	F4				
MEM_A3	D2				
MEM_A4	H2				
MEM_A5	G1				
MEM_A6	G2				
MEM_A7	G3				
MEM_A8	F3				
MEM_A9	E1				
MEM_A10	B1				
MEM_A11	D1				
MEM_A12	E2				
MEM_BA0	J1		O_S	MEM_CLK	DDR memory, Bank Select.
MEM_BA1	J2				
MEM_RASZ	D3		O_S	MEM_CLK	DDR memory, Row Address Strobe (Active low).
MEM_CASZ	J3		O_S	MEM_CLK	DDR memory, Column Address Strobe (Active low).
MEM_WEZ	C2		O_S	MEM_CLK	DDR memory, Write Enable (Active low).
MEM_CSZ	K2		O_S	MEM_CLK	DDR memory, Chip Select (Active low).
MEM_CKE	K1		O_S	MEM_CLK	DDR memory, Clock Enable (Active high).
MEM_ODT	E4		O_S	MEM_CLK	DDR memory, On die termination (ODT). ODT is not verified and supported operational mode. This pin should be left open or connected to corresponding DDR2 pin.
MEM_RST	C3		O_S	MEM_CLK	DDR memory, Reset. Do Not connect.
MEM_ZQ	J4		O_S	MEM_CLK	DDR memory, External pad where to connect the external impedance calibration resistor. The user connects the PAD pin through an external 240 Ω ± 1% resistor to ground.
MEM_DQS0	N1		B_{SD}	N/A	DDR memory, Lower Byte, R/W Data Strobe.
MEM_DQSZ0	N2		B_{SD}	N/A	DDR memory, Lower Byte, R/W Data Strobe, inverted.
MEM_DQ0	P2		B_S	MEM_DQS0	DDR memory, Lower Byte, Bidirectional R/W Data.
MEM_DQ1	R1				
MEM_DQ2	P1				
MEM_DQ3	M2				
MEM_DQ4	L3				
MEM_DQ5	M1				
MEM_DQ6	L2				
MEM_DQ7	L1				

Memory Interface (continued)

PIN		I/O	I/O	CLOCK	
NAME	NO.	POWER	TYPE	SYSTEM	DESCRIPTION
MEM_DQS1	R4	1.80 V	B_S	N/A	DDR memory, Upper Byte, R/W Data Strobe.
MEM_DQSZ1	T4		B_{SD}	N/A	DDR memory, Upper Byte, R/W Data Strobe, inverted.
MEM_DQ8	T6		B_S	MEM_DQS1	DDR memory, Upper Byte, Bidirectional R/W Data.
MEM_DQ9	R6				
MEM_DQ10	T5				
MEM_DQ11	R5				
MEM_DQ12	P5				
MEM_DQ13	T3				
MEM_DQ14	T2				
MEM_DQ15	R3				

Board Level Test and Debug

PIN		I/O	I/O	CLOCK	
NAME	NO.	POWER	TYPE	SYSTEM	DESCRIPTION
JTAGRSTZ	J13	3.30 V	I_2	Async	JTAG, Reset. Includes weak internal pull-up. Holds TAP controller and associated JTAG logic in idle state under normal operation. **This pin should be pulled down with a 5 kΩ or smaller resistor for normal operation.**
JTAGTDI	K15		I_2	JTAGTCK	JTAG, Serial Data In. Includes weak internal pull-up.
JTAGTCK	L15		I_2	N/A	JTAG, Serial Data Clock. Includes weak internal pull-up.
JTAGTMS	L16		I_2	JTAGTCK	JTAG, Test Mode Select. Includes weak internal pull-up.
JTAGTDO	K14		O_6	JTAGTCK	JTAG, Serial Data Out.

Manufacturing Test Support

PIN		I/O	I/O	CLOCK	
NAME	NO.	POWER	TYPE	SYSTEM	DESCRIPTION
HWTEST_EN	G16	3.30 V	I_2	N/A	Manufacturing Test Enable signal. Should be connected directly to ground on the PCB for normal operation. Weak Internal Pulldown.
MEM_ATO	K3	N/A	O	N/A	Memory Controller Analog Test Output. Factory Test purposes only, should be left unconnected in system.
MEM_DTO0	M4	3.30 V	O_S	N/A	Memory Controller Digital Test Output #1. Factory Test purposes only, should be left unconnected in system.
MEM_DTO1	N4	3.30 V	O_S	N/A	Memory Controller Digital Test Output #2. Factory Test purposes only, should be left unconnected in system.

Test Point Interface

PIN		I/O	I/O	CLOCK	
NAME	NO.	POWER	TYPE	SYSTEM	DESCRIPTION
TSTPT_0	K16	3.30 V	B_8	Async	Reserved for Test Outputs. These test I/O should be left open or unconnected for normal operation in final product design. (DO NOT tie to GND), Internal Pullup on all signals. **TSTPT_4 should be pulled up using external 10 kΩ resistor to ensure proper initialization**.
TSTPT_1	J14				
TSTPT_2	J15				
TSTPT_3	J16				
TSTPT_4	H16				
TSTPT_5	H15				
TSTPT_6	H12				
TSTPT_7 (CM_DM)	H14	3.30 V	B_8	Async	This pin is configured by default to indicate whether the system is in Continuous Mode (High) or Discontinuous Mode (Low). Contact a TI Applications Engineer for implementation details. It can also be reserved as a Test Output.

Power and Ground

PIN		I/O	
NAME	**NO.**		**DESCRIPTION**
VCCIO_1	B2, D4, G4, K4, M3, N5, P3, R7	PWR	1.8 V (DDR2 MEM).
VCCIO_2	BA2, D10, D12, D6, D8	PWR	1.8 V (DMD I/F).
VCCIO_3	B15, E12, L14, N10, P13	PWR	3.3 V (MISC IO).
MEM_VREF0	H4		Voltage Referenced Input (50% of DDR Memory Voltage).
MEM_VREF1	N6		Voltage Referenced Input (50% of DDR Memory Voltage).
VCCA	G12	PWR	PLL Power Input.
VSSA	F12		PLL R-C Return Path (NOT a GND).
VDD	G8, G9, H7, H10, J7, J10, K8, K9	PWR	1.2-V core logic power supply.
VDDQ	J12	GND	EFUSE Programming voltage (Used in Manufacturing Test only.) Should be tied to GND.
GND	A1, A16, B3, C6, C9, C12, E3, G7, G10, H3, H8, H9, J8, J9, K7, K10, K12, L4, N3, N7, N14, P4, P6, P9, R2, T1, T7, T16	GND	Common Ground (I/O Ground).

Table 1. I/O Type Subscript Definition

I/O		SUPPLY REFERENCE
SUBSCRIPT	**DESCRIPTION**	
1	1.8 V	VDD
2	3.3 V	VCCIO_3
4	8 mA	VDD
5	6, 10, or 12 mA	VCCIO_2
6	8 mA	VCCA
S	SSTL_18	VCCIO_1
8	8 mA	VCCIO_3
SD	SSTL_18 Differential	VCCIO_1
TYPE		
I	Input	N/A
O	Output	
B	Bidirectional	
PWR	Power	
GND	Ground return	

Table 2. Internal Pullup and Pulldown Characteristics(1)

INTERNAL PULL-UP AND PULL-DOWN RESISTOR CHARACTERISTICS	VCCIO	MIN	TYP	MAX	UNIT
Weak pull-up resistance	3.3 V	27	39	61	kΩ
Weak pull-down resistance	3.3 V	32	46	79	kΩ
	1.8 V	52	91	180	kΩ

(1) The resistance is dependent on the supply voltage level applied to the I/O.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) (1)

		MIN	MAX	UNIT
SUPPLY VOLTAGE(2)				
VCCIO_1		0	1.98	V
VCCIO_2		0	3.6	V
VCCIO_3		0	3.6	V
VCCA (PLL)		0	1.32	V
VDD		0	1.32	V
GENERAL				
T_J	Operating junction temperature	–40	125	°C
T_{stg}	Storage temperature	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (A1, A16, T1, and T16)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	1.2-V supply voltage, core logic	1.14	1.2	1.26	V
VCCA	Analog voltage for PLL	1.14	1.2	1.26	V
VCCIO_0	DDR2 memory interface	1.71	1.8	1.89	V
VCCIO_1	1.8-V supply voltage for DMD	1.71	1.8	1.89	V
VCCIO_2	Pixel interface supply voltage	3.135	3.3	3.465	V
VDDQ	EFuse programming voltage	0.0	0.0	0.0	V
T_J	Operating junction temperature	–40		125	°C
T_A	Operating ambient temperature (1)	–40		105	°C

(1) Operating ambient temperature is dependent on system thermal design. Operating junction temperature may not exceed its specified range across ambient temperature conditions.

6.4 Thermal Information (1)

THERMAL METRIC (2)		DLPC120-Q1 ZXS (BGA) 216 PINS	UNIT
ψ_{JT}	Case-to-junction thermal coefficient	0.28	°C/W
T_{JA}	Junction-to-ambient thermal coefficient	26.32	°C/W

(1) TI recommends customers refer to JEDEC Standard J-STD-020D for information regarding solder reflow profiles. The peak reflow temperature for DLPC120-Q1 is 260°C.
(2) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD}	Logic core power (1.2 V)			140	186	mA
I_{VCCA}	PLL power (1.2 V)			3	10	mA
$I_{VCCIO\_0/1}$	DDR2 memory and DMD interface I/O power (1.8 V)			180	245	mA
I_{VCCIO_2}	Pixel data input power (3.3 V)			4	10	mA
	Total power			469	724	mW

6.6 Electrical Characteristics for I/O(1)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input threshold voltage	1.8-V LVCMOS (I/O Type 1)		1.17		VCCIO + 0.3	V
		3.3-V LVCMOS (I/O Type 2, 8)		2.0		VCCIO + 0.3	
		SSTL_18 (I/O Type S, SD)		1.08		VCCIO + 0.3	
V_{IL}	Low-level input threshold voltage	1.8-V LVCMOS (I/O Type 1)		–0.3		0.63	V
		3.3-V LVCMOS (I/O Type 2, 8)		–0.3		0.8	
		SSTL_18 (I/O Type S, SD)		–0.3		0.73	
V_{OH}	High-level output voltage	1.8-V LVCMOS fixed current (I/O Type 4)		1.35			V
		1.8-V LVCMOS variable current (I/O Type 5)		1.35			
		3.3-V LVCMOS fixed current (I/O Type 6, 8)		2.4			
		SSTL_18 (I/O Type S, SD)		VCCIO – 0.28			
V_{OL}	Low-level output voltage	1.8-V LVCMOS fixed current (I/O Type 4)				0.45	V
		1.8-V LVCMOS variable current (I/O Type 5)				0.45	
		3.3-V LVCMOS fixed current (I/O Type 6, 8)				0.4	
		SSTL_18 (I/O Type S, SD)				0.28	

(1) See Table 1 for a definition of the different I/O subscript types.

6.7 Power Supply and Reset Timing Requirements

			MIN	MAX	UNIT
t_{ramp}	Time for all DLPC120-Q1 power rails to be applied	Power supplies can be applied in any order if they occur within this maximum timing. Otherwise, refer to Note (1).		10	ms
t_{pwr_en}	RESETZ rising edge (or PWRGOOD rising edge—whichever comes second) to DMD_PWR_EN rising edge	For the DLP3030-Q1, PWRGOOD shall be controlled by LED_R_PWM / PWRGOOD_CNTRL signal, which is an output of the DLPC120-Q1 and will automatically be asserted after the device releases from reset.		150	µs
t_{dly}	External delay between DMD_PWR_EN and DMD mirror supply voltages	This delay is required for the DLP3000-Q1. For the DLP3030-Q1, there are no delay requirements.	2.5	4.5	ms
t_{oez}	DMD_PWR_EN rising edge to falling edge of DMD_OEZ			5	ms

(1) If the DLPC120-Q1 supplies cannot be applied according to this timing specification, then they must be applied in the following order, spanning no longer than 100 ms (shall be removed in the reverse order for power down):
(a) Apply VCCIO_2 (3.3 V)
(b) Apply VCCIO_0, VCCIO_1 (1.8 V) DDR Memory and DMD, in any order
(c) Apply VDD (1.2 V) DLPC120-Q1 core supply voltage

Power Supply and Reset Timing Requirements (continued)

			MIN	MAX	UNIT
$t_{precondition}$	DMD preconditioning time	For the DLP3030-Q1, it is required that the DMD executes a Pre-Conditioning Sequence prior to parking. The final action of this sequence is the de-assertion of the LED_R_PWM / PWRGOOD_CNTRL signal, which shall drive the PWRGOOD signal low. See the *DLPC120-Q1 Programmer's Guide* for instructions on how to execute the Pre-Conditioning Sequence.	800		µs
t_{park}	DMD park time (approximate)		200	200	µs
t_{pd_dmd}	PWRGOOD low to falling edge of DMD_PWR_EN			500	µs
t_{fall}	Time for DLPC120-Q1 power supplies to be removed	Power supplies can be removed in any order if they occur within this maximum timing. Otherwise, they shall be removed in the reverse order they were applied, per the t_{ramp} specification and Note (1).		10	ms

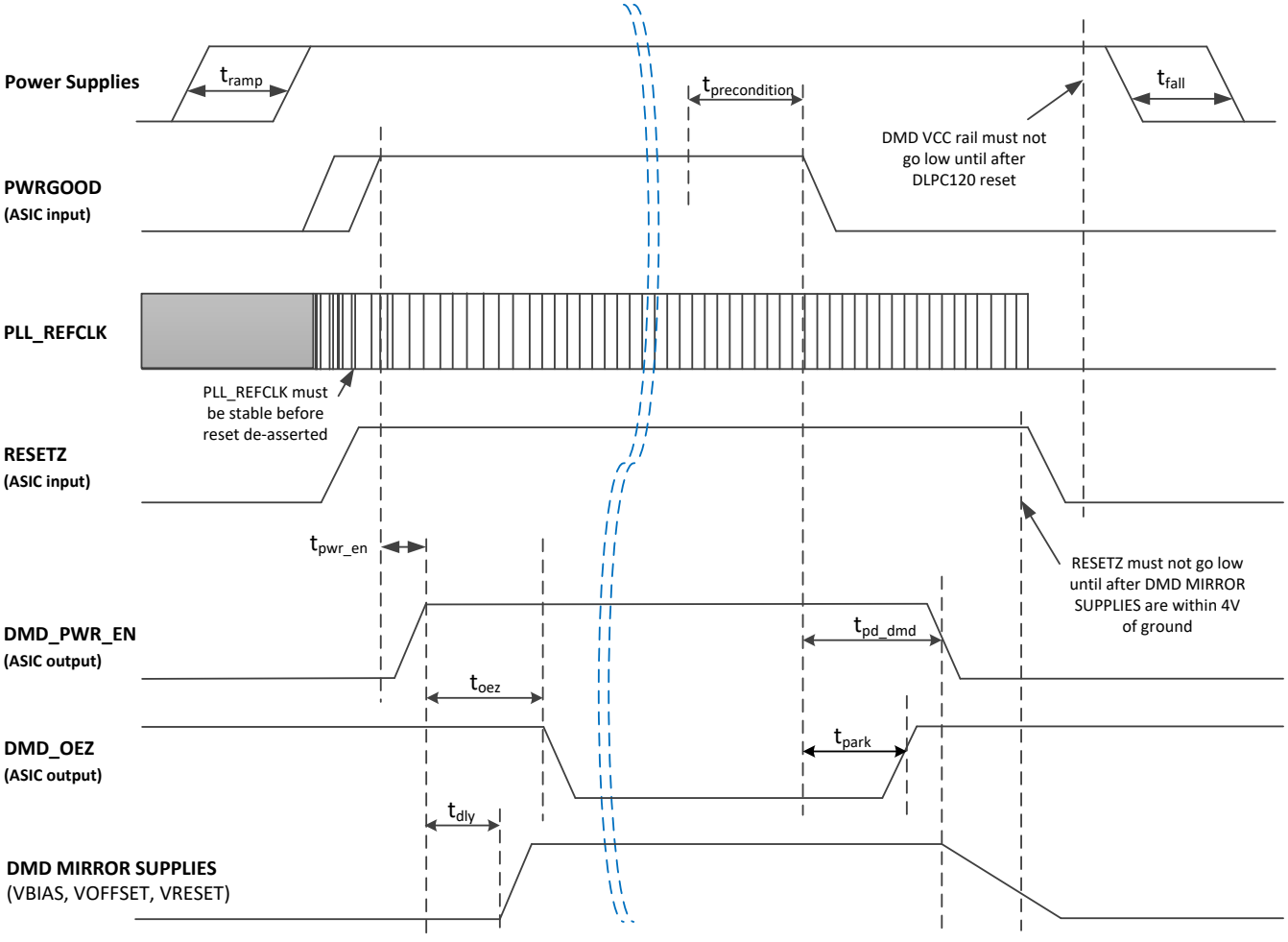


Figure 1. Power Supply and RESETZ Timing

6.8 Reference Clock PLL Timing Requirements

		MIN	NOM	MAX	UNIT
f_{clock}	Clock frequency		16.00		MHz

Reference Clock PLL Timing Requirements (continued)

			MIN	NOM	MAX	UNIT
t_c	Cycle time	No clock spreading (1)		62.5		ns
		With clock spreading (1)		1.02 × t_c		ns
t_w(H)	Pulse duration, high	50% to 50% reference points	0.4 x t_c			ns
t_w(L)	Pulse duration, low	50% to 50% reference points	0.4 x t_c			ns
t_{jp}	Period jitter, PLL_REFCLK_I		–250		250	ps

(1) PLL clock spreading is configurable. See *DLPC120-Q1 Programmer's Guide* for a description of how to select spread spectrum options.

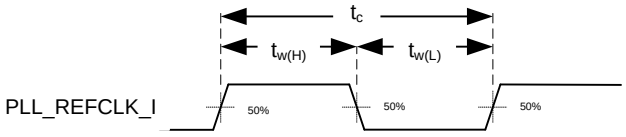


Figure 2. PLL Reference Clock Timing

6.9 Parallel Interface General Timing Requirements

			MIN	MAX	UNIT
f_{clock}	Clock frequency, PCLK (1)		3.1	40.0	MHz
t_{p_clkper}	Clock period, PCLK	VIH/VIL	25.0	320.0	ns
t_{p_wh}	Pulse width low, PCLK	VIH/VIL	6.0		ns
t_{p_wl}	Pulse width high, PCLK	VIH/VIL	6.0		ns
t_{p_su}	Setup time - HSYNC, DATEN, PDATA(23:0) valid before the active edge of PCLK (2)	VIH/VIL	2.0		ns
t_{p_h}	Hold time - HSYNC, DATEN, PDATA(23:0) valid after the active edge of PCLK (2)	VIH/VIL	2.0		ns
t_t	Transition time - PCLK	10% to 90% reference points	0.2	6	ns

(1) This range includes the 200 ppm of the external oscillator.
(2) The active (capture) edge of PCLK for HSYNC, DATEN, and PDATA(23:0) is software programmable, but defaults to rising edge.

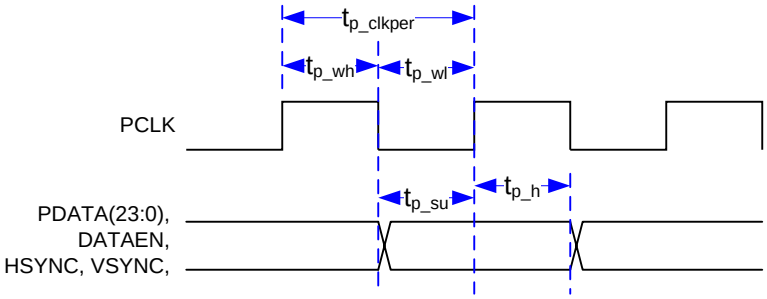


Figure 3. Parallel Video Interface General Timing

6.10 Parallel Interface Frame Timing Requirements (1)

			MIN	MAX	UNIT
t_{p_vsw}	Vertical sync width	50% reference points	1		Lines
t_{p_vbp}	Vertical back porch	50% reference points	6		Lines
t_{vfp}	Vertical front porch	50% reference points	4 (2)		Lines

(1) All values verified at 60-Hz input frame rate.
(2) Values depend on many factors and may need to be higher depending on scaling ratio and other factors. See resolution table for typical values that have been verified.

Parallel Interface Frame Timing Requirements(1) (continued)

			MIN	MAX	UNIT
t_{hsw}	Horizontal sync width	50% reference points	5		PCLKs
t_{hbp}	Horizontal back porch	50% reference points	4		PCLKs
t_{hfp}	Horizontal front porch	50% reference points	40(2)		PCLKs

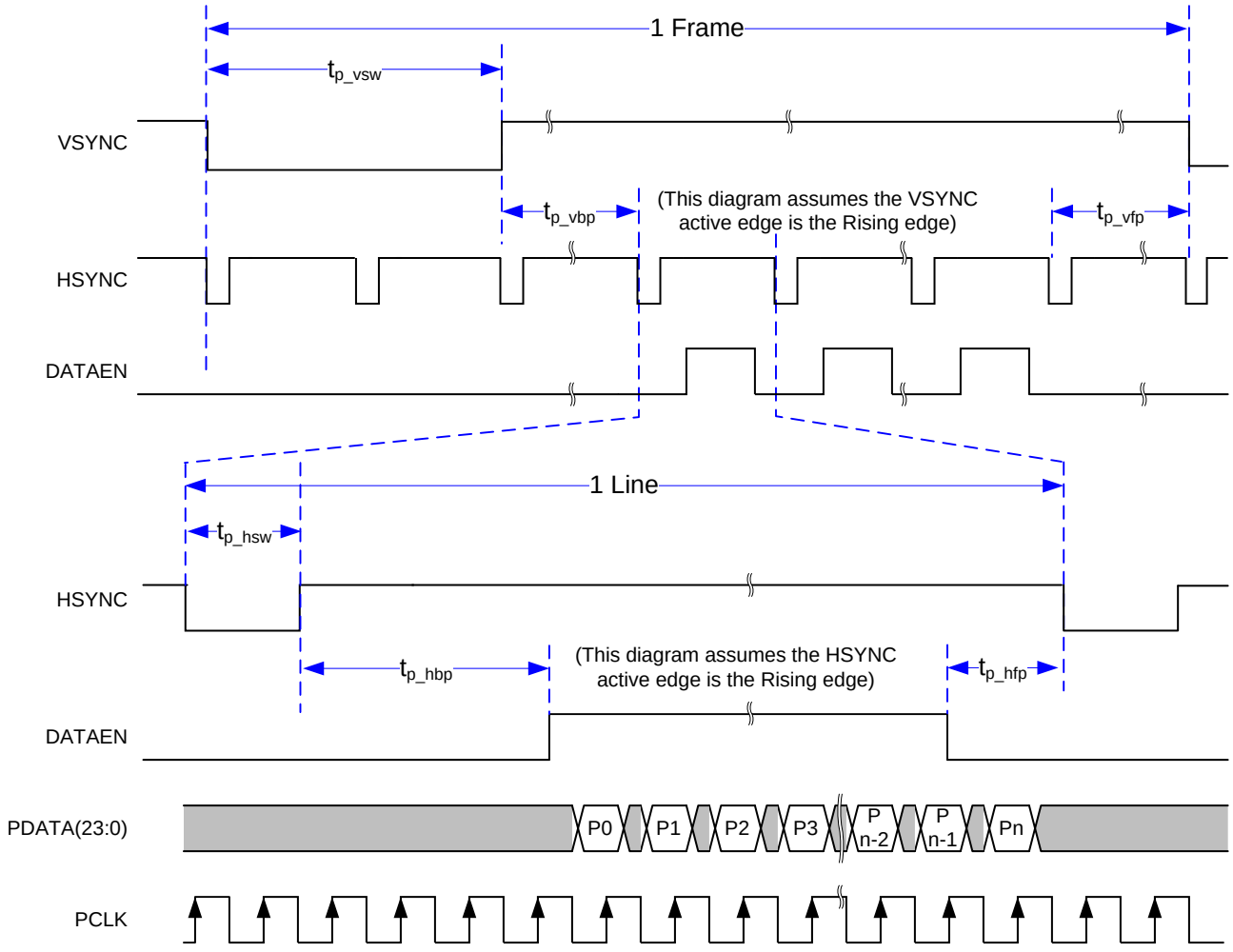


Figure 4. Parallel Interface Frame Timing

6.11 Flash Memory Interface Timing Requirements (1)

			MIN	NOM	MAX	UNIT
f_{clock}	Clock frequency, FLASH_SCLK(2)			39.00		MHz
t_{clkper}	Clock period, FLASH_SCLK	50% reference points		25.64		ns
t_{wh}	Pulse width high, FLASH_SCLK	50% reference points	10			ns
t_{wl}	Pulse width low, FLASH_SCLK	50% reference points	10			ns
t_t	Transition time, all signals	20% to 80% reference points, C_{load} = 20 pF	1		3	ns
t_{valid_MISO}	Flash MISO valid data max delay after FLASH_SCLK falling edge	50% reference points			10	ns

(1) FLASH_CSZ is asserted '1' FLASH_SCLK cycle prior to a write transaction and deasserted '1' FLASH_SCLK after a write transaction.
(2) Spread Spectrum clock modulation, when enabled, will affect the nominal frequency of the FLASH_SCLK.

Flash Memory Interface Timing Requirements (1) (continued)

			MIN	NOM	MAX	UNIT
$t_{valid\_MISO\_b}$	MOSI valid before rising edge of FLASH_SCLK	50% reference points	2.2			ns
$t_{valid\_MISO\_a}$	MOSI valid after rising edge of FLASH_SCLK	50% reference points	5.2			ns

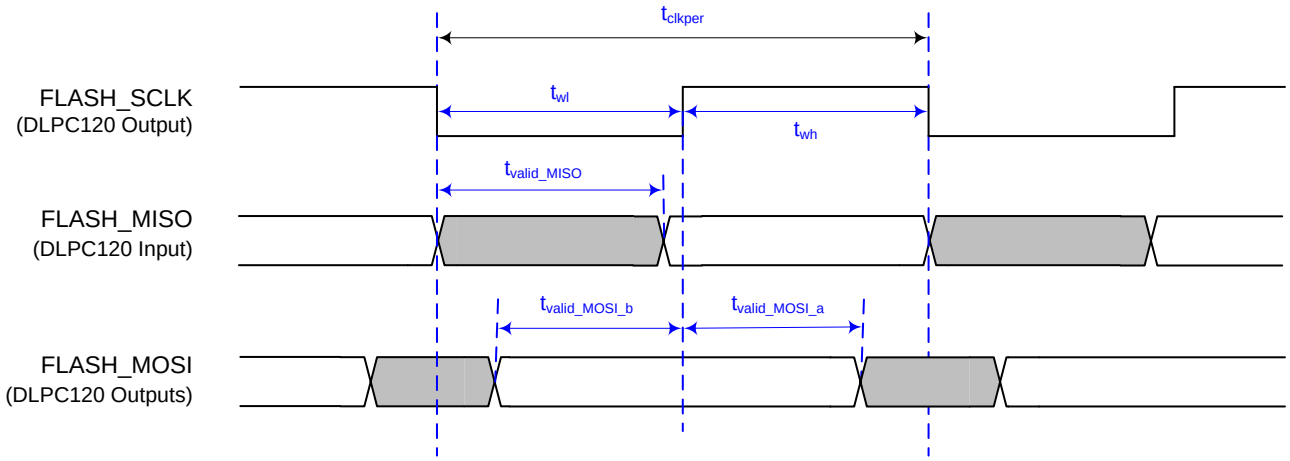


Figure 5. Flash Interface Timing

6.12 DMD Interface Timing Requirements (1)(2)(3)(4)

			MIN	NOM	MAX	UNIT
f_{clock}	Clock frequency, DMD_DCLK and DMD_SAC_CLK (5)		75.00	78.00	80.00	MHz
t_{p_clkper}	Clock period, DMD_DCLK and DMD_SAC_CLK	50% reference points	12.5		15.0	ns
t_{p_clkjit}	Clock jitter, DMD_DCLK and DMD_SAC_CLK	Maximum f_{clock}			200	ps
t_{p_wh}	Pulse width high, DMD_DCLK and DMD_SAC_CLK	50% reference points	6.2			ns
t_{p_wl}	Pulse width low, DMD_DCLK and DMD_SAC_CLK	50% reference points	6.2			ns
t_t	Transition time, all signals	20% to 80% reference points	0.5		1.5	ns
t_{p_su}	Output setup time – DMD_D(14:0), DMD_SCTRL, DMD_LOADB and DMD_TRC relative to both rising and falling edges of DMD_DCLK (6)	50% reference points			1.5	ns
t_{p_h}	Output hold time – DMD_D(14:0), DMD_SCTRL, DMD_LOADB and DMD_TRC signals relative to both rising and falling edges of DMD_DCLK (6)	50% reference points			1.5	ns
$t_{p\_d1\_skew}$	DMD data skew – DMD_D(14:0), DMD_SCTRL, DMD_LOADB and DMD_TRC signals relative to each other	50% reference points			0.20	ns
$t_{p\_d2\_skew}$	DAD/ SAC data skew - DMD_SAC_BUS, DMD_DAD_OEZ and DMD_DAD_BUS signals relative to DMD_SAC_CLK	50% reference points			1.65	ns
$t_{p\_d3\_skew}$	DMD_DAD_STRB signal relative to DMD_DCLK	50% reference points			1.65	ns

(1) Assumes minimum DMD setup time = 1.00 ns and minimum DMD hold time = 1.00 ns.
(2) Assumes DMD Data routing skew = 0.10 ns max.
(3) Assumes a 20-Ω series termination for all DMD interface signals.
(4) TI recommends performing simulations using the DLPC120-Q1 IBIS device model, the DMD IBIS device model, and customer specific PCB/connector interface model to verify system will meet above timing requirements between ASIC and DMD. Information regarding recommendation for PCB design and layout can also be found in Layout.
(5) This range includes the 200 PPM of the external oscillator.
(6) Output setup and hold numbers already account for ASIC clock jitter. Only routing skew and DMD setup/ hold need be considered in system timing analysis.

DMD Interface Timing Requirements(1)(2)(3)(4) (continued)

			MIN	NOM	MAX	UNIT
$t_{p\_clk\_skew}$	Clock skew – DMD_DCLK and DMD_SAC_CLK relative to each other	50% reference points			0.25	ns

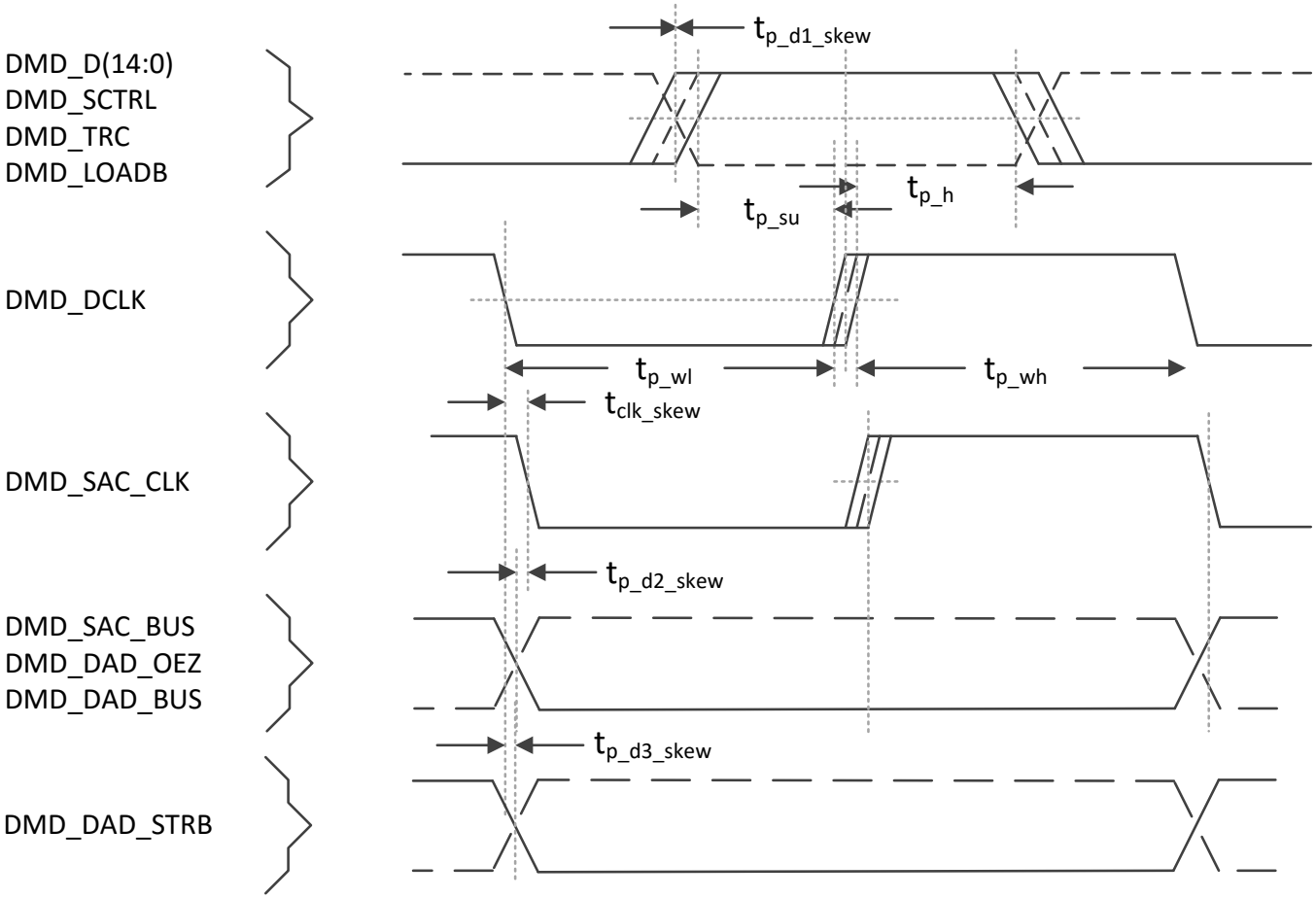


Figure 6. DMD Interface Timing

6.13 JTAG Interface Timing Requirements (1)

			MIN	MAX	UNIT
f_{clock}	Clock frequency, JTAGTCK			10	MHz
t_c	Cycle time, JTAGTCK		100		ns
$t_{w(H)}$	Pulse duration high	50% to 50% reference points	40		ns
$t_{w(L)}$	Pulse duration low	50% to 50% reference points	40		ns
t_t	Transition time, $t_t = t_f = t_r$	20% to 80% reference points		5	ns
t_{su}	Setup time, JTAGTDI valid before JTAGTCK rising edge, and JTAGTMS valid before JTAGTCK rising edge		10		ns
t_h	Hold time, JTAGTDI valid after JTAGTCK, and JTAGTMS valid after JTAGTCK		10		ns
t_{pd}	Output propagation, clock to Q. JTAGTCK falling edge to JTAGTDO		3	20	ns

(1) Switching characteristics over recommended operating conditions, CL (min timing) = 5 pF, CL (max timing) = 25 pF (unless otherwise noted).

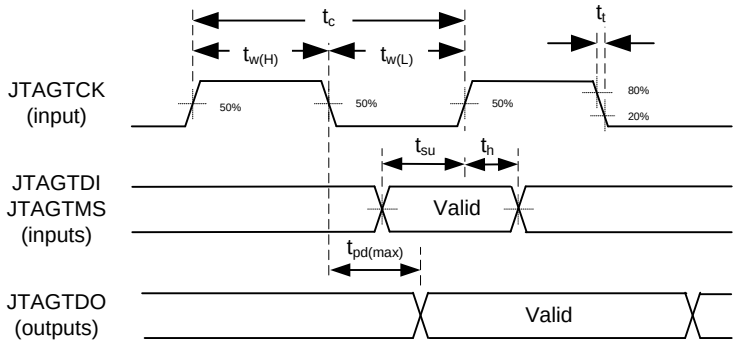


Figure 7. JTAG Interface Timing

6.14 I²C Interface Timing Requirements(1)(2)

		MIN	MAX	UNIT
f_{scl}	Clock frequency	20	400	kHz
t_{sch}	Clock duration high	0.6		µs
t_{scl}	Clock duration low	1.3		µs
t_{sp}	Spike time	0	400	ns
t_{sds}	Setup time	100(3)		ns
t_{sdh}	Hold time	0(4)	0.9(5)	µs
t_{icr}	Input rise time	20 + 0.1 x C_b(6)	300	ns
t_{ocf}	Output fall time	1 + 0.1 x C_b(6)	300	ns
t_{buf}	Bus free time between stop and start conditions	1.3		µs
t_{sts}	Start or repeated start condition setup	0.6		µs
t_{sth}	Start or repeated start condition hold	0.6		µs
t_{sph}	Stop condition hold	0.6		µs

(1) The Phillips I²C Requirements v2.1 should be used as a reference.
(2) The DLPC120-Q1 has three I²C ports. Port 1 and 2 are configured as slaves. Only one of these ports is intended to be used at a time. The unused port is meant for system debug or development purposes. Port 3 is configured as an I²C master and is exclusively designed to work with the TMP411, as described in Temperature Monitor Function. The TMP411 is utilized to monitor the DMD array temperature.
(3) A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, but the requirement t_{SU_DAT} 250 ns must then be met. This is automatically the case since the device does not stretch the LOW period of the SCL signal.
(4) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of SCL.
(5) The maximum t_{HD_DAT} has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
(6) C_b = total capacitance of one bus line in pF.

7 Parameter Measurement Information

7.1 Parallel Interface Input Source Timing

The supported sources with typical timings are shown in Table 3.

Table 3. Parallel Interface Supported Resolutions (Typical Timing)(1)(2)(3)

RESOLUTION		HORIZONTAL			VERTICAL			CLOCK
HORIZONTAL	VERTICAL	FP	BP	SYNC WIDTH	FP	BP	SYNC WIDTH	MHz
320	120	40	32	6	4	7	1	3.1
320	160	42	32	6	7	7	1	4.2
320	240	42	32	6	15	7	1	6.3
400	240	48	50	6	16	6	1	7.8
480	240	96	24	6	8	14	1	9.4
500	250	50	24	6	36	15	1	10.2
640	160	41	41	6	11	19	1	8.3
640	240	104	50	6	14	8	1	12.6
640	480	84	70	6	35	9	1	25.2
800	480	144	50	6	35	9	1	31.5
852	480	68	74	6	35	9	1	31.5
853	480	67	74	6	35	9	1	31.5
854	240	68	72	6	14	9	1	15.8
854	480	68	72	6	35	9	1	31.5
864	480	60	70	6	35	9	1	31.5
960	160	164	70	6	5	9	1	12.6
960	240	164	70	6	13	9	1	18.9
960	250	164	70	6	14	9	1	19.7
960	480	164	70	6	35	9	1	37.8
608	684(4)	46	40	6	104	30	1	33.33

(1) All input timing to DLPC120-Q1 must have a frame rate between 58.0 Hz and 60.0 Hz.
(2) Each input resolution shown is scaled to fill the native resolution of the DMD (864×480) to as many pixels as possible while still maintaining the aspect ratio of the input. For example, the input resolution of 480x240 (aspect ratio of 2:1) would be scaled to and displayed as 854×427 Values assume active low Vsync and Hsync signals. Rising edge is the active edge. If above numbers cannot be met, then it is recommended to extend Front Porch times and reduce Back Porch to adjust.
(3) For proper function, the following equation must be met for any input resolution:
  (a) Horizontal Total Pixels > (PCLK(MHz)/Vertical Total Lines) * 9160
  (b) Horizontal Total Pixels = Active Pixels + Front Porch + Back Porch + Sync Width
  (c) Vertical Total Lines = Active Lines + Front Porch + Back Porch + Sync Width
  (d) 9160 is a constant based on the scaling engine contained in the DLPC120-Q1
  (e) Example calculation for 320x120 resolution:
    (a) Horizontal Total Pixels = 320 + 40 + 32 + 6 = 398
    (b) PCLK = 3.1 MHz
    (c) Vertical Total Lines = 120 + 4 + 7 + 1 = 132
    (d) 398 > (3.1 / 132) * 9160
    (e) 398 > 215, valid input resolution
(4) Optical Bypass Mode.

7.2 Design for Test Functions

The DLPC120-Q1 has several built-in test features. These tests can be run to verify ASIC functionality on startup or during normal operation. Refer to *DLPC120-Q1 Programmer's Guide* for more detail regarding test usage. Table 4 defines the execution time of each test.

Design for Test Functions (continued)

Table 4. Test Execution Times

TEST NAME	LENGTH (ms)	SUMMARY
DDR2 BIST (Short)	145	The Short DDR2 BIST implements a memory check using a March13 Algorithm to verify the external DDR2 SDRAM frame buffer space. It runs at power-up or also can be executed on demand, but it is recommended to run only at power-up, since the image will flash if executed on demand. The short version runs a portion of the long test.
DDR2 BIST (Long)	470	The Long DDR2 BIST is the same as the Short DDR2 BIST, but it runs the test multiple times.
FLASH BIST (1 MByte)	215	The Flash BIST calculates configuration memory checksum (32 bits) for data integrity of the Flash data and interface. Flash checksum is recommended to be done at power-up to verify configuration settings. The Flash BIST memory range to perform checksum is programmable to up to 32M.
System BIST(1)	See(2)	The System BIST validates the DLPC120-Q1 internal logic. It sends a known test pattern image through the ASIC to verify the checksum at the last stage before the data reaches the DMD. When enabled, the checksum for each frame of data is calculated and stored in an I^2C register.
DMD Interface Test	6.93	The DMD JTAG BIST validates the connection between the ASIC and DMD. It uses the DMD JTAG interface to sample the ASIC pins and compare against expected values, and it also tries to detect shorts between signals. The BIST is run on demand.
Front End Video Checksum	See(2)	The Front End Video Checksum is used to verify that the video is received correctly at the front end on the specified region of the frame. When enabled, it calculates the checksum for the specified region of the video frame and stored in an I^2C register.
Video Detect Test	See(2)	The Video Detect test shall be used to monitor external video VSYNC. **If external video is not valid, the DMD must be put into a safe state (e.g. switched to an internal black test pattern).**

(1) Some processing options must be turned off for this test.
(2) The length of these tests will vary depending on frame rate but will not exceed 2 frames.

8 Detailed Description

8.1 Overview

The DLPC120-Q1 is compatible with two DMD components:

- DLP3000-Q1 - 0.3 WVGA TYPE A100 DMD
- DLP3030-Q1 - 0.3 WVGA S450 DMD

The DLPC120-Q1 formats incoming video data from a parallel interface and drives the DMD timing to display the video. It also controls illumination enables to strobe illuminators synchronously with the DMD mirror movement. The DLPC120-Q1 is designed for automotive applications with a wide operating temperature range and diagnostic features to identify certain failure modes.

8.2 Functional Block Diagram

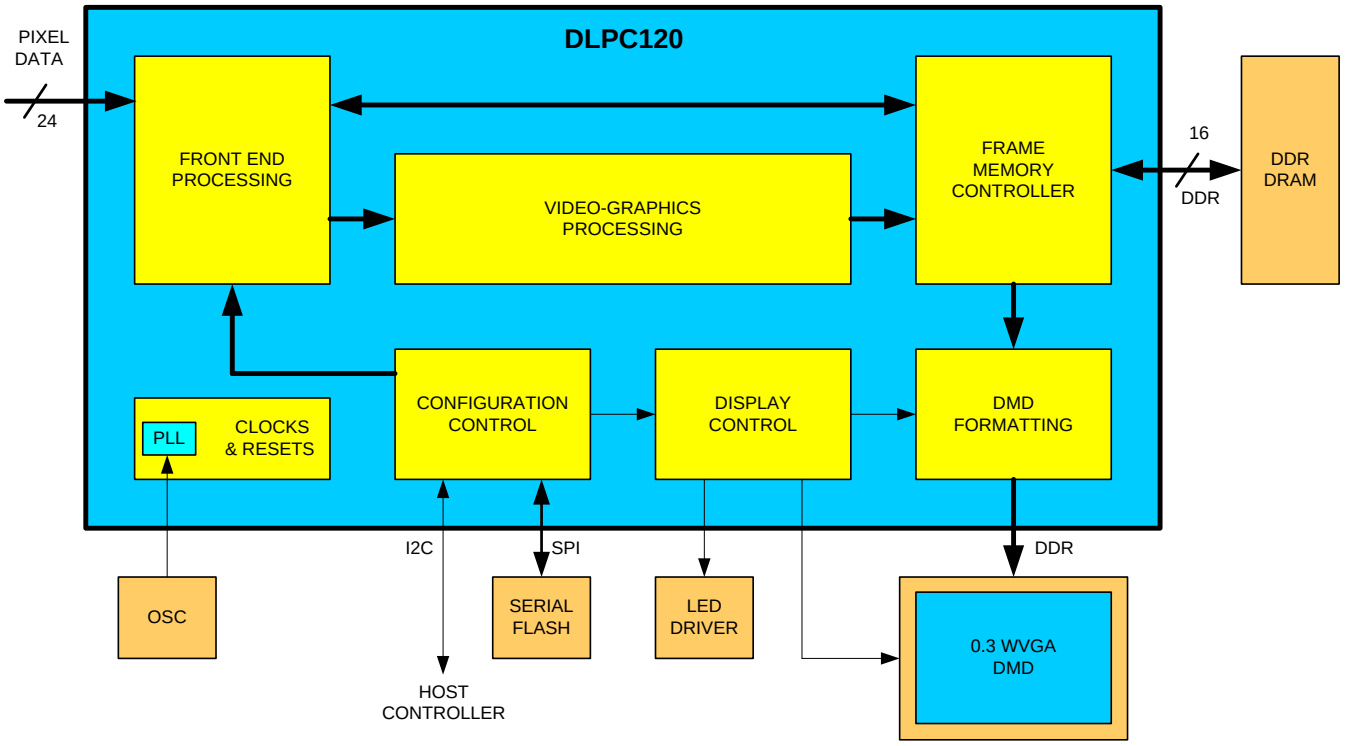


Figure 8. Functional Block Diagram

8.3 Feature Description

8.3.1 Serial Flash Interface

The DLPC120-Q1 utilizes an external SPI serial flash memory device for configuration support. The minimum required size is dependent on the desired minimum number of Sequences, CMT tables, and Splash options, while the maximum supported size is 64 Mb. The DLPC120-Q1 can be used to Read, Erase, and program the serial flash. Refer to *DLPC120-Q1 Programmer's Guide* for details of Flash configuration information.

The DLPC120-Q1 utilizes a single SPI interface, employing SPI mode 0 protocol, operating at a frequency of 39.0 MHz. All read operations assume the Flash supports address auto-incrementing. The DLPC120-Q1 should support any flash device that meets these criteria plus the criteria listed in Table 5.

Feature Description (continued)

Table 5. SPI Flash Instruction Op Code Compatibility Requirements

FLASH COMMAND	OPCODE
Fast Read (Single Output)	0x0B
Read Electronic Signature	0xAB
Others	May vary

The DLPC120-Q1 does not have any specific Page, Block or Sector size requirements. If the user would like to use a portion of the serial flash for storing external data (such as calibration data) via the I^2C interface, then the minimum sector size needs to be considered as it will drive minimum erase size. Note that use of serial flash for storing external data may impact the number of features that can be supported.

The DLPC120-Q1 does not drive the /HOLD (active low Hold) or /WP (active low Write Protect) pins on the flash device and thus these pins should be tied to a logic high on the PCB via an external pull-up.

Table 6. DLPC120-Q1 Compatible SPI Flash Device Options

VENDOR	PART NUMBER	DENSITY (Mb)	SUPPLY VOLTAGE SUPPORTED(1)
ISSI	IS25LP064A-JMLE	64	3.3 V
Winbond	W25Q64CVSFAG	64	3.3 V
Spansion	S25FL064P0XMFV000	64	3.3 V
Micron	M25P64-VMF3TPB	64	3.3 V

(1) The Flash supply voltage must match VCCIO_2 on the DLPC120-Q1. Multiple voltage options are often available under the same base part number.

8.3.2 Serial Flash Programming

The external serial flash may also be programmed via the same SPI interface which is connected to the DLPC120-Q1. In order to avoid conflicting data on this interface, the DLPC120-Q1 must be held in reset while the flash memory is programmed. See flash specification for details of the programming configuration.

8.3.3 DDR2 Memory Interface

The DLPC120-Q1 ASIC DDR2 Memory interface consists of a 16-bit wide, 312-MHz (nominal) DDR2 interface with standard signaling. The DLPC120-Q1 only support DDR2 interface with external termination. The DDR2 interface is a very high speed signaling interface.

A DDR2 memory should be selected that supports the 312-MHz clock frequency and compliant to the JEDEC standard for DDR2 memories (JESD79-2A).

Table 7. Compatible JEDEC DDR2 Devices

PARAMETER	MIN	MAX	UNITS
JEDEC DDR2 device speed grade(1)	DDR2-800		
JEDEC DDR2 device bit width	X16		Bits
JEDEC DDR2 device count	1		Device(s)
JEDEC DDR2 Memory size	512	1024	MByte
CAS Latency	5	5	

(1) The DDR2 interface operates with a clock frequency of 312 MHz, higher DDR2 speed grades are supported due to inherent JEDEC DDR2 backwards compatibility.

Table 8. DLPC120-Q1 Compatible DDR2 Device Options

VENDOR	PART NUMBER	SIZE	ORGANIZATION	SPEED GRADE	C_L
ISSI	IS46DR16320C-25DBLA2	512 Mb	32Mx16	DDR2-800	5
Micron	MT47H64M16HR-25E AAT	1 Gb	32Mx16	DDR2-800	5
Micron	MT47H32M16HR-25E AAT	512 Mb	32Mx16	DDR2-800	5

8.3.4 JTAG and DMD Interface Test

The DLPC120-Q1 has two test interfaces using JTAG protocol:

- A standard JTAG (IEEE-1149) function of the ASIC is provided. The TI-provided BSDL file contains the details of the DLPC120-Q1 boundary scan chain. This JTAG interface is provided to enable system level validation of proper assembly of the DLPC120-Q1 onto a PCB.
- The DLPC120-Q1's DMD interface is designed to be the master for an in-system DMD interface test. The DMD interface should be connected directly to the DMD's JTAG pins. This interface is exclusively designed and verified to support the DLP3000-Q1 and DLP3030-Q1.

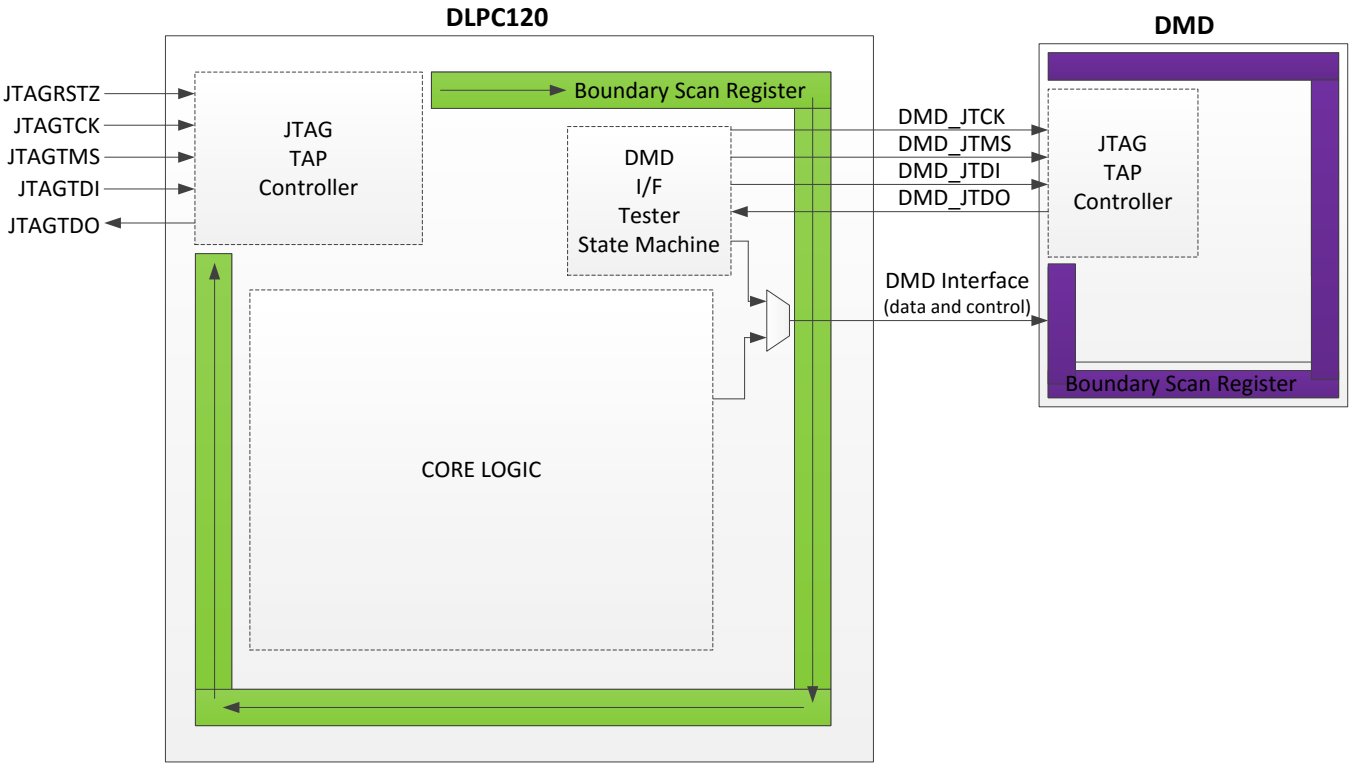


Figure 9. JTAG and DMD Interface Test

Using the DMD JTAG function, the DMD interface signals are toggled, and the connection at the DMD is verified by using the DMD JTAG signals to sample the inputs, and then toggled back to the DLPC120-Q1 for comparison to expected values. All DMD logic signals, except DAD OEZ, are tested individually for stuck high or low independently. Alternating data pattern for adjacent pins, as well as "walking 1's" and "walking 0's" patterns are used during the test. The DAD_OEZ is only tested in the high state as asserting this signal and toggling the inputs could cause damage to the DMD. Refer to Figure 10 for recommended connections for the DLPC120-Q1 boundary scan test configuration. Refer to Figure 11 for recommended connections of the DLPC120-Q1 to DMD interface test. For additional information about the DMD Boundary scan function refer to the *DLP3030-Q1 Data Sheet*.

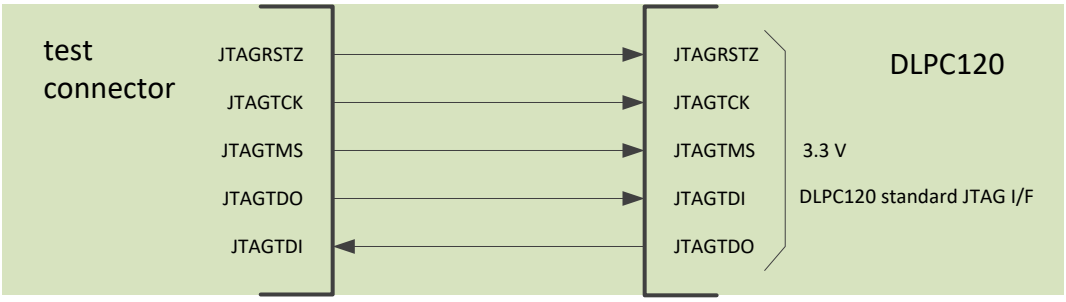


Figure 10. DLPC120-Q1 JTAG Boundary Scan Connection Example

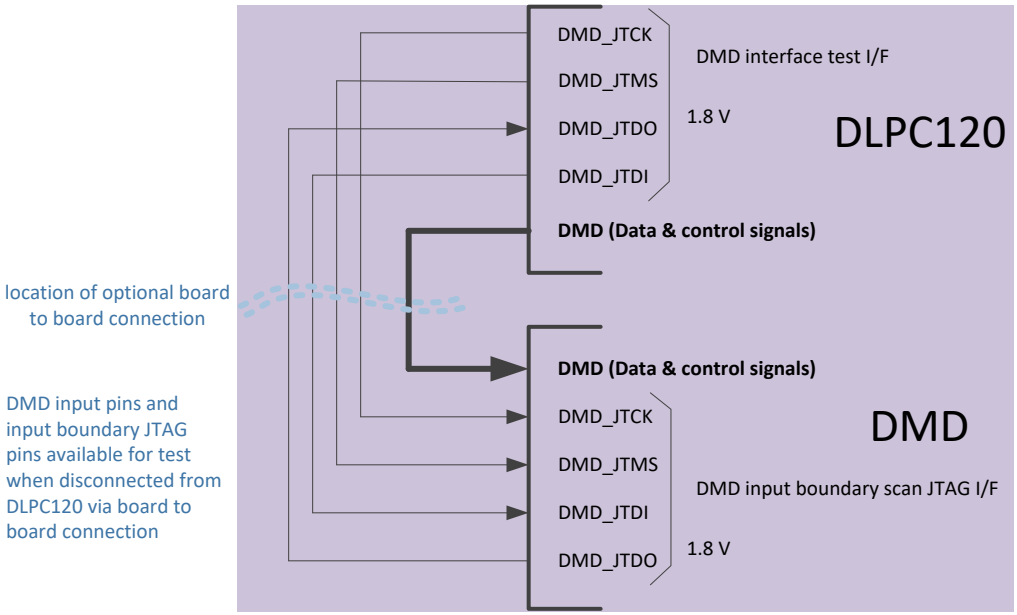


Figure 11. DLPC120-Q1 JTAG to DMD Interface Connection Example

8.3.5 Temperature Monitor Function

The DLPC120-Q1 connects with the TMP411 using a standard I^2C bus protocol using pins TMP_SDA and TMP_SCL. The internal temperature controller acts as a master to initialize the TMP411 to read the temperature of the DMD.

The TMP controller will issue a set of read commands at 8 times per second through the I^2C interface to read the Remote Temperature (DMD) and Local Temperature from the TMP411.

The TMP411 is used to monitor the DMD temperature and to control the DMD park operation when the DMD is operated beyond the required specification. See *DLP3030-Q1 Data Sheet* for the DMD operating temperature. If the DMD Park operation is used, then a 1 degree hysteresis is applied. See *DLPC120-Q1 Programmer's Guide* for description of this function.

8.3.6 DMD Heater PWM

Note that the package heater is not required for DLP3030-Q1 operation.

The DLPC120-Q1 provides a heater enable output PWM signal (HTR_ENABLE), which is designed to drive an external heater circuit for the DLP3000-Q1 DMD with a built-in resistive heater. The PWM signal output is enabled and disabled as required, based on readings from an external temperature sensor connected to the DMD temperature sense diode. See *DLPC120-Q1 Programmer's Guide* for description of this function.

8.3.7 Host Command Interface

The DLPC120-Q1 provides two I^2C interface port for host commands. Only one of these ports is intended to be used at a time. The unused port is meant for system debug or development purposes. The I^2C protocol and register definitions are defined in the *DLPC120-Q1 Programmer's Guide*.

8.4 Device Functional Modes

The DLPC120-Q1 has three operational display modes, which are selected with command list execution via the Host control interface. These display modes are External Video, Splash Screen, and Test Pattern.

8.4.1 External Video Mode

Upon the release of reset and initialization, the DLPC120-Q1 will automatically enter in External Video mode. This mode will process the video source on the parallel RGB input interface at a given resolution and frame rate. The system supports multiple input video resolutions, and the resolution expected by the DLPC120-Q1 can be configured via command list execution. See Table 3 for the different external video resolutions supported by the system.

8.4.2 Splash Screen Mode

This mode displays a custom, static image, which is stored in the DLPC120-Q1 Application Serial Flash memory. The content of the splash image is configurable. The Flash memory can store multiple Splash Screens, where the quantity is limited by the size of the splash images, size of the memory chip, and capacity of the remaining memory contents. Splash Screens are displayed via command list execution. Contact a TI Applications Engineer in order to change the splash images stored in the Flash memory.

8.4.3 Test Pattern Mode

This mode displays a fixed, static image, which is stored in the DLPC120-Q1 Application Serial Flash memory. The content of the test patterns are pre-defined, limited by the design of the DLPC120-Q1. Test Patterns are displayed via command list execution. See *DLPC120-Q1 Programmer's Guide* for a list and image of the supported Test Patterns.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DLPC120-Q1 is a DLP display processor that supports automotive head-up display (HUD) applications. It accepts data from a variety of video input resolutions and provides the digital image processing and control necessary to drive an LED based DLP display system. This document reflects the operation, pin-out and timing associated with the DLPC120-Q1 device only.

The DLPC120-Q1 is compatible with two DMD components:

- DLP3000-Q1 - 0.3 WVGA TYPE A100 DMD
- DLP3030-Q1 - 0.3 WVGA S-450 DMD

9.2 Typical Application

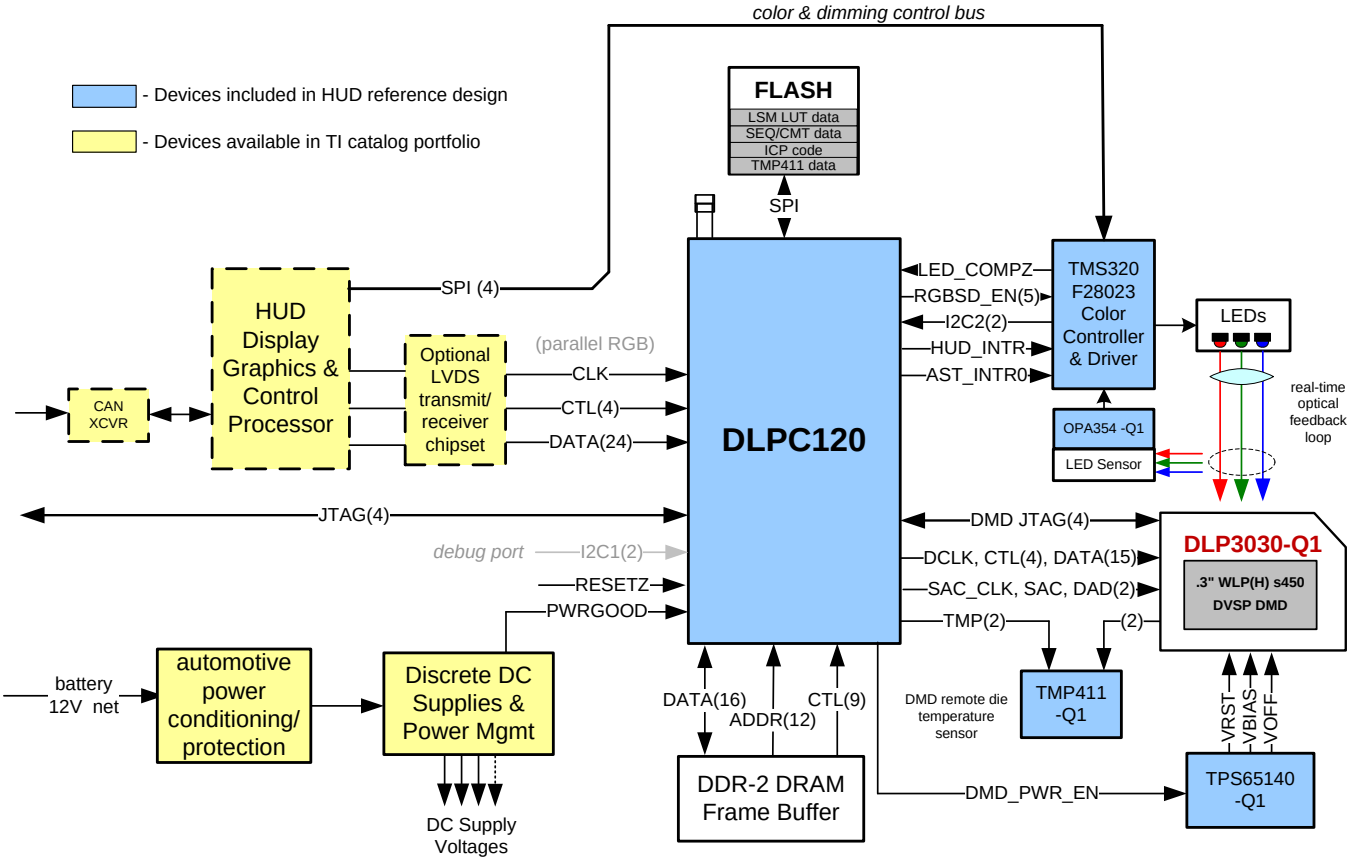


Figure 12. DLPC120-Q1 System Block Diagram

9.2.1 Design Requirements

A typical projector application is shown in Figure 12. For this application, the DLPC120-Q1 is controlled by a separate control processor, and the image data is received through the Parallel RGB interface.

Typical Application (continued)

As with prior DLP® electronics solutions, image data is 100% digital from the DLPC120-Q1 input port to the image projected on to the display screen. The image stays in digital form and is never converted into an analog signal. The DLPC120-Q1 processes the digital input image and converts the data into bit-plane format as needed by the DMD. The DMD then reflects light to the screen using binary Pulse-Width-Modulation (PWM) for each pixel mirror. The viewer's eyes integrate this light to form brilliant, crisp images.

The DLPC120-Q1 provides signals that enable Red, Green, and Blue LEDs to synchronize to the DMD PWM bit planes. These signals combined with an external MCU (TMS320F28023) can be used to create a very high dynamic dimming range necessary for automotive head-up display (HUD) applications.

The DLPC120-Q1 also features temperature monitoring of the DMD in order to automatically park the micro-mirrors when the DMD temperature is beyond the operating range.

The DLPC120-Q1 uses the DDR2 SDRAM as a frame buffer to convert RGB video data into the necessary bit plane format required by the DMD. The DLPC120-Q1 also supports multiple input resolutions and scales them to match the native .3" WVGA DMD format. These images can also be electronically bezel adjusted on the DMD, which could allow the displayed image to be electronically adjusted for mechanical misalignment. The DLPC120-Q1 is configured at power up with data stored in the Flash memory via SPI. The Flash interface is the primary method to configure the controller.

The DLPC120-Q1 supports system diagnostic and self-check features, such as video detection, DDR2 memory Built-in Self Test (BIST), System BIST, Flash BIST, and JTAG (in system and DMD interface).

Due to the mechanical nature of the micromirrors, the latency of the DLP3030-Q1 and DLPC120-Q1 chipset is fixed across all temperature and operating conditions. The observed video latency is one frame, or 16.67 ms at an input frame rate of 60 Hz. However, please note that the use of the DLPC120-Q1 bezel adjustment feature, if enabled, requires an additional frame of processing.

Contact a TI Applications Engineer in order to gain access to a fully functional reference design based on the DLP3030-Q1 chipset.

10 Power Supply Recommendations

10.1 Power Supply Filtering

The following filtering circuits are recommended for the various supply inputs.

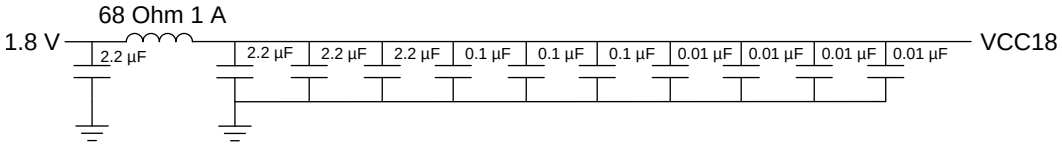


Figure 13. VCC18 Recommended Filter

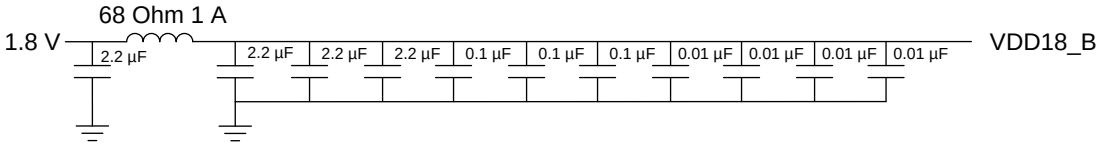


Figure 14. VDD18_B Recommended Filter

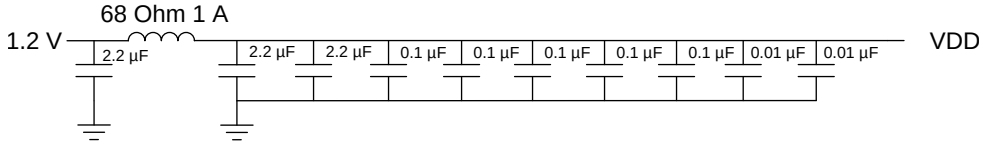


Figure 15. VDD Recommended Filter

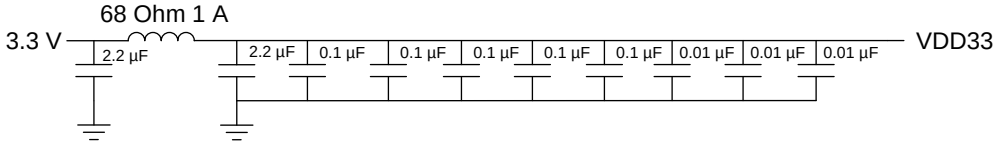


Figure 16. VDD33 Recommended Filter

11 Layout

11.1 Layout Guidelines

11.1.1 PCB layout guidelines for internal ASIC PLL power

The PLL's two analog supplies, VCCA and VSSA, shall be filtered with two series ferrite beads and two shunt 0.1-µF and 0.01-µF capacitors. The ferrite on VSSA is preferred but optional.

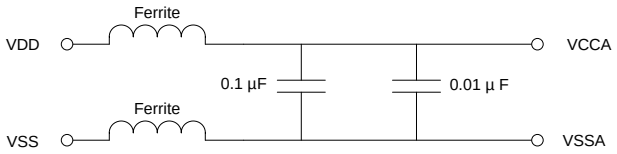


Figure 17. PLL Power Guidelines

Table 9. Recommended PLL Filter Components

COMPONENT	PARAMETER	RECOMMENDED VALUE	UNIT
Shunt Capacitor	Capacitance	0.1	µF
Shunt Capacitor	Capacitance	0.01	µF
Series Ferrite	Impedance at 10 MHz	>= 180	Ω
	Impedance at 100 MHz	>= 600	Ω
	DC Resistance	< 0.40	Ω

Example ferrite bead recommendations are listed in Table 10.

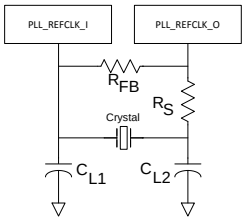
Table 10. PLL Power Ferrite Bead Recommendations

PART NUMBER	R @ DC	Z @ 10 MHz	Z @ 100 MHz	Z @1-GHz SIZE
BLM18EG601SN1	0.35	200	600	0603
BLM15AX601SN1	0.34	190	600	0402

The capacitors should be mounted as close to the package balls as possible.

11.1.2 DLPC120-Q1 Reference Clock

The DLPC120-Q1 requires an external reference clock to feed its internal PLL. A crystal or oscillator can supply this reference. The recommended crystal configurations and reference clock frequencies are listed in Table 11, with additional required discrete components shown in Figure 18 and defined in Table 11.



A. C_L = Crystal load capacitance

B. R_{FB} = Feedback Resistor

Figure 18. Discrete Components Required When Using Crystal

11.1.2.1 Recommended Crystal Oscillator Configuration

Table 11. Recommended Crystal Configuration

PARAMETER	RECOMMENDED	UNIT
Crystal circuit configuration	Parallel resonant	
Crystal type	Fundamental (first harmonic)	
Crystal nominal frequency	16	MHz
Crystal frequency tolerance (including accuracy, temperature, aging and trim sensitivity)	±200	PPM
Maximum crystal equivalent series resistance (ESR)	80	Ω
Temperature range	–40°C to +105°C	°C
R_{FB} feedback resistor (nominal)	1	MΩ
C_{L1} external crystal load capacitor	See equation in (1)	pF
C_{L2} external crystal load capacitor	See equation in (2)	pF
PCB layout	A ground isolation ring around the crystal is recommended	

(1) CL1 = 2 × (CL – Cstray_pll_refclk_i), where: Cstray_pll_refclk_i = Sum of package and PCB stray capacitance at the crystal pin associated with the ASIC pin PLL_REFCLK_I. PLL_REFCLK_I device capacitance is approximately 3 pF.

(2) CL2 = 2 × (CL – Cstray_pll_refclk_o), where: Cstray_pll_refclk_o = Sum of package and PCB stray capacitance at the crystal pin associated with the ASIC pin PLL_REFCLK_O. PLL_REFCLK_O device capacitance is approximately 3 pF.

11.1.3 General PCB Recommendations

TI provides PCB design files, which serve as a reference for a DLPC120-Q1 and DLP3030-Q1 chipset PCB schematic and layout design. Please contact a TI Applications Engineer to access these files.

11.1.4 PCB Routing Guidelines

All signals should follow a 0.005-in width 0.015-in spacing design rule. Minimum trace clearance from the ground ring around the PCB shall be 0.1-in minimum. Actual trace widths and clearances will be determined based on an analysis of impedance and stack-up requirements, some variation is expected.

Table 12. PCB Trace Matching Recommendations

GROUP	SIGNAL	CONSTRAINTS(1)
DDR2 I/F	MEM_CLK MEM_CLKZ MEM_DQS0 MEM_DQSZ0 MEM_DQS1 MEM_DQSZ1	Lengths Matched to 25 mils Max Total Length: 1500 mils Impedance: 100-Ω differential (± 10%)
	MEM_DQ[0:15]	Lengths Matched to 50 mils Max Total Length: 1500 mils Impedance: 50 Ω (± 10%)
	MEM_RASZ MEM_CASZ MEM_WEZ MEM_CSZ MEM_CKE MEM_A[0:12]	Lengths Matched to 100 mils Max Total Length: 1500 mils Impedance: 50 Ω (± 10%)
DMD I/F	DMD_D[0:14] DMD_DCLK DMD_BUS DMD_STRB DMD_OEZ DMD_LOADB DMD_SAC_CLK DMD_SAC_BUS DMD_SCTRL DMD_TRC DMD_JTCK DMD_JTDI DMD_JTDO DMD_JTMS	Lengths Matched to 50 mils Max Total Length: 10000 mils Impedance: 50 Ω (± 10%)
Serial Flash I/F	FLASH_DCLK, FLASH_MISO, FLASH_MOSI, FLASH_CSZ	Lengths Matched to 100 mils Max Total Length: 2500 mils Impedance: 50 Ω (± 10%)

(1) Trace lengths on Layers 1 and 10 should be less than 50 mils.

11.1.5 Number of Layer Changes

- As a reference, the TI design uses no more than three layer changes per trace.
- Individual differentially matched signal pairs can be routed on different layers, but the signals of a given pair should not change.

11.1.6 Terminations

- All DMD I/F signals should be terminated at the source with a 20-Ω series resistor.
- MEM_CLK and MEM_CLKZ should be terminated with an external 100-Ω differential resistor across the two signals as close to the DRAM as possible. All other DDR2 control and data signals should be pulled to VTT(0.9 V) with a 56-Ω resistor as close to the DRAM as possible.

11.1.7 General Handling Guidelines for Unused CMOS-Type Pins

To avoid potentially damaging current caused by floating CMOS input-only pins, it is recommended that unused ASIC input pins be tied through a pull-up resistor to its associated power supply or a pull-down to ground. For ASIC inputs with an internal pull-up or pull-down resistors, it is unnecessary to add an external pullup or pulldown unless specifically recommended. Note that internal pull-up and pull-down resistors are weak and should not be expected to drive the external line. The DLPC120-Q1 implements very few internal resistors and these are noted in the pin list.

Unused output-only pins can be left open. When possible, it is recommended that unused Bi-directional I/O pins be configured to their output state such that the pin can be left open. If this control is not available and the pins may become an input, then they should be pulled-up (or down) using an appropriate resistor.

12 器件和文档支持

12.1 器件支持

12.1.1 器件命名规则

12.1.1.1 器件标记

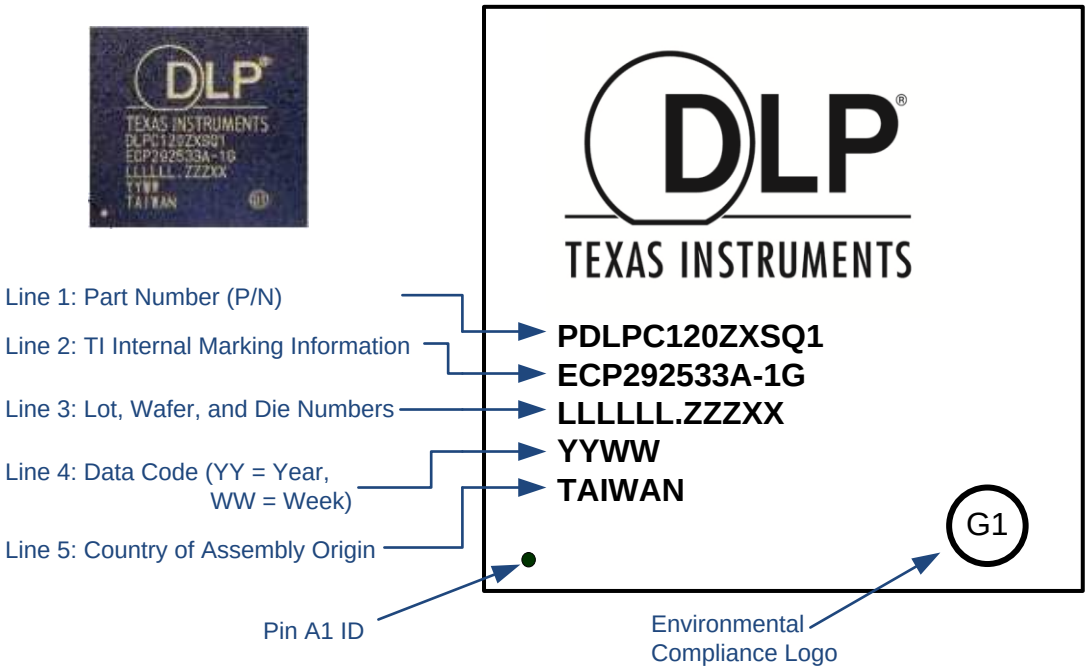


图 **19.** 器件标记

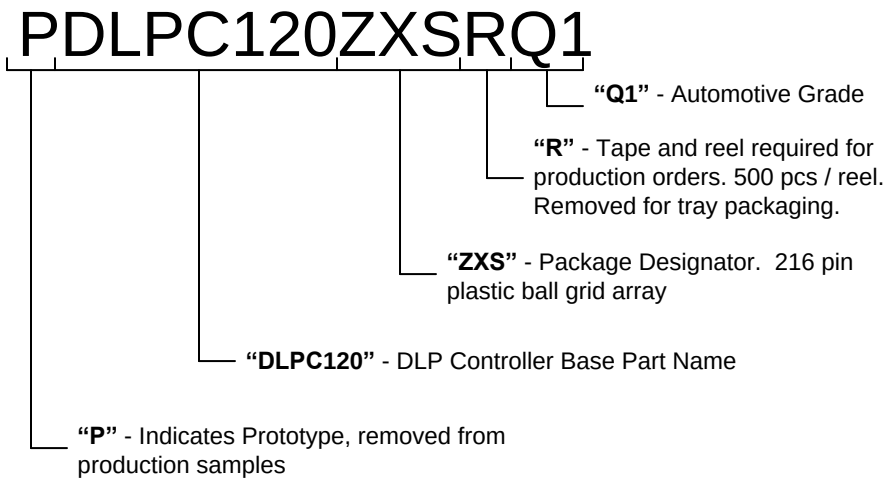


图 **20.** 器件型号定义

12.2 文档支持

12.2.1 相关文档

请参阅如下相关文档：

- DLP3030-Q1 产品文件夹，以获取 *DLP3030-Q1 数据表*

12.3 接收文档更新通知

如需接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

12.5 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如欲获取此数据表的浏览器版本，请参阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLPC120ZXSQ1	ACTIVE	NFBGA	ZXS	216	10	TBD	Call TI	Call TI	-40 to 105		Samples
DLPC120ZXSRQ1	ACTIVE	NFBGA	ZXS	216	500	TBD	Call TI	Call TI	-40 to 105		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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