

# SN74AVC4T774 具有可配置电压电平转换和三态输出以及独立方向控制输入的 4 位双电源总线收发器

## 1 特性

- 每个通道都具有独立的 DIR 控制输入
- 控制输入  $V_{IH}/V_{IL}$  电平以  $V_{CCA}$  电压为基准
- 完全可配置的双轨设计，支持各个端口在 1.1V 至 3.6V 的整个电源电压范围内运行
- I/O 可耐受 4.6V 电压
- $I_{off}$  支持局部省电模式运行
- 典型数据速率
  - 380Mbps ( 1.8V 至 3.3V 转换 )
  - 200Mbps ( <1.8V 至 3.3V 转换 )
  - 200Mbps ( 转换至 2.5V 或 1.8V )
  - 150Mbps ( 转换至 1.5V )
  - 100Mbps ( 转换至 1.2V )
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范
- ESD 保护超过以下等级 ( 测试符合 JESD 22 标准 )
  - $\pm 8000V$  人体放电模型 (A114-A)
  - 250V 机器放电模型 (A115-A)
  - $\pm 1500V$  充电器件模型 (C101)

## 2 应用

- 个人电子产品
- 工业
- 企业
- 电信

## 3 说明

这款 4 位同相总线收发器使用两个独立的可配置电源轨。A 端口旨在跟踪  $V_{CCA}$ ， $V_{CCA}$  电源电压为 1.1V 至 3.6V。B 端口旨在用于跟踪  $V_{CCB}$ ， $V_{CCB}$  电源电压为 1.1V 至 3.6V。SN74AVC4T774 经过优化，可在  $V_{CCA}/V_{CCB}$  设置为 1.4V 至 3.6V 范围内时正常运行。该器件可在  $V_{CCA}/V_{CCB}$  低至 1.2V 的情况下正常运行，因此，可在 1.2V、1.5V、1.8V、2.5V 和 3.3V 电压节点之间进行通用的低电压双向转换。

SN74AVC4T774 旨在实现数据总线间的异步通信。方向控制 (DIR) 输入和输出使能 ( $\overline{OE}$ ) 输入的逻辑电平会

激活 B 端口输出或 A 端口输出，或将两个输出端口置于高阻抗模式。当 B 输出被激活时，此器件将数据从 A 总线发送到 B 总线，而当 A 输出被激活时，此器件将数据从 B 总线发送到 A 总线。A 端口和 B 端口上的输入电路一直处于激活状态并且必须施加一个逻辑高或低电平，从而防止过大的  $I_{CC}$  和  $I_{CCZ}$ 。

SN74AVC4T774 的设计方式决定了控制引脚 ( DIR1、DIR2、DIR3、DIR4 和  $\overline{OE}$  ) 由  $V_{CCA}$  供电。该器件专用于使用  $I_{off}$  的局部省电应用。 $I_{off}$  电路可禁用输出，以防在器件省电模式时电流回流对器件造成损坏。 $V_{CC}$  隔离特性可确保当任一  $V_{CC}$  输入接地时，两个端口都处于高阻抗状态。

为了确保加电或断电期间的高阻抗状态，应通过一个上拉电阻器将  $\overline{OE}$  连接至  $V_{CCA}$ ；该电阻器的最小值由驱动器的电流灌入能力决定。由于此器件具有 CMOS 输入，因此请勿将其悬空。如果输入未驱动至高  $V_{CC}$  状态或低 GND 状态，则可能会导致比预期更大的  $I_{CC}$  电流。由于输入电压稳定取决于许多因素 ( 例如，电容、电路板布局布线、封装电感、周围条件等 )，因此，确保这些输入不处于错误的开关状态并将其连接到高电平或低电平，可更大限度地减少漏电流。

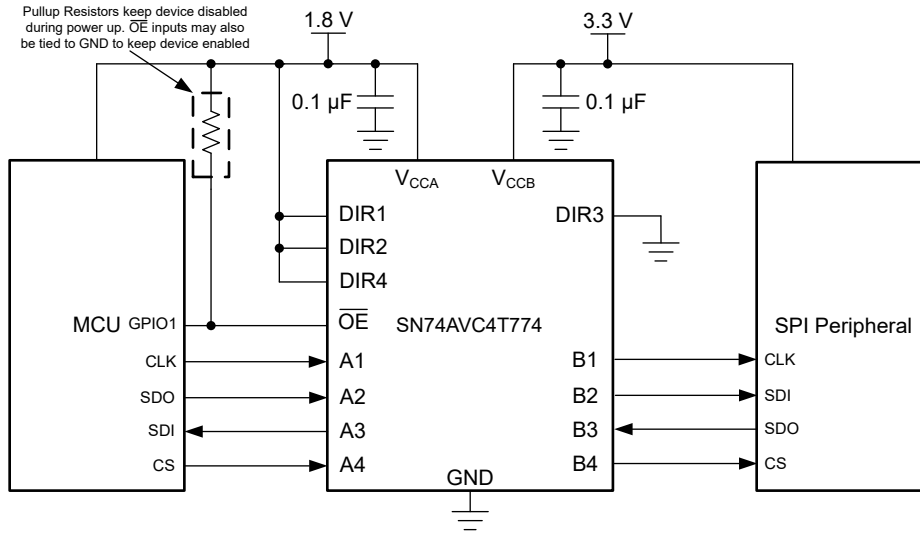
### 封装信息

器件型号	封装 <sup>(1)</sup>	封装尺寸 <sup>(2)</sup>
SN74AVC4T774	TSSOP ( PW , 16 )	5mm × 4.40mm
	VQFN ( RGY , 16 )	4mm × 3.5mm
	UQFN ( RSV , 16 )	2.6mm × 1.8mm
	BQB ( WQFN , 16 )	3.5mm × 2.5mm
	DYY ( SOT , 16 )	4.2mm × 2mm

(1) 有关更多信息，请参阅节 11。

(2) 封装尺寸 ( 长 × 宽 ) 为标称值，并包括引脚 ( 如适用 )。



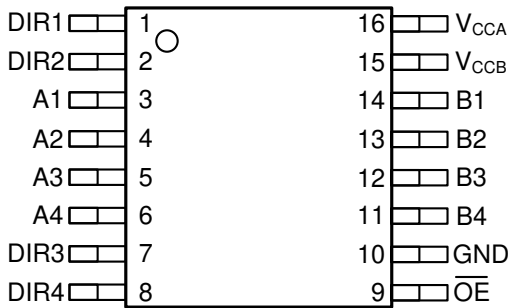


典型应用原理图

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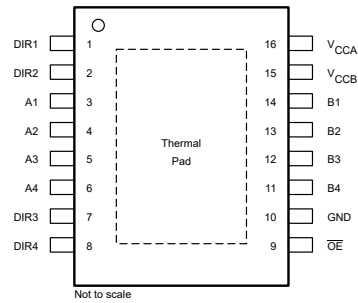
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### 4 Pin Configuration and Functions

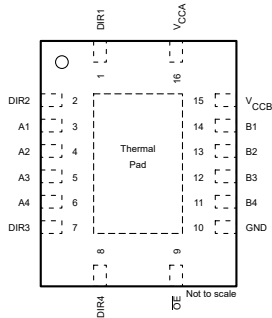


A. Shown for a single channel

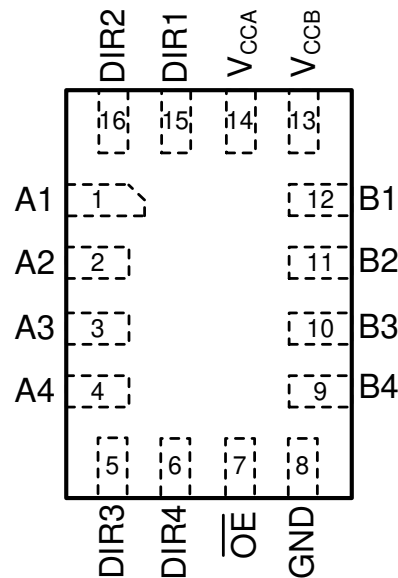
**图 4-1. PW Package, 16-Pin TSSOP (Top View)**



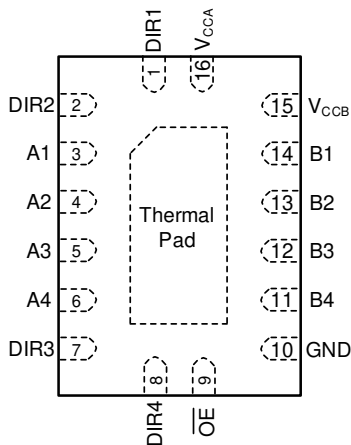
**图 4-2. DYY Package, 16-Pin SOT (Top View)**



**图 4-3. RGY Package, 16-Pin VQFN (Top View)**



**图 4-4. RSV Package, 16-Pin UQFN (Top View)**



**图 4-5. BQB Package, 16-Pin WQFN, Transparent (Top View)**

**表 4-1. Pin Functions**

NAME	PIN		TYPE	DESCRIPTION
	PW RGY BQB DYY	RSV		
DIR1	1	15	I	Direction-control input referenced to $V_{CCA}$ , controls signal flow for the first (A1/B1) I/O channels.
DIR2	2	16	I	Direction-control input referenced to $V_{CCA}$ , controls signal flow for the second (A2/B2) I/O channels.
A1	3	1	I/O	Input/output A1. Referenced to $V_{CCA}$ .
A2	4	2	I/O	Input/output A2. Referenced to $V_{CCA}$ .
A3	5	3	I/O	Input/output A3. Referenced to $V_{CCA}$ .
A4	6	4	I/O	Input/output A4. Referenced to $V_{CCA}$ .
DIR3	7	5	I	Direction-control input referenced to $V_{CCA}$ , controls signal flow for the third (A3/B3) I/O channels.
DIR4	8	6	I	Direction-control input referenced to $V_{CCA}$ , controls signal flow for the fourth (A4/B4) I/O channels.
$\overline{OE}$	9	7	I	3-state output-mode enables. Pull $\overline{OE}$ high to place all outputs in 3-state mode. Referenced to $V_{CCA}$ .
GND	10	8	—	Ground.
B4	11	9	I/O	Input/output B4. Referenced to $V_{CCB}$ .
B3	12	10	I/O	Input/output B3. Referenced to $V_{CCB}$ .
B2	13	11	I/O	Input/output B2. Referenced to $V_{CCB}$ .
B1	14	12	I/O	Input/output B1. Referenced to $V_{CCB}$ .
$V_{CCB}$	15	13	—	B-port supply voltage. $1.1V \leq V_{CCB} \leq 3.6V$ .
$V_{CCA}$	16	14	—	A-port supply voltage. $1.1V \leq V_{CCA} \leq 3.6V$ .

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
VCCA VCCB	Supply voltage		- 0.5	4.6	V
VI	Input voltage range <sup>(2)</sup>	I/O ports (A port)	- 0.5	4.6	V
		I/O ports (B port)	- 0.5	4.6	
		Control inputs	- 0.5	4.6	
VO	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	A port	- 0.5	4.6	V
		B port	- 0.5	4.6	
VO	Voltage range applied to any output in the high or low state <sup>(2)</sup> <sup>(3)</sup>	A port	- 0.5	VCCA + 0.5	V
		B port	- 0.5	VCCB + 0.5	
I <sub>IK</sub>	Input clamp current	VI < 0		- 50	mA
I <sub>OK</sub>	Output clamp current	VO < 0		- 50	mA
IO	Continuous output current			±50	mA
	Continuous current through VCCA, VCCB, or GND			±100	
T <sub>J</sub>	Junction temperature			150	°C
T <sub>stg</sub>	Storage temperature		- 65	150	°C

(1) Stresses beyond those listed under [Absolute Maximum Ratings](#) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.

### 5.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±8000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	
		Machine model (A115-A)	250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup> <sup>(2)</sup> <sup>(3)</sup>

			V <sub>CCI</sub>	V <sub>CCO</sub>	MIN	MAX	UNIT
V <sub>CCA</sub>	Supply voltage				1.1	3.6	V
V <sub>CCB</sub>	Supply voltage				1.1	3.6	V
V <sub>IH</sub>	High-level input voltage	Data inputs <sup>(4)</sup>	1.1 V to 1.95 V		V <sub>CCI</sub> × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V <sub>IL</sub>	Low-level input voltage	Data inputs <sup>(4)</sup>	1.1 V to 1.95 V		V <sub>CCI</sub> × 0.35		V
			1.95 V to 2.7 V		0.7		
			2.7 V to 3.6 V		0.8		

### 5.3 Recommended Operating Conditions (续)

over operating free-air temperature range (unless otherwise noted)<sup>(1) (2) (3)</sup>

			V <sub>CCI</sub>	V <sub>CCO</sub>	MIN	MAX	UNIT
V <sub>IH</sub>	High-level input voltage	Control Inputs (referenced to V <sub>CCA</sub> ) <sup>(5)</sup> (DIRx, $\overline{OE}$ )	1.1 V to 1.95 V		V <sub>CCA</sub> × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V <sub>IL</sub>	Low-level input voltage	Control Inputs (referenced to V <sub>CCA</sub> ) <sup>(5)</sup> (DIRx, $\overline{OE}$ )	1.1 V to 1.95 V		V <sub>CCA</sub> × 0.35		V
			1.95 V to 2.7 V		0.7		
			2.7 V to 3.6 V		0.8		
V <sub>I</sub>	Input voltage				0	3.6	V
V <sub>O</sub>	Output voltage	Active state			0	V <sub>CCO</sub>	V
		3-state			0	3.6	
I <sub>OH</sub>	High-level output current			1.1 V to 1.3 V		-3	mA
				1.4 V to 1.6 V		-6	
				1.65 V to 1.95 V		-8	
				2.3 V to 2.7 V		-9	
				3 V to 3.6 V		-12	
I <sub>OL</sub>	Low-level output current			1.1 V to 1.3 V		3	mA
				1.4 V to 1.6 V		6	
				1.65 V to 1.95 V		8	
				2.3 V to 2.7 V		9	
				3 V to 3.6 V		12	
$\Delta t / \Delta v$	Input transition rise or fall rate					5	ns/V
T <sub>A</sub>	Operating free-air temperature				-40	85	°C

- (1) V<sub>CCI</sub> is the V<sub>CC</sub> associated with the input port.
- (2) V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.
- (3) All unused data inputs of the device must be held at V<sub>CCI</sub> or GND to ensure proper device operation. Refer to the TI application report, [Implications of Slow or Floating CMOS Inputs](#).
- (4) For V<sub>CCI</sub> values not specified in the data sheet, V<sub>IH</sub> min = V<sub>CCI</sub> × 0.7 V, V<sub>IL</sub> max = V<sub>CCI</sub> × 0.3 V
- (5) For V<sub>CCI</sub> values not specified in the data sheet, V<sub>IH</sub> min = V<sub>CCA</sub> × 0.7 V, V<sub>IL</sub> max = V<sub>CCA</sub> × 0.3 V

### 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74AVC4T774					UNIT
		RGY (VQFN)	RSV (UQFN)	DYY (SOT)	BQB (WQFN)	PW (TSSOP)	
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	37.7	139.2	163.4	79.1	123.8	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	56.1	64.9	90.0	77.5	58.3	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	15.9	67.7	93.1	49.0	81.7	°C/W
Y <sub>JT</sub>	Junction-to-top characterization parameter	0.5	1.7	10.9	7.3	6.7	°C/W
Y <sub>JB</sub>	Junction-to-board characterization parameter	16.1	67.4	92.1	48.9	80.9	°C/W
R <sub>θJC(bottom)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	26.4	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)<sup>(1) (2) (3)</sup>

PARAMETER	TEST CONDITIONS	$V_{CCA}$	$V_{CCB}$	TA = 25°C			- 40°C to 85°C			UN IT
				MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OH}$		$I_{OH} = -100 \mu A$	$V_I = V_{IH}$	1.1 V to 3.6 V	1.1 V to 3.6 V		$V_{CCO} - 0.2$			V
				1.2 V	1.2 V	0.95				
				1.4 V	1.4 V		1.05			
				1.65 V	1.65 V		1.2			
				2.3 V	2.3 V		1.75			
				3 V	3 V		2.3			
$V_{OL}$		$I_{OL} = 100 \mu A$	$V_I = V_{IL}$	1.1 V to 3.6 V	1.1 V to 3.6 V				0.2	V
				1.2 V	1.2 V	0.25				
				1.4 V	1.4 V		0.35			
				1.65 V	1.65 V		0.45			
				2.3 V	2.3 V		0.55			
				3 V	3 V		0.7			
$I_I$	Control inputs	$V_I = V_{CCA}$ or GND		1.1 V to 3.6 V	1.1 V to 3.6 V	$\pm 0.025$	$\pm 0.25$		$\pm 1$	$\mu A$
$I_{off}$	A or B port	$V_I$ or $V_O = 0$ to 3.6 V		0 V	0 V to 3.6 V	$\pm 0.1$	$\pm 1$		$\pm 5$	$\mu A$
				0 V to 3.6 V	0 V	$\pm 0.1$	$\pm 1$		$\pm 5$	
$I_{OZ}$	A or B port	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND, $\overline{OE} = V_{IH}$		3.6 V	3.6 V	$\pm 0.5$	$\pm 2.5$		$\pm 5$	$\mu A$
$I_{CCA}$		$V_I = V_{CCI}$ or GND, $I_O = 0$		1.1 V to 3.6 V	1.1 V to 3.6 V				8	$\mu A$
				0 V	0 V to 3.6 V			- 2		
				0 V to 3.6 V	0 V				8	
$I_{CCB}$		$V_I = V_{CCI}$ or GND, $I_O = 0$		1.1 V to 3.6 V	1.1 V to 3.6 V				8	$\mu A$
				0 V	0 V to 3.6 V				8	
				0 V to 3.6 V	0 V			- 2		
$I_{CCA} + I_{CCB}$		$V_I = V_{CCI}$ or GND, $I_O = 0$		1.1 V to 3.6 V	1.1 V to 3.6 V				16	$\mu A$
$C_i$	Control inputs	$V_I = 3.3$ V or GND		3.3 V	3.3 V		2.5		4.5	pF
$C_{io}$	A or B port	$V_O = 3.3$ V or GND		3.3 V	3.3 V		5		7	pF

(1)  $V_{CCI}$  is the  $V_{CC}$  associated with the input port.

(2)  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.

(3) All unused data inputs of the device must be held at  $V_{CCI}$  or GND to ensure proper device operation. Refer to the TI application report, [Implications of Slow or Floating CMOS Inputs](#).



### 5.6 Switching Characteristics: VCCA = 1.2 V ± 0.1 V

See Figure 8-1 and Table 8-1 for test circuit and loading. See Figure 8-2, Figure 8-3, and Figure 8-4 for measurement waveforms.

PARAMETER	PARAMETER	FROM	TO	Test Conditions	V <sub>CCB</sub> = 1.2 V ± 0.1 V		V <sub>CCB</sub> = 1.5 V ± 0.1 V		V <sub>CCB</sub> = 1.8 V ± 0.15 V		V <sub>CCB</sub> = 2.5 V ± 0.2 V		V <sub>CCB</sub> = 3.3 V ± 0.3 V		UNIT
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	t <sub>PLH</sub>	A	B	-40°C to 85°C	2	7.5	1.5	5.5	1	4.5	1	4	0.5	4	ns
t <sub>PHL</sub>	t <sub>PHL</sub>				1.5	5.5	1	4	1	4	0.5	4.5	0.5	6	
t <sub>PLH</sub>	t <sub>PLH</sub>	B	A		2	7	1.5	6.5	1	6	1	6	1	6	
t <sub>PHL</sub>	t <sub>PHL</sub>				1.5	5.5	1	5	1	4.5	0.5	4	0.5	4	
t <sub>PZH</sub>	t <sub>PZH</sub>	OE	A		2.5	8	2	8	1	8	1	8	1	8.5	
t <sub>PZL</sub>	t <sub>PZL</sub>				2.5	9	2	9	1.5	9	1	9	1	9	
t <sub>PZH</sub>	t <sub>PZH</sub>	OE	B		2	7.5	1.5	5.5	1	6.5	1	9.5	0.5	30	
t <sub>PZL</sub>	t <sub>PZL</sub>				2.5	8.5	1.5	6.5	1	7	1	8.5	0.5	24	
t <sub>PHZ</sub>	t <sub>PHZ</sub>	OE	A		3	6.5	2	6.5	2	6.5	1.5	6.5	2	6.5	
t <sub>PLZ</sub>	t <sub>PLZ</sub>				3	6.5	2.5	6.5	2.5	6.5	2	6.5	2	6.5	
t <sub>PHZ</sub>	t <sub>PHZ</sub>	OE	B		3	6	2.5	5.5	2	6	1.5	5	2	6.5	
t <sub>PLZ</sub>	t <sub>PLZ</sub>				3	6	2.5	5.5	2.5	5.5	1.5	5	2	6	

### 5.7 Switching Characteristics: VCCA = 1.5 V ± 0.1 V

See Figure 8-1 and Table 8-1 for test circuit and loading. See Figure 8-2, Figure 8-3, and Figure 8-4 for measurement waveforms.

PARAMETER	PARAMETER	FROM	TO	V <sub>CCB</sub> = 1.2 V ± 0.1 V		V <sub>CCB</sub> = 1.5 V ± 0.1 V		V <sub>CCB</sub> = 1.8 V ± 0.15 V		V <sub>CCB</sub> = 2.5 V ± 0.2 V		V <sub>CCB</sub> = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	t <sub>PLH</sub>	A	B	1.5	6.5	0.3	6.3	0.3	5.2	0.4	4.2	0.4	4.2	ns
t <sub>PHL</sub>	t <sub>PHL</sub>			1.5	4.5	0.3	6.3	0.3	5.2	0.4	4.2	0.4	4.2	
t <sub>PLH</sub>	t <sub>PLH</sub>	B	A	1.5	5	0.7	6.3	0.5	6	0.4	5.7	0.3	5.6	ns
t <sub>PHL</sub>	t <sub>PHL</sub>			1.5	4	0.7	6.3	0.5	6	0.4	5.7	0.3	5.6	
t <sub>PZH</sub>	t <sub>PZH</sub>	OE	A	1.5	5	1.4	9.6	1.1	9.5	0.7	9.4	0.4	9.4	ns
t <sub>PZL</sub>	t <sub>PZL</sub>			2	5.5	1.4	9.6	1.1	9.5	0.7	9.4	0.4	9.4	
t <sub>PZH</sub>	t <sub>PZH</sub>	OE	B	2	6.5	1.4	9.6	1.1	7.7	0.9	5.8	0.9	5.6	ns
t <sub>PZL</sub>	t <sub>PZL</sub>			2	7.5	1.4	9.6	1.1	7.7	0.9	5.8	0.9	5.6	
t <sub>PHZ</sub>	t <sub>PHZ</sub>	OE	A	2	5	1.8	10.2	1.5	10.2	1.3	10.2	1.6	10.2	ns
t <sub>PLZ</sub>	t <sub>PLZ</sub>			2.5	4.5	1.8	10.2	1.5	10.2	1.3	10.2	1.6	10.2	
t <sub>PHZ</sub>	t <sub>PHZ</sub>	OE	B	3	5.5	1.9	10.3	1.9	9.1	1.4	7.4	1.2	7.6	ns
t <sub>PLZ</sub>	t <sub>PLZ</sub>			3	5.5	1.9	10.3	1.9	9.1	1.4	7.4	1.2	7.6	

### 5.8 Switching Characteristics: $V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V}$

See Figure 8-1 and Table 8-1 for test circuit and loading. See Figure 8-2, Figure 8-3, and Figure 8-4 for measurement waveforms.

PARAMETER	PARAMETER	FROM	TO	Test Conditions	$V_{CCB} = 1.2\text{ V} \pm 0.1\text{ V}$		$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$		$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	$t_{PLH}$	A	B	-40°C to 85°C	1.5	6.5	0.3	6.3	0.3	5.2	0.4	4.2	0.4	4.2	ns
$t_{PHL}$	$t_{PHL}$				1	4.5	0.3	6.3	0.3	5.2	0.4	4.2	0.4	4.2	
$t_{PLH}$	$t_{PLH}$	B	A		1.5	6	0.7	6.3	0.5	6	0.4	5.7	0.3	5.6	
$t_{PHL}$	$t_{PHL}$				1	4.5	0.7	6.3	0.5	6	0.4	5.7	0.3	5.6	
$t_{PZH}$	$t_{PZH}$	$\overline{OE}$	A		1	6.5	1.4	9.6	1.1	9.5	0.7	9.4	0.4	9.4	
$t_{PZL}$	$t_{PZL}$				1.5	7.5	1.4	9.6	1.1	9.5	0.7	9.4	0.4	9.4	
$t_{PZH}$	$t_{PZH}$	$\overline{OE}$	B		2	6	1.4	9.6	1.1	7.7	0.9	5.8	0.9	5.6	
$t_{PZL}$	$t_{PZL}$				2	7	1.4	9.6	1.1	7.7	0.9	5.8	0.9	5.6	
$t_{PHZ}$	$t_{PHZ}$	$\overline{OE}$	A		2	6	1.8	10.2	1.5	10.2	1.3	10.2	1.6	10.2	
$t_{PLZ}$	$t_{PLZ}$				2.5	5.5	1.8	10.2	1.5	10.2	1.3	10.2	1.6	10.2	
$t_{PHZ}$	$t_{PHZ}$	$\overline{OE}$	B		2.5	5	1.9	10.3	1.9	9.1	1.4	7.4	1.2	7.6	
$t_{PLZ}$	$t_{PLZ}$				2.5	5	1.9	10.3	1.9	9.1	1.4	7.4	1.2	7.6	

### 5.9 Switching Characteristics: $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$

See Figure 8-1 and Table 8-1 for test circuit and loading. See Figure 8-2, Figure 8-3, and Figure 8-4 for measurement waveforms.

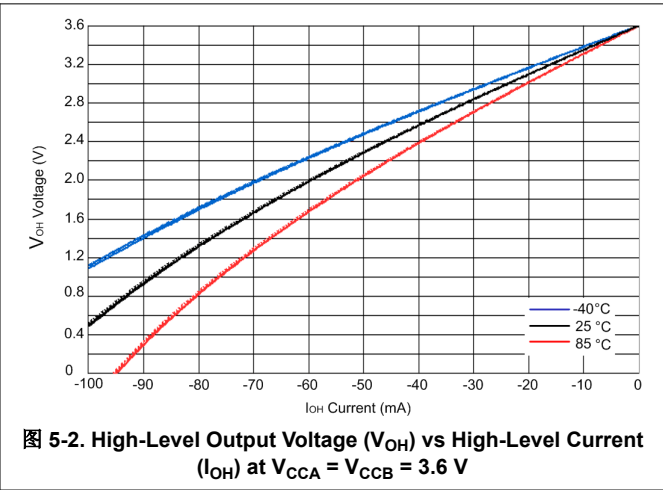
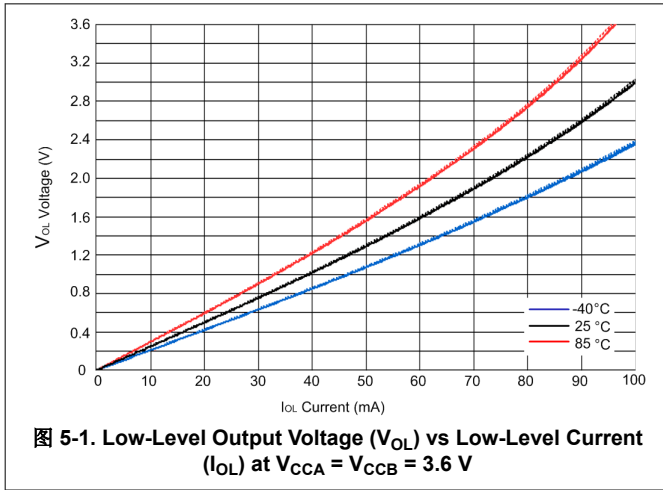
PARAMETER	PARAMETER	FROM	TO	$V_{CCB} = 1.2\text{ V} \pm 0.1\text{ V}$		$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$		$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	$t_{PLH}$	A	B	1.5	6.5	0.1	5.7	0.1	4.6	0.2	3.5	0.1	3.6	ns
$t_{PHL}$	$t_{PHL}$			1	4.5	0.1	5.7	0.1	4.6	0.2	3.5	0.1	3.6	
$t_{PLH}$	$t_{PLH}$	B	A	1.5	4	0.6	4.2	0.4	3.9	0.2	3.4	0.2	3.3	ns
$t_{PHL}$	$t_{PHL}$			1	5	0.6	4.2	0.4	3.9	0.2	3.4	0.2	3.3	
$t_{PZH}$	$t_{PZH}$	$\overline{OE}$	A	1	2.5	0.7	6.5	0.7	5.2	0.6	4.8	0.4	4.8	ns
$t_{PZL}$	$t_{PZL}$			1	3	0.7	6.5	0.7	5.2	0.6	4.8	0.4	4.8	
$t_{PZH}$	$t_{PZH}$	$\overline{OE}$	B	1.5	6	0.9	8.8	0.8	7	0.6	4.8	0.6	4	ns
$t_{PZL}$	$t_{PZL}$			2	7	0.9	8.8	0.8	7	0.6	4.8	0.6	4	
$t_{PHZ}$	$t_{PHZ}$	$\overline{OE}$	A	1.5	3.5	1	8.4	1	8.4	1	6.2	1	6.6	ns
$t_{PLZ}$	$t_{PLZ}$			2	3.5	1	8.4	1	8.4	1	6.2	1	6.6	
$t_{PHZ}$	$t_{PHZ}$	$\overline{OE}$	B	2	5	1.5	9.4	1.3	8.2	1.1	6.2	0.9	5.2	ns
$t_{PLZ}$	$t_{PLZ}$			2.5	5	1.5	9.4	1.3	8.2	1.1	6.2	0.9	5.2	

### 5.10 Switching Characteristics: $V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$

See [Figure 8-1](#) and [Table 8-1](#) for test circuit and loading. See [Figure 8-2](#), [Figure 8-3](#), and [Figure 8-4](#) for measurement waveforms.

PARAMETER	PARAMETER	FROM	TO	$V_{CCB} = 1.2\text{ V} \pm 0.1\text{ V}$		$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$		$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	$t_{PLH}$	A	B	1.5	6	0.1	5.6	0.1	4.5	0.1	3.3	0.1	2.9	ns
$t_{PHL}$	$t_{PHL}$			1	4	0.1	5.6	0.1	4.5	0.1	3.3	0.1	2.9	
$t_{PLH}$	$t_{PLH}$	B	A	1.5	4	0.6	4.2	0.4	3.4	0.2	3	0.1	2.8	ns
$t_{PHL}$	$t_{PHL}$			1.5	7.5	0.6	4.2	0.4	3.4	0.2	3	0.1	2.8	
$t_{PZH}$	$t_{PZH}$	$\overline{OE}$	A	1	2.5	0.6	8.7	0.6	5.2	0.6	3.8	0.4	3.8	ns
$t_{PZL}$	$t_{PZL}$			1	2.5	0.6	8.7	0.6	5.2	0.6	3.8	0.4	3.8	
$t_{PZH}$	$t_{PZH}$	$\overline{OE}$	B	1.5	6	0.8	8.7	0.6	6.8	0.5	4.7	0.5	3.8	ns
$t_{PZL}$	$t_{PZL}$			1.5	7	0.8	8.7	0.6	6.8	0.5	4.7	0.5	3.8	
$t_{PHZ}$	$t_{PHZ}$	$\overline{OE}$	A	2	4	0.7	9.3	0.7	8.3	0.7	5.6	0.7	6.6	ns
$t_{PLZ}$	$t_{PLZ}$			2	4	0.7	9.3	0.7	8.3	0.7	5.6	0.7	6.6	
$t_{PHZ}$	$t_{PHZ}$	$\overline{OE}$	B	2	5	1.4	9.3	1.2	8.1	1	6.4	0.8	6.2	ns
$t_{PLZ}$	$t_{PLZ}$			2	4.5	1.4	9.3	1.2	8.1	1	6.4	0.8	6.2	

### 5.11 Typical Characteristics

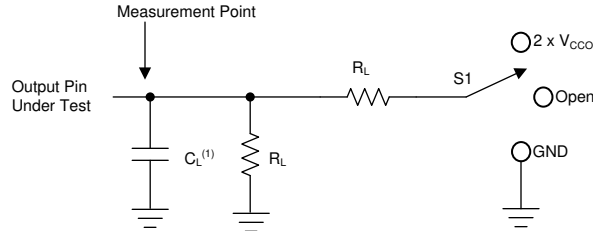


## 6 Parameter Measurement Information

### 6.1 Load Circuit and Voltage Waveforms

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- $f = 10 \text{ MHz}$
- $Z_O = 50 \ \Omega$
- $\Delta t / \Delta V \leq 1 \text{ ns/V}$



A.  $C_L$  includes probe and jig capacitance.

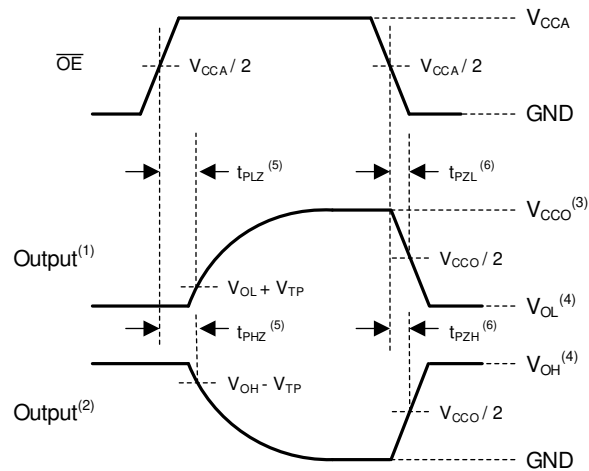
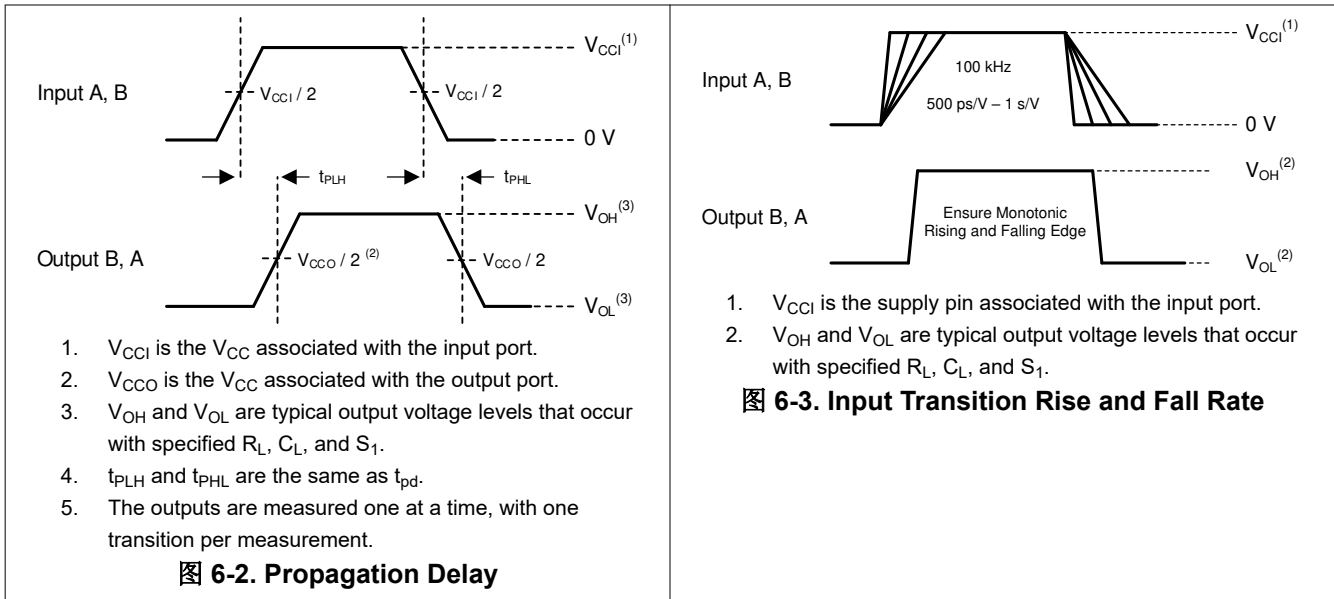
图 6-1. Load Circuit

表 6-1. Load Circuit Parameters

Test Parameter		$S_1$
$t_{pd}$	Propagation (delay) time	Open
$t_{PZL}, t_{PLZ}$	Enable time, disable time	$2 \times V_{CCO}$
$t_{PZH}, t_{PHZ}$	Enable time, disable time	GND

表 6-2. Load Circuit Conditions

$V_{CCO}$	$R_L$	$C_L$	$V_{TP}$
$1.2 \text{ V} \pm 0.1 \text{ V}$	$2 \text{ k}\Omega$	$15 \text{ pF}$	$0.1 \text{ V}$
$1.5 \text{ V} \pm 0.1 \text{ V}$	$2 \text{ k}\Omega$	$15 \text{ pF}$	$0.1 \text{ V}$
$1.8 \text{ V} \pm 0.15 \text{ V}$	$2 \text{ k}\Omega$	$15 \text{ pF}$	$0.15 \text{ V}$
$2.5 \text{ V} \pm 0.2 \text{ V}$	$2 \text{ k}\Omega$	$15 \text{ pF}$	$0.15 \text{ V}$
$3.3 \text{ V} \pm 0.3 \text{ V}$	$2 \text{ k}\Omega$	$15 \text{ pF}$	$0.3 \text{ V}$



- Output waveform on the condition that input is driven to a valid Logic Low.
- Output waveform on the condition that input is driven to a valid Logic High.
- $V_{CCO}$  is the supply pin associated with the output port.
- $V_{OH}$  and  $V_{OL}$  are typical output voltage levels with specified  $R_L$ ,  $C_L$ , and  $S_1$ .
- $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .

**图 6-4. Enable Time And Disable Time**

## 7 Detailed Description

### 7.1 Overview

The SN74AVC4T774 is a 4-bit, dual-supply, noninverting, bi-directional voltage level translation. Pins An and control pins (DIR1, DIR2, DIR3, DIR4 and  $\overline{OE}$ ) are support by  $V_{CCA}$  and pins Bn are support by  $V_{CCB}$ . The A port is able to accept I/O voltages ranging from 1.1V to 3.6V, while the B port can accept I/O voltages from 1.1V to 3.6V. A high on DIR allows data transmission from An to Bn and a low on DIR allows data transmission from B to A when  $\overline{OE}$  is set to low. When  $\overline{OE}$  is set to high, both An and Bn are in the high-impedance state.

### 7.2 Functional Block Diagram

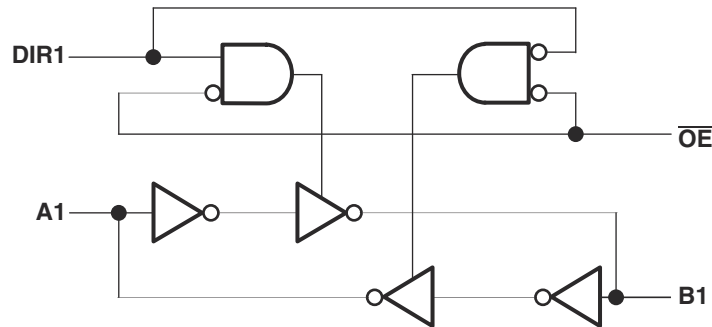


图 7-1. Logic Diagram (Positive Logic)

### 7.3 Feature Description

#### 7.3.1 Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.1V to 3.6V Power-Supply Range

Both  $V_{CCA}$  and  $V_{CCB}$  can be supplied at any voltage between 1.1V and 3.6V making the device suitable for translating between any of the low-voltage nodes (1.2V, 1.8V, 2.5V and 3.3V).

#### 7.3.2 Support High-Speed Translation

SN74AVC4T774 can support high data rate application. The translated signal data rate can be up to 380Mbps when signal is translated from 1.8V to 3.3V.

#### 7.3.3 $I_{off}$ Supports Partial-Power-Down Mode Operation

$I_{off}$  will prevent backflow current by disabling I/O output circuits when device is in partial-power-down mode.

### 7.4 Device Functional Modes

表 7-1. Function Table (Each Bit)

CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A data
L	H	Hi-Z	Enabled	A data to B data
H	X	Hi-Z	Hi-Z	Isolation

## 8 Application and Implementation

### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 8.1 Application Information

The SN74AVC4T774 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The device is designed for use in applications where a push-pull driver is connected to the data I/Os. The max data rate can be up to 380Mbps when the device translate signal is from 1.8V to 3.3V.

### 8.2 Typical Application

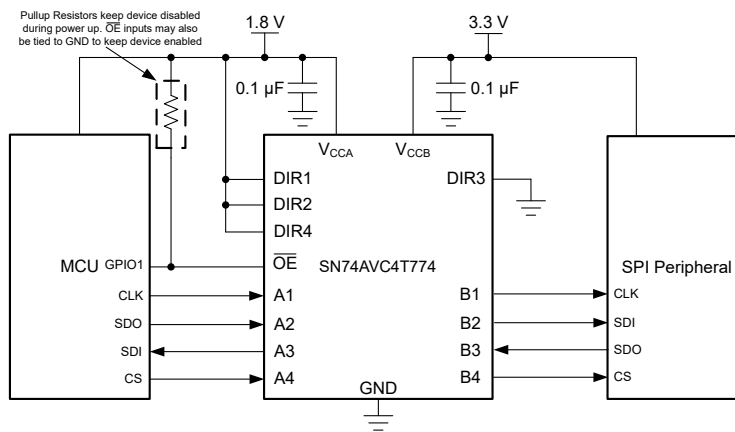


图 8-1. Typical Application of the SN74AVC4T774

#### 8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-1.

表 8-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Input Voltage Range	1.1V to 3.6V
Output Voltage Range	1.1V to 3.6V



## 8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74AVC4T774 device to determine the input voltage range. For a valid logic high, the value must exceed the  $V_{IH}$  of the input port. For a valid logic low, the value must be less than the  $V_{IL}$  of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74AVC4T774 device is driving to determine the output voltage range.

## 8.2.3 Application Curve

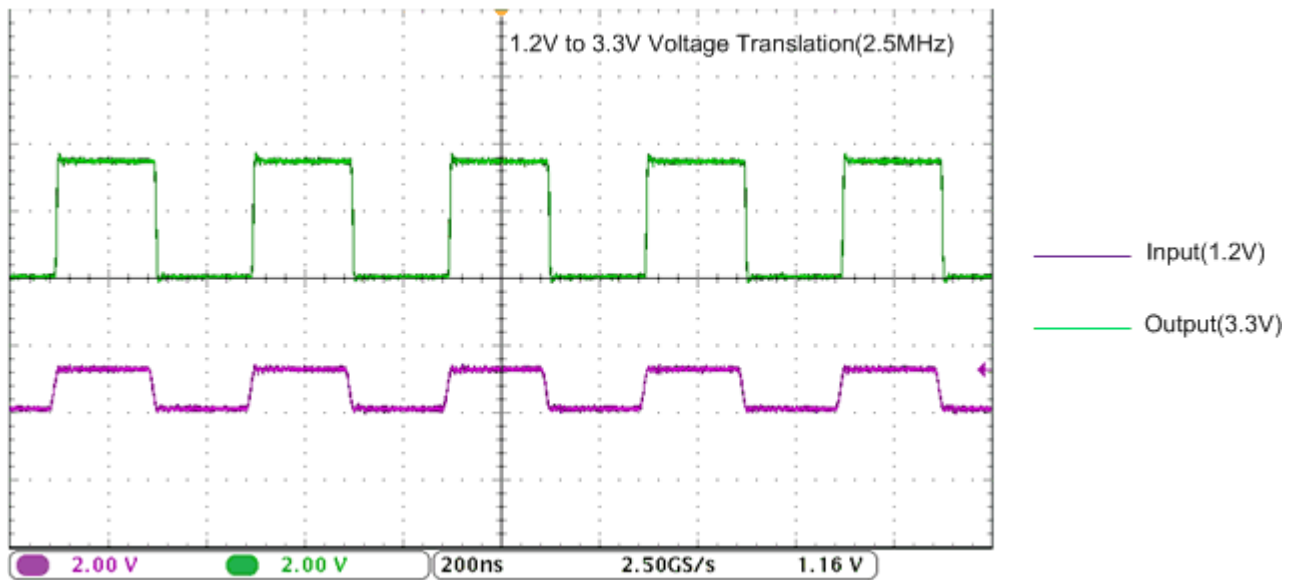


图 8-2. Translation Up (1.2 V to 3.3 V) at 2.5 MHz

## 8.3 Power Supply Recommendations

The SN74AVC4T774 device uses two separate configurable power-supply rails,  $V_{CCA}$  and  $V_{CCB}$ .  $V_{CCA}$  accepts any supply voltage from 1.1V to 3.6V and  $V_{CCB}$  accepts any supply voltage from 1.1V to 3.6V. The A port and B port are designed to track  $V_{CCA}$  and  $V_{CCB}$  respectively allowing for low-voltage, bi-directional translation between any of the 1.2V, 1.5V, 1.8V, 2.5V and 3.3V voltage nodes.

The output-enable  $\overline{OE}$  input circuit is designed so that it is supplied by  $V_{CCA}$  and when the  $\overline{OE}$  input is high, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power-up or power-down, the  $\overline{OE}$  input pin must be tied to  $V_{CCA}$  through a pullup resistor and must not be enabled until  $V_{CCA}$  and  $V_{CCB}$  are fully ramped and stable. The minimum value of the pullup resistor to  $V_{CCA}$  is determined by the current-sinking capability of the driver.

## 8.4 Layout

### 8.4.1 Layout Guidelines

For reliability of the device, following common printed-circuit board layout guidelines are recommended:

- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.
- Placing pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depending on the system requirements

### 8.4.2 Layout Example

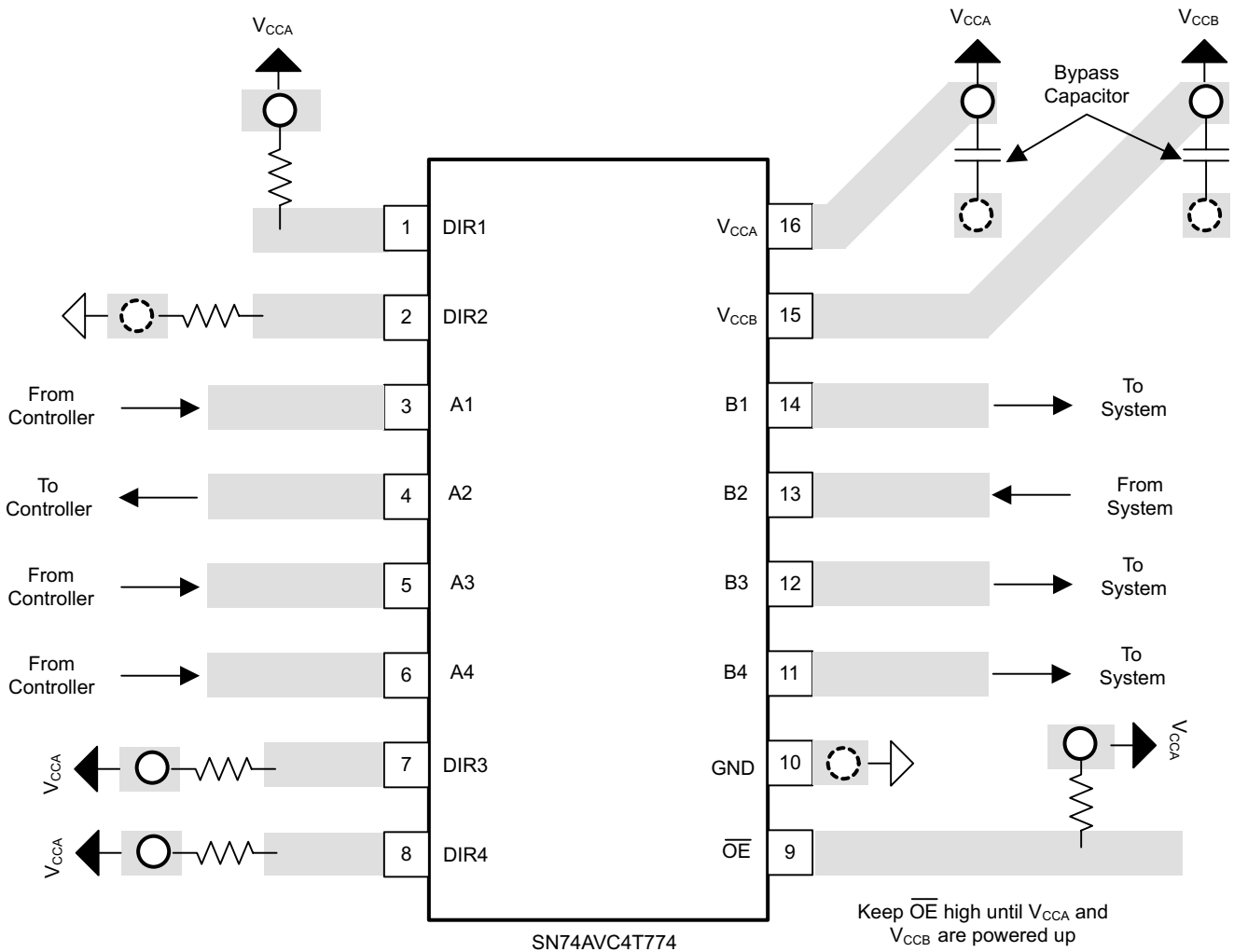


图 8-3. PCB Layout Example

## 9 Device and Documentation Support

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [16-Bit Widebus Logic Families in 56-Ball, 0.65-mm Pitch Very Thin Fine-Pitch BGA application report](#)
- Texas Instruments, [AVC Logic Family Technology and Applications application report](#)
- Texas Instruments, [AVC Advanced Very-Low-Voltage CMOS Logic Data Book, March 2000 data book](#)
- Texas Instruments, [Dynamic Output Control \(DOC\) Circuitry Technology And Applications \(Rev. B\) application report](#)
- Texas Instruments, [Introduction to Logic application report](#)
- Texas Instruments, [LCD Module Interface Application Clip brochure](#)
- Texas Instruments, [Logic Cross-Reference application note](#)
- Texas Instruments, [Logic Guide marketing selection guide](#)
- Texas Instruments, [LOGIC Pocket Data Book data book](#)
- Texas Instruments, [Selecting the Right Level Translation Solution application report](#)
- Texas Instruments, [Semiconductor Packing Material Electrostatic Discharge \(ESD\) Protection application report](#)
- Texas Instruments, [Solving CMOS Transition Rate Issues Using Schmitt Trigger Solution white paper](#)
- Texas Instruments, [Standard Linear & Logic for PCs, Servers & Motherboards brochure](#)
- Texas Instruments, [TI Tablet Solutions solution guide](#)
- Texas Instruments, [Understanding and Interpreting Standard-Logic Data Sheets application report](#)
- Texas Instruments, [Voltage Translation Between 3.3-V, 2.5-V, 1.8-V, and 1.5-V Logic Standards application report](#)

#### 9.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

#### 9.3 支持资源

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链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

#### 9.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 10 Revision History

注：以前版本的页码可能与当前版本的页码不同

<b>Changes from Revision G (May 2021) to Revision H (March 2024)</b>	<b>Page</b>
• 向数据表中添加了 BQB 和 DYY 封装.....	1
<hr/>	
<b>Changes from Revision F (November 2020) to Revision G (May 2021)</b>	<b>Page</b>
• 更新了说明部分典型应用原理图.....	1
• Updated the <i>Typical Application of the SN74AVC4T774</i> figure in the <i>Typical Application</i> section.....	16
<hr/>	
<b>Changes from Revision E (October 2017) to Revision F (November 2020)</b>	<b>Page</b>
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• $V_{CCA}$ and $V_{CCB}$ supply voltage min in <i>Recommended Operating Conditions</i> table expanded down to 1.1V.....	6
<hr/>	
<b>Changes from Revision D (January 2015) to Revision E (October 2017)</b>	<b>Page</b>
• Added Storage junction temperature to <i>Absolute Maximum Ratings</i> .....	6
<hr/>	
<b>Changes from Revision C (December 2014) to Revision D (January 2015)</b>	<b>Page</b>
• Changed Pin Functions table order for Pins B4, B3, B2 and B1.....	4
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<b>Changes from Revision B (May 2008) to Revision C (December 2014)</b>	<b>Page</b>
• 添加了引脚配置和功能部分、ESD 等级表、特性说明部分、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分.....	1

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74AVC4T774RSVR-NT	ACTIVE	UQFN	RSV	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZVK	<a href="#">Samples</a>
74AVC4T774RSVRG4	ACTIVE	UQFN	RSV	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZVK	<a href="#">Samples</a>
SN74AVC4T774PW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT774	<a href="#">Samples</a>
SN74AVC4T774PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT774	<a href="#">Samples</a>
SN74AVC4T774RGYR	ACTIVE	VQFN	RGY	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	WT774	<a href="#">Samples</a>
SN74AVC4T774RSVR	ACTIVE	UQFN	RSV	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZVK	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74AVC4T774RSVR-NT	UQFN	RSV	16	3000	180.0	9.5	2.1	2.9	0.75	4.0	8.0	Q1
SN74AVC4T774PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AVC4T774RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
SN74AVC4T774RSVR	UQFN	RSV	16	3000	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74AVC4T774RSVR-NT	UQFN	RSV	16	3000	189.0	185.0	36.0
SN74AVC4T774PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74AVC4T774RGYR	VQFN	RGY	16	3000	356.0	356.0	35.0
SN74AVC4T774RSVR	UQFN	RSV	16	3000	189.0	185.0	36.0



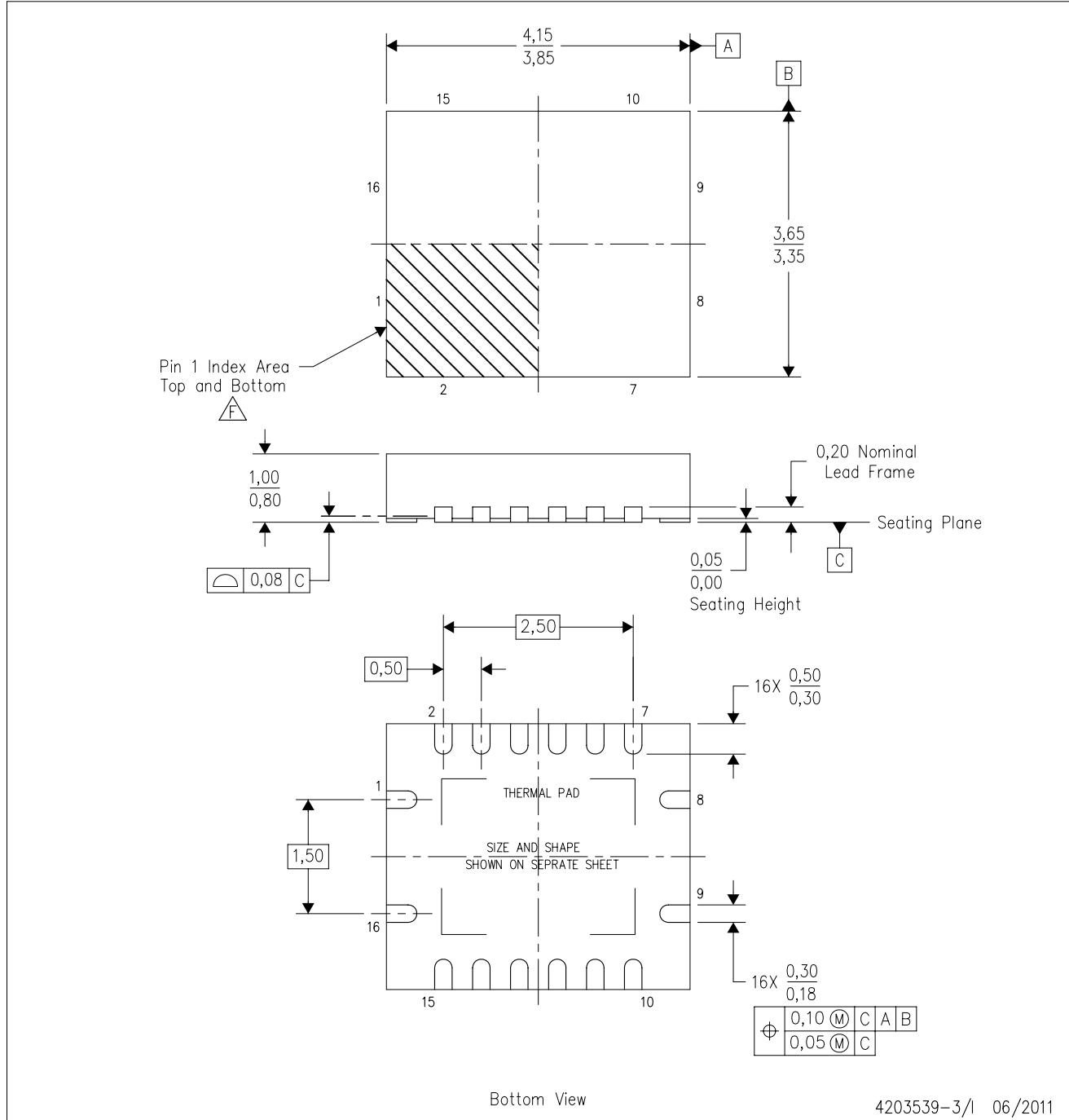
**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74AVC4T774PW	PW	TSSOP	16	90	530	10.2	3600	3.5

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - G. Package complies to JEDEC MO-241 variation BA.

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD

**THERMAL INFORMATION**

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-3/P 03/14

NOTE: All linear dimensions are in millimeters

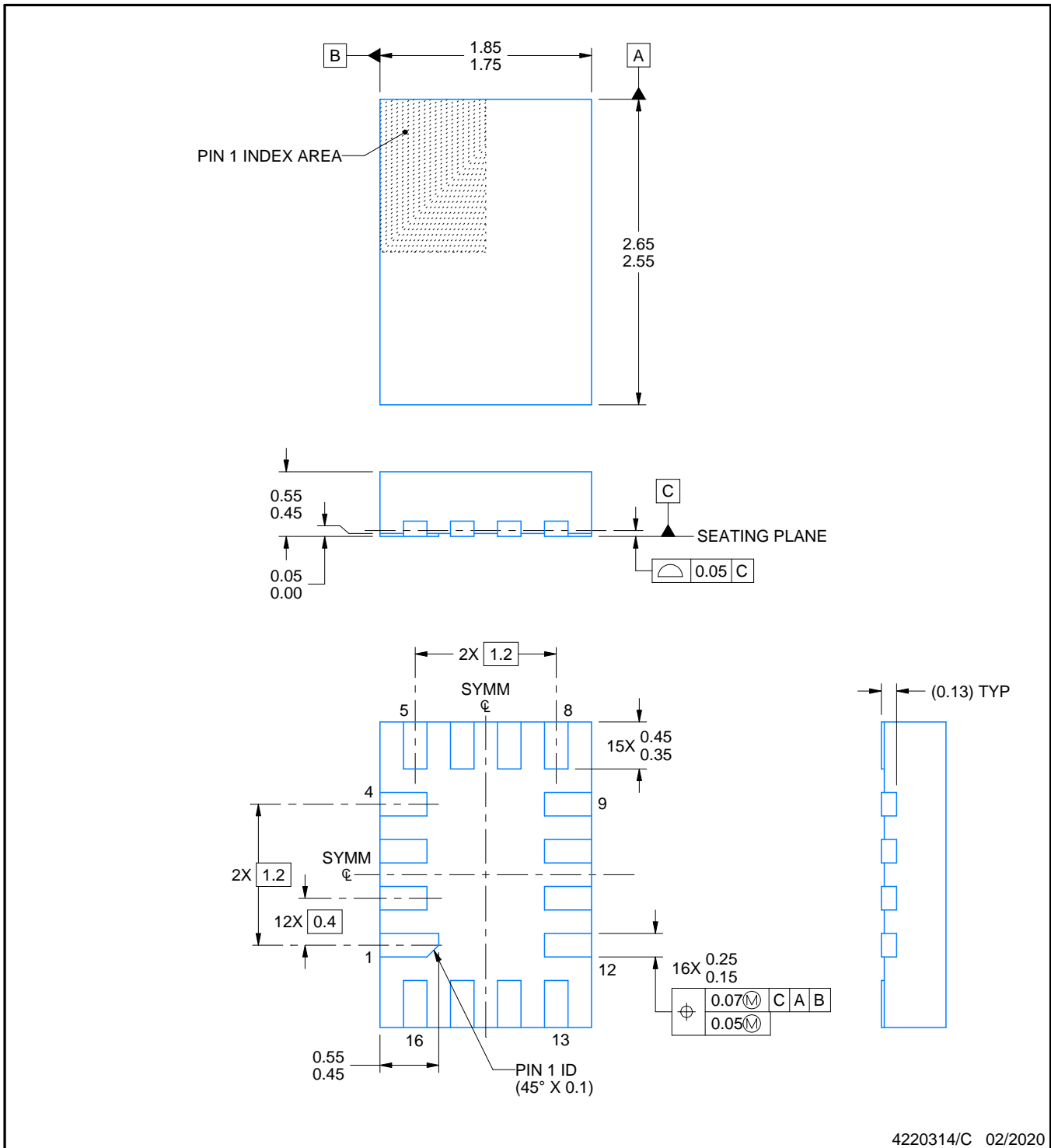
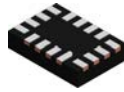
RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-3/P 03/14

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.



NOTES:

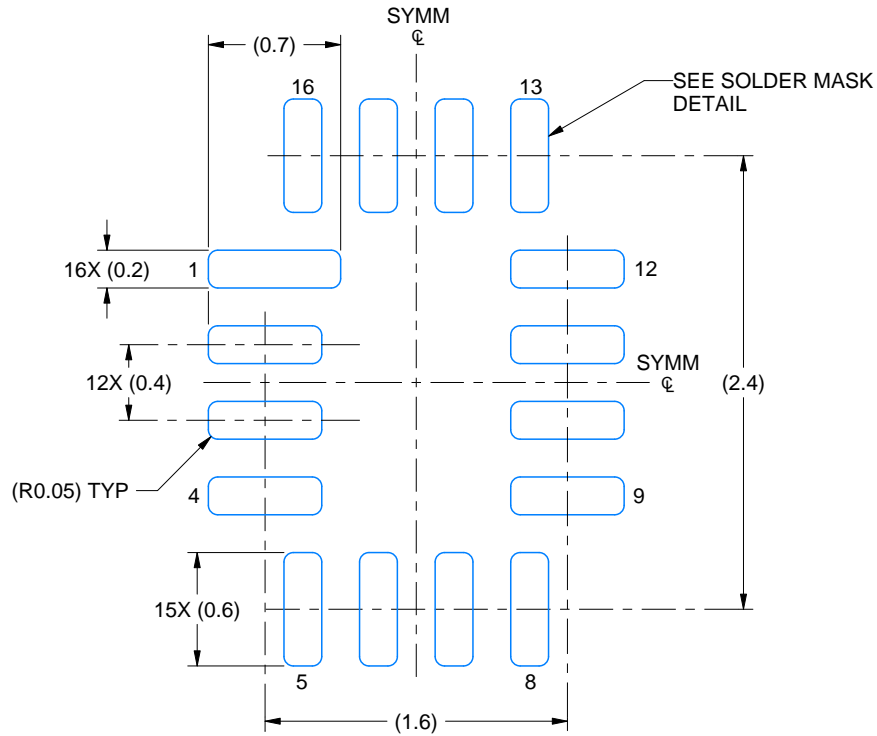
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

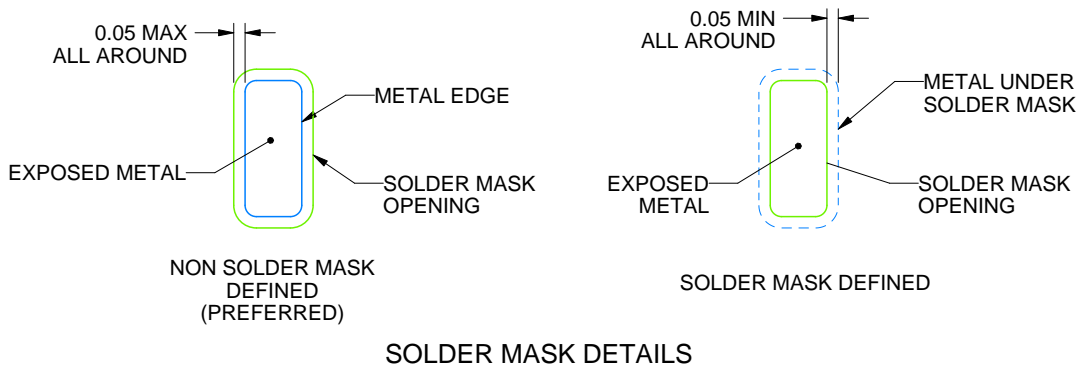
RSV0016A

UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 25X



4220314/C 02/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

RSV0016A

UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 25X

4220314/C 02/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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