SN74HCS08-Q1 Automotive Quadruple 2-Input Positive-AND Gates with Schmitt-trigger Inputs

1 Features

- AEC-Q100 Qualified for Automotive Applications:
  - Device Temperature Grade 1: –40°C to +125°C, T_A
- Wide Operating Voltage Range: 2 V to 6 V
- Schmitt-trigger Inputs Allow for Slow or Noisy Input Signals
- Outputs Can Drive Up To 10 LSTTL Loads
- ±8-mA Output Drive at 5 V
- ESD Protection as per AEC Q-100
  - 4000-V Human-Body Model (H2)
  - 1500-V Charged-Device Model (C6)

2 Applications

- Combine power good signals for multiple power rails
- Prevent a signal from being passed until multiple conditions are true
- Combine active-low error signals

3 Description

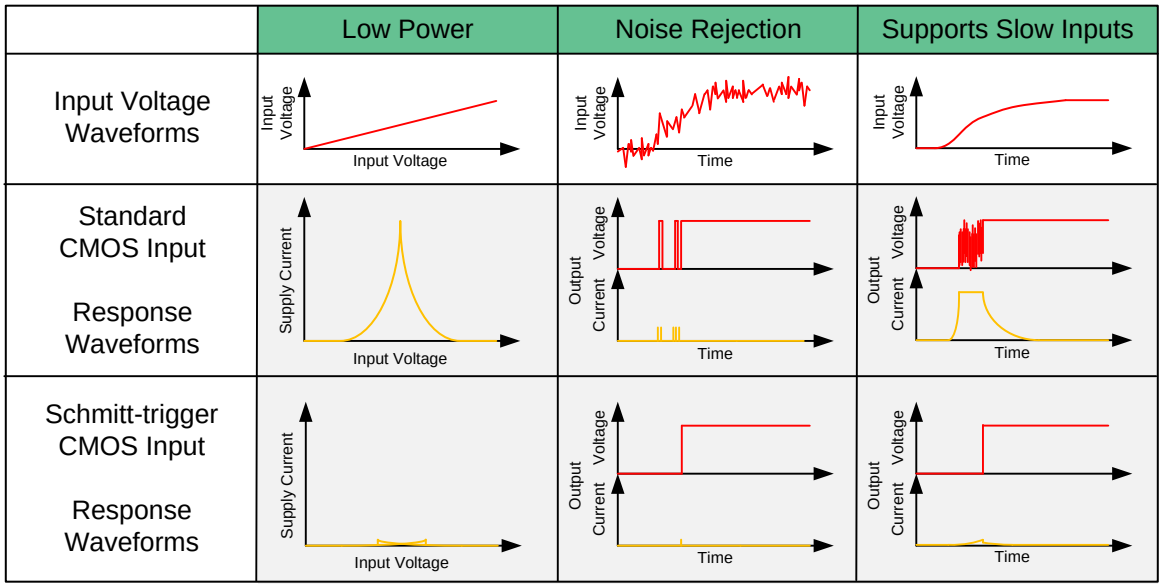
This device contains two independent 2-input AND gates. It performs the Boolean function Y = A ● B in positive logic.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74HCS08QPWRQ1	TSSOP (14)	6.40 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Benefits of Schmitt-trigger Inputs in the HCS Logic Family



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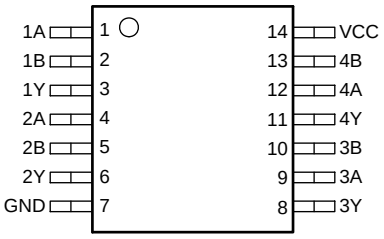
4 Revision History

DATE	REVISION	NOTES
May 2019	*	Initial release.

5 Pin Configuration and Functions

PW Package
14-Pin TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1A	1	Input	Channel 1, Input A
1B	2	Input	Channel 1, Input B
1Y	3	Output	Channel 1, Output Y
2A	4	Input	Channel 2, Input A
2B	5	Input	Channel 2, Input B
2Y	6	Output	Channel 2, Output Y
GND	7	—	Ground
3Y	8	Output	Channel 3, Output Y
3A	9	Input	Channel 3, Input A
3B	10	Input	Channel 3, Input B
4Y	11	Output	Channel 4, Output Y
4A	12	Input	Channel 4, Input A
4B	13	Input	Channel 4, Input B
V_{CC}	14	—	Positive Supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input clamp current(2)	$V_I < 0$ or $V_I > V_{CC} + 0.5$		±20	mA
I_{OK}	Output clamp current(2)	$V_O < 0$ or $V_O > V_{CC} + 0.5$		±20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		±25	mA
I_{CC}	Continuous output current through V_{CC} or GND			±50	mA
T_J	Junction temperature(3)			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed. Do not exceed the absolute maximum voltage supply rating.
(3) Guaranteed by design.

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6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1] HBM ESD Classification Level 2	±4000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	±1500	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2		6	V
V_I	Input voltage	0		V_{CC} + 0.5	V
V_O	Output voltage	0		V_{CC} + 0.5	V
$\Delta t/\Delta v$	Input transition rise and fall rate			Unlimited	ns/V
T_A	Ambient temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC		SN74HCS08-Q1 PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	151.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	79.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	94.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	25.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	94.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP[1]	MAX	UNIT
V_{T+}	Positive switching threshold			2 V	0.7	1.22	1.5	V
				4.5 V	1.55	2.43	3.15	
				6 V	2.1	3.15	4.2	
V_{T-}	Negative switching threshold			2 V	0.3	0.8	1	V
				4.5 V	0.9	1.83	2.45	
				6 V	1.2	2.4	3.2	
ΔV_T	Hysteresis (V_{T+} - V_{T-})			2 V	0.2	0.422	1.2	V
				4.5 V	0.400	0.600	2.1	
				6 V	0.5	0.750	2.5	
V_{OH}	High-level output voltage	V_I = V_{IH} or V_{IL}	I_{OH} = -20 µA	2 V to 6 V	V_{CC} – 0.1	V_{CC} – 0.002		V
			I_{OH} = -6 mA	4.5 V	4	4.2		
			I_{OH} = -7.8 mA	6 V	5.4	5.66		
V_{OL}	Low-level output voltage	V_I = V_{IH} or V_{IL}	I_{OL} = 20 µA	2 V to 6 V		0.002	0.1	V
			I_{OL} = 6 mA	4.5 V		0.18	0.28	
			I_{OL} = 7.8 mA	6 V		0.22	0.33	
I_I	Input leakage current	V_I = V_{CC} or 0		6 V		±100	±1000	nA
I_{CC}	Supply current	V_I = V_{CC} or 0, I_O = 0		6 V		0.1	2	µA
C_i	Input capacitance			2 V to 6 V		3	10	pF

(1) T_A = 25°C

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Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP(1)	MAX	UNIT
C_{pd}	Power dissipation capacitance per gate	No load		2 V to 6 V		10		pF

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	TYP(2)	MAX	UNIT
t_{pd}	Propogation delay	A or B	Y	2 V		19	42	ns
				4.5 V		8	17	
				6 V		7	14	
t_t	Transition-time		Y	2 V		9	17	ns
				4.5 V		5	8	
				6 V		4	7	

(1) See the Parameter Measurement Information section for more information.
(2) T_A = 25°C

6.7 Typical Characteristics

T_A = 25°C

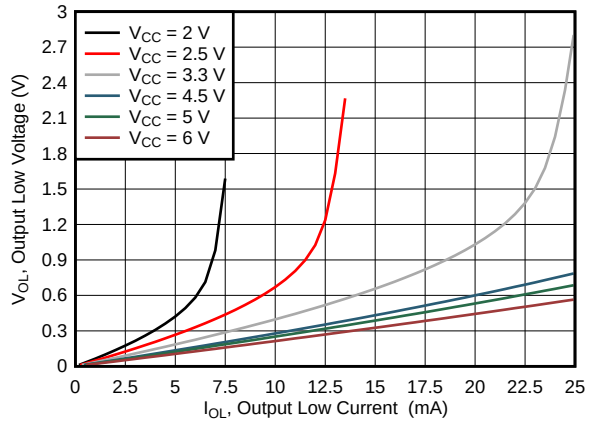

Figure 1. Typical output low voltage versus sink current across common supply values

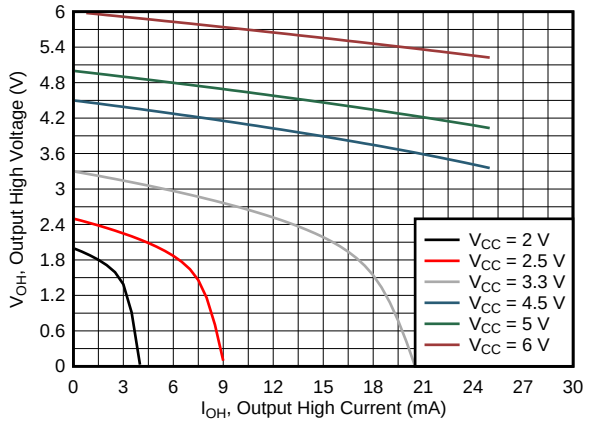

Figure 2. Typical output high voltage versus source current across common supply values

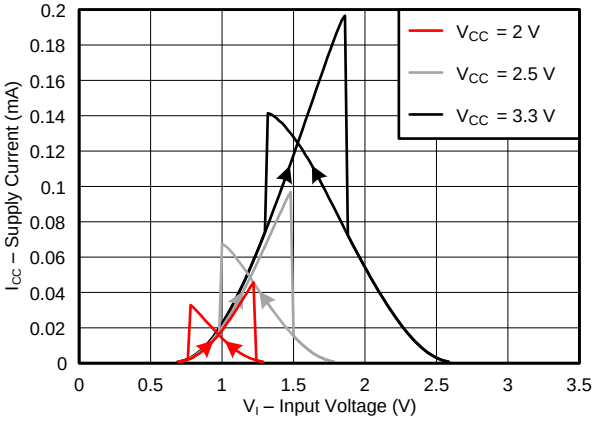

Figure 3. Typical supply current versus input voltage across common supply values (2 V to 3.3 V)

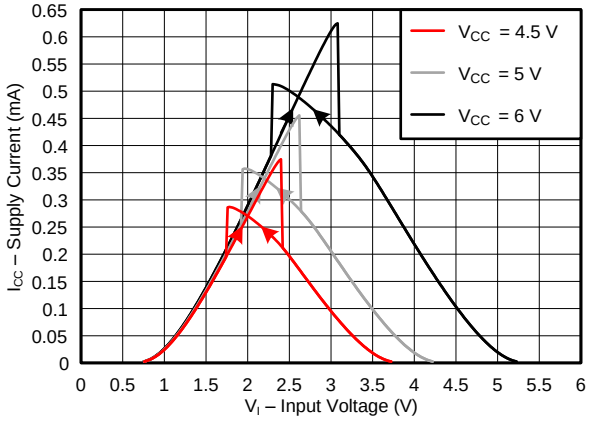

Figure 4. Typical supply current versus input voltage across common supply values (4.5 V to 6 V)

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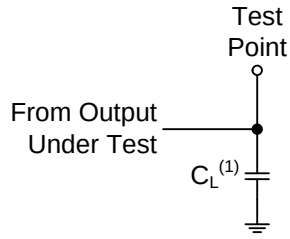
7 Parameter Measurement Information

- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_t < 2.5 ns.
- The outputs are measured one at a time, with one input transition per measurement.



C_L= 50 pF and includes probe and jig capacitance.

Figure 5. Load Circuit

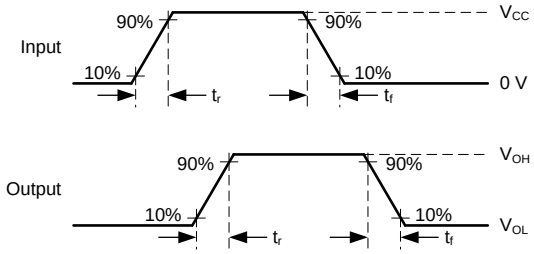
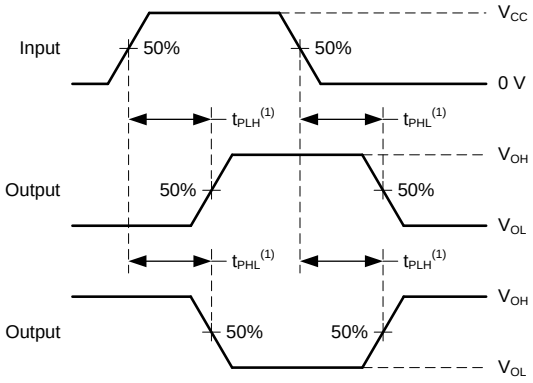


Figure 6. Voltage Waveforms Transition Times



The maximum between t_{PLH} and T_{PHL} is used for t_{pd}.

Figure 7. Voltage Waveforms Propagation Delays

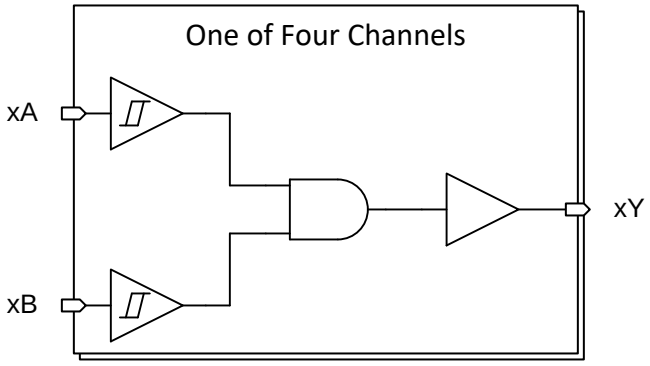
ADVANCE INFORMATION

8 Detailed Description

8.1 Overview

The SN74HCS08-Q1 includes four 2-input AND gates with Schmitt-trigger inputs. These CMOS logic gates operate independently.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined the in the *Absolute Maximum Ratings* must be followed at all times.

8.3.2 CMOS Schmitt-Trigger Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the *Electrical Characteristics*, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs slowly will also increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see application reportUnderstanding Schmitt Triggers (SCEA046).

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Feature Description (continued)

8.3.3 Positive and Negative Clamping Diodes

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in Figure 8.

CAUTION

Voltages beyond the values specified in the table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

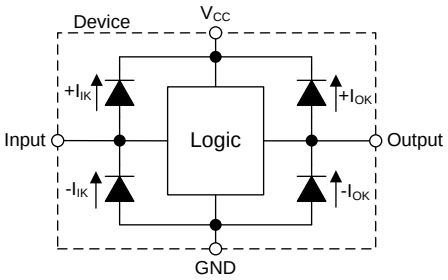

Figure 8. Electrical Placement of Clamping Diodes for Each Input and Output

8.4 Device Functional Modes

Table 1. Function Table

INPUTS		OUTPUT Y
A	B	
H	H	H
L	X	L
X	L	L

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

In this application, three 2-input AND gates are combined to produce a 4-input AND gate function as shown in Figure 9. The fourth gate can be used for another application in the system, or the inputs can be grounded and the channel left unused.

The SN74HCS08-Q1 is used to directly control the $\overline{\text{RESET}}$ pin of a motor controller. The controller requires four input signals to all be HIGH before being enabled, and should be disabled in the event that any one signal goes LOW. The 4-input AND gate function combines the four individual reset signals into a single active-low reset signal.

Many power good signals utilize open-drain outputs which can produce slow input transition rates when they transition from LOW to Hi-Z mode. This makes the SN74HCS08-Q1 ideal for the application since it has Schmitt-trigger inputs that do not have input transition rate requirements.

9.2 Typical Application

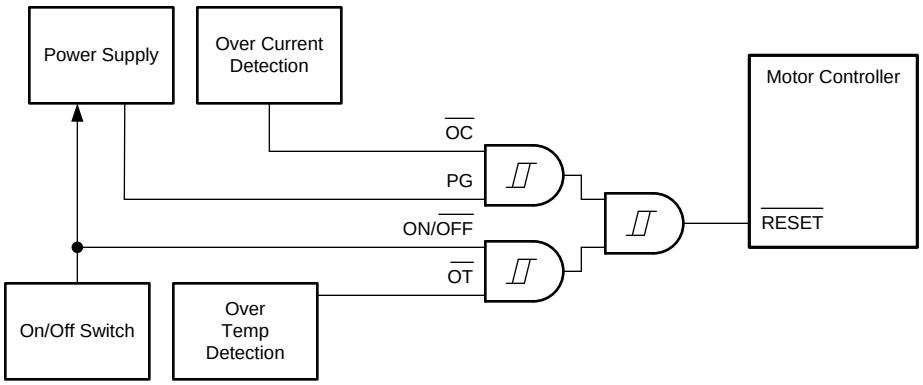

Figure 9. Application block diagram

9.2.1 Design Requirements

- All signals in the system operate at 5 V
- The motor controller should be disabled if any of these conditions apply:
  - Power Supply is not ready (PG)
  - Excessive current is detected ($\overline{\text{OC}}$)
  - Excessive temperature is detected ($\overline{\text{OT}}$)
  - The power switch is in the OFF position (ON/$\overline{\text{OFF}}$)

9.2.1.1 Power

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the output voltage and other characteristics as described in the *Electrical Characteristics*.

The supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74HCS08-Q1 plus the maximum supply current, I_{CC}, listed in *Electrical Characteristics*. The logic device can only source or sink as much current as it is provided at the supply and ground pins, respectively. Be sure not to exceed the maximum total current through GND or V_{CC} listed in *Absolute Maximum Ratings*.

ADVANCE INFORMATION

Typical Application (continued)

The SN74HCS08-Q1 can drive a load with a total capacitance less than or equal to 50 pF connected to a high-impedance CMOS input while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed 70 pF.

Total power consumption can be calculated using the information provided in CMOS Power Consumption and C_{pd} Calculation.

Thermal increase can be calculated using the information provided in Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices.

CAUTION

The maximum junction temperature, T_J(max) listed in Absolute Maximum Ratings, is an *additional limitation* to prevent damage to the device. Do not violate any values listed in the Absolute Maximum Ratings. These limits are provided to prevent damage to the device.

9.2.1.2 Inputs

Input signals must cross V_{t-}(min) to be considered a logic LOW, and V_{t+}(max) to be considered a logic HIGH. Do not exceed the maximum input voltage range found in *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74HCS08-Q1, as specified in *Electrical Characteristics*, and the desired input transition rate. A 10-kΩ resistor value is often used due to these factors.

The SN74HCS08-Q1 has no input signal transition rate requirements because it has Schmitt-trigger inputs.

Another benefit to having Schmitt-trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the ΔV_T(min) in the *Electrical Characteristics*. This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than V_{CC} or ground is plotted in Figure 3 and Figure 4.

Refer to Feature Description for additional information regarding the inputs for this device.

9.2.1.3 Outputs

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. Similarly, the ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*. The plots in Figure 1 and Figure 2 provide a typical relationship between output voltage and current for this device.

Unused outputs can be left floating.

Refer to Feature Description for additional information regarding the outputs for this device.

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Typical Application (continued)

9.2.2 Detailed Design Procedure

1. The motor controller requires a 5-V input signal, so the SN74HCS08-Q1 is powered from the same 5-V regulated supply as the controller. This ensures that the gate will be active any time that the controller is active.
2. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in Figure 11.
3. Ensure the capacitive load at the output is ≤ 70 pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74HCS08-Q1 to the Motor Controller (or other receiving device).
4. Ensure the resistive load at the output is larger than (V_{CC} / 25 mA) Ω. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.
5. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, CMOS Power Consumption and Cpd Calculation (SCAA035).

9.2.3 Application Curves

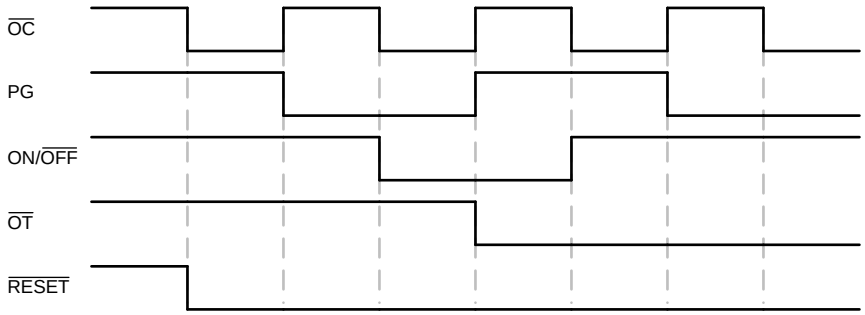

Figure 10. Application timing diagram

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10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Absolute Maximum Ratings* table. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in Figure 11.

11 Layout

11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

11.2 Layout Example

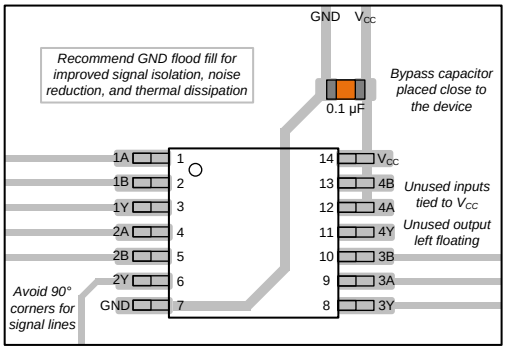


Figure 11. Example layout for the PW package for 2-input logic gates

ADVANCE INFORMATION

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- HCMOS Design Considerations
- CMOS Power Consumption and CPD Calculation
- Designing With Logic
- 14-24-Logic-EVM User's Guide
- Implications of Slow or Floating CMOS Inputs

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PSN74HCS08QPWRQ1	ACTIVE	TSSOP	PW	14	2000	TBD	Call TI	Call TI	-40 to 125		Samples
SN74HCS08QPWRQ1	PREVIEW	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS08Q	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

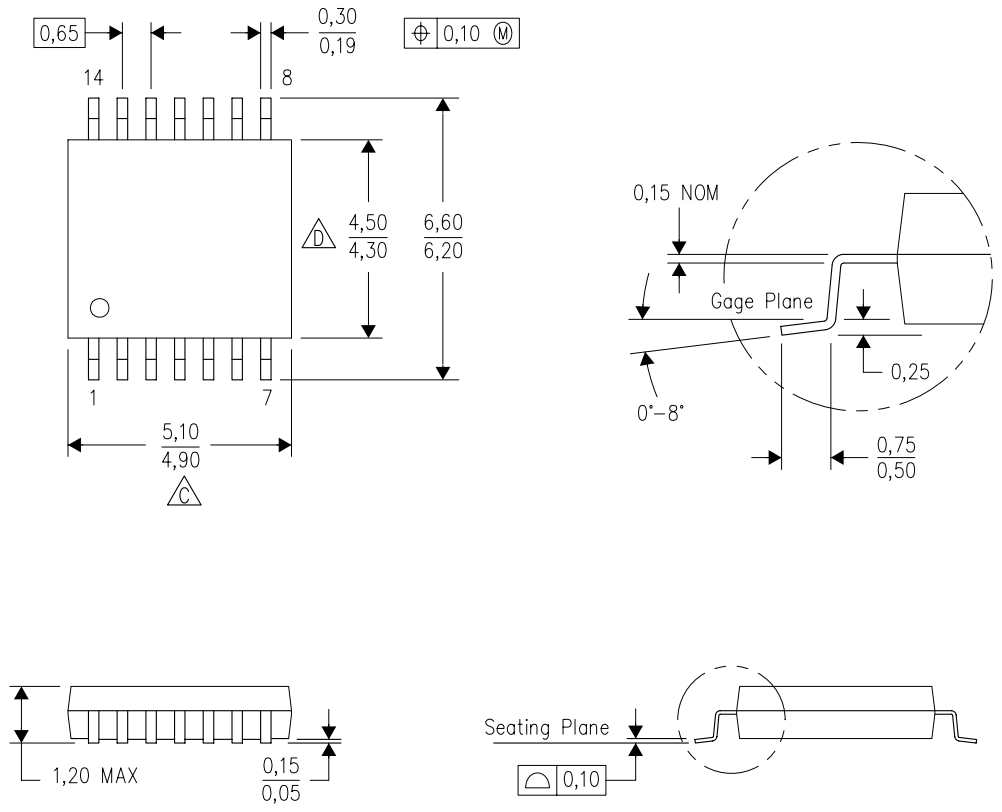
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

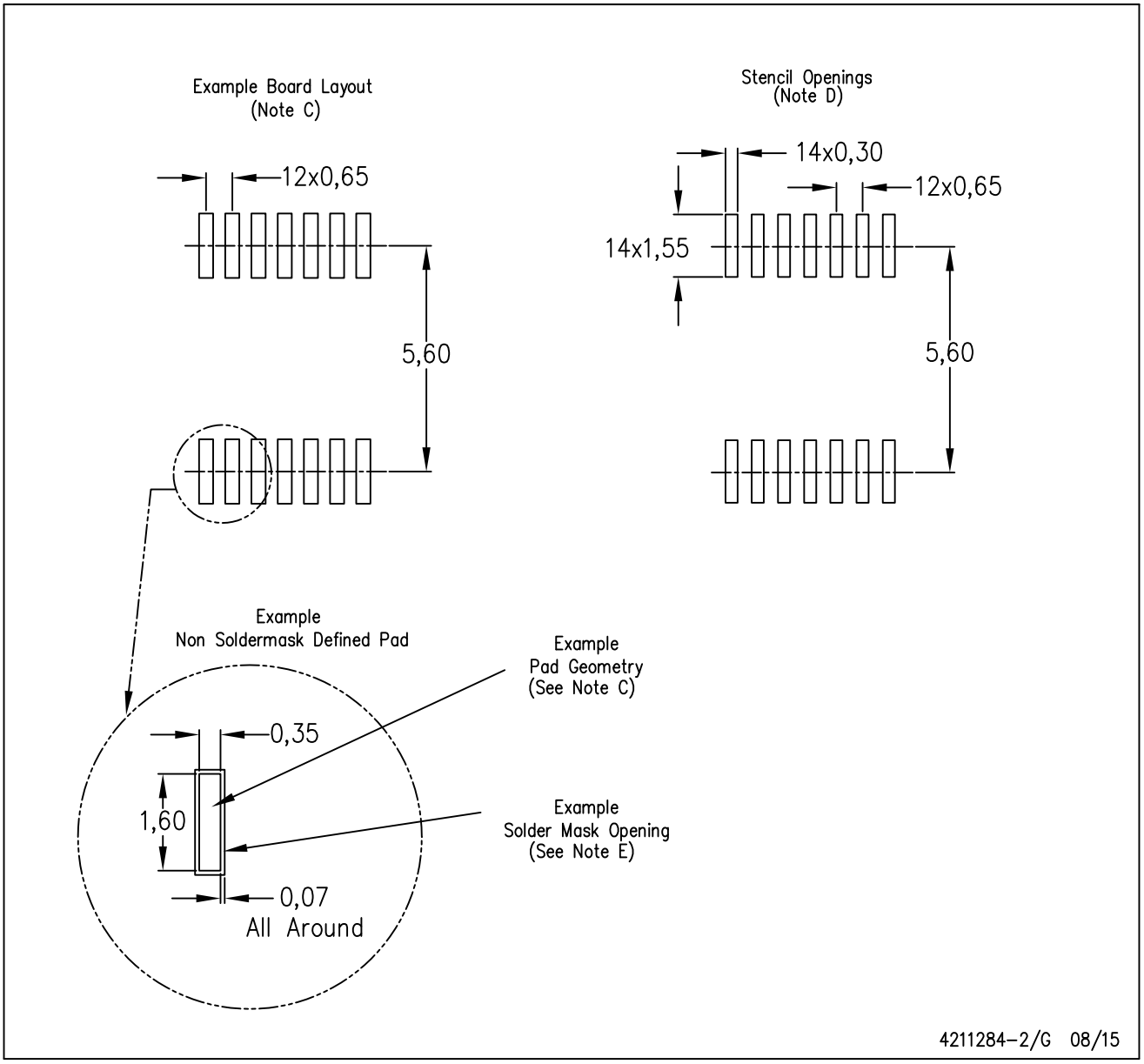
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265