

TPS92682-Q1 Dual-channel constant-voltage and constant-current controller with SPI interface

1 Features

- AEC-Q100 grade 1 qualified
- Wide input voltage range: 4.5 V to 65 V
- Better than $\pm 4\%$ LED current accuracy over -40°C to 150°C junction temperature Range
- SPI communication interface
- SPI programmable features:
 - Spread spectrum for Improved EMI
 - Soft-start timing
 - ILED current and output voltage settings
 - Current limit, overvoltage, fault-timer
 - Single vs dual phase
 - CV and CC mode configuration
- Dual channel peak-current-mode (PCM) controller
- Low Input offset rail-to-rail current sense amplifier
- Analog dimming
- External series FET PWM dimming with integrated P-channel driver interface
 - Over 1000:1 PWM dimming range
- Open drain fault flag indicator per channel
- Up to 1-MHz Programmable switching frequency with external clock synchronization capability
- Comprehensive programmable fault protection circuitry

2 Applications

- Automotive forward lighting
- Emergency vehicles
- General lighting

3 Description

The TPS92682-Q1 is a dual-channel, peak current-mode controller with SPI communication interface. The device is programmable to operate in constant-voltage (CV) or constant-current (CC) modes.

In CV mode, TPS92682-Q1 can be programmed to operate as two independent or dual-phase Boost voltage regulators. The output voltage can be programmed using an external resistor voltage divider, and a SPI-programmable 8-bit DAC.

In CC mode, the device is designed to support dual channel step-up or step-down LED driver topologies. LED current can be independently modulated using analog or PWM dimming techniques. Analog dimming with over 15:1 range, is obtained using a programmable 8-bit DAC. PWM dimming of LED current is achieved either by directly modulating the PWM input pins with the desired duty cycle, or using a SPI-programmable 10-bit PWM counter. The optional PDRV gate driver output can be used to drive an external P-Channel series MOSFET.

The TPS92682-Q1 incorporates an advanced SPI-programmable diagnostic and fault protection mechanism including: cycle-by-cycle current limit, output overvoltage and undervoltage protection, ILED overcurrent protection, and thermal warning. The device also includes an open-drain fault indicator output per channel.

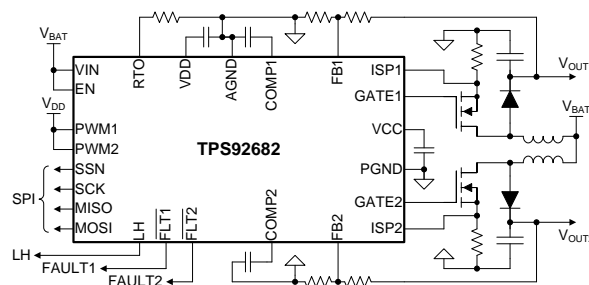
The TPS92682-Q1 includes an LH pin, when pulled high, initiates the limp home (LH) condition. In LH mode, the device uses a separate set of SPI-programmed registers.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS92682-Q1	VQFN (32)	5.0 mm x 5.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2019	*	Initial release.

5 Device and Documentation Support

5.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

5.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

5.3 Trademarks

E2E is a trademark of Texas Instruments.

5.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

6.1 VQFN Package

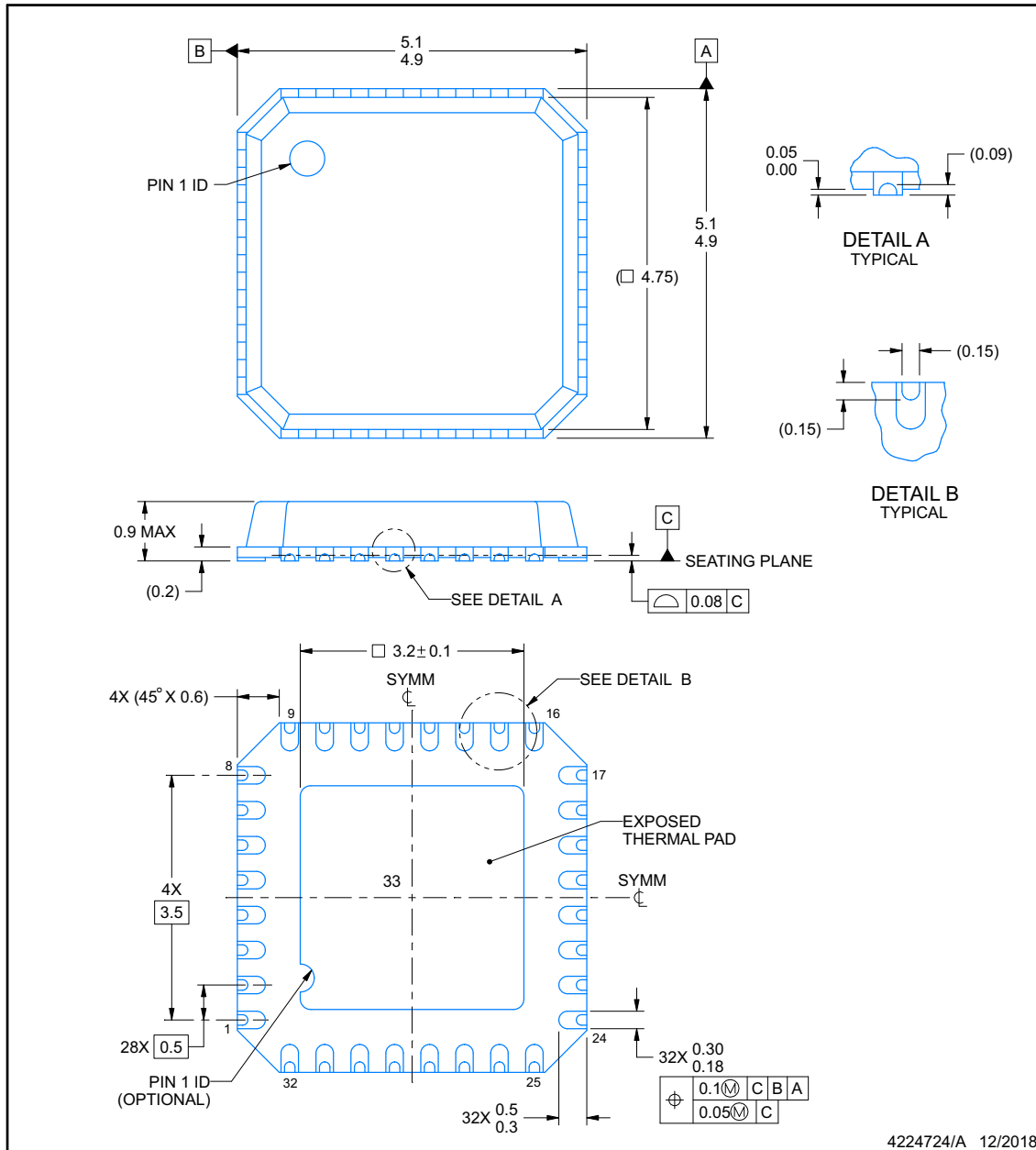


PACKAGE OUTLINE

RHM0032C

VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

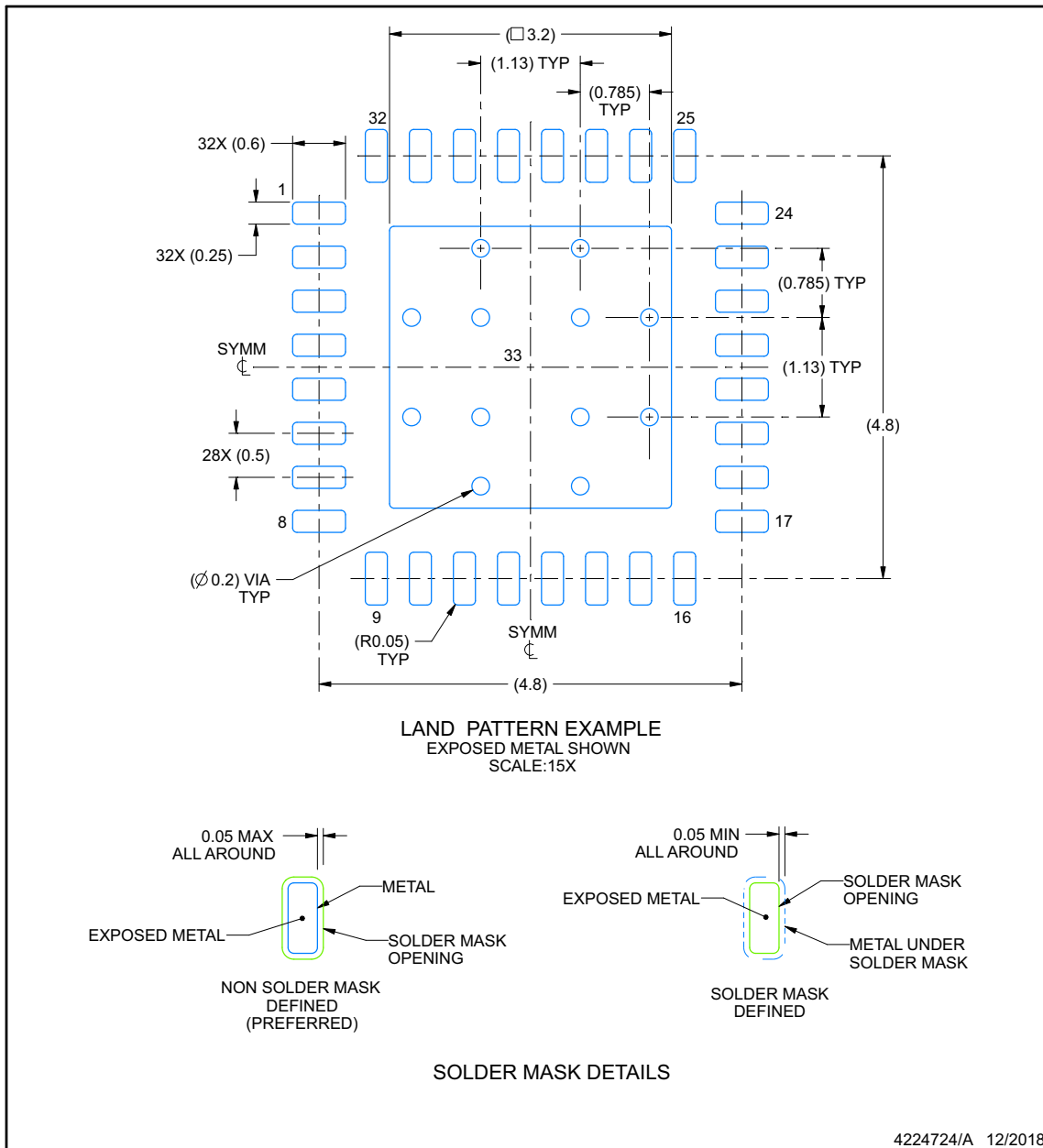
VQFN Package (continued)

EXAMPLE BOARD LAYOUT

RHM0032C

VQFNP - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

ADVANCE INFORMATION

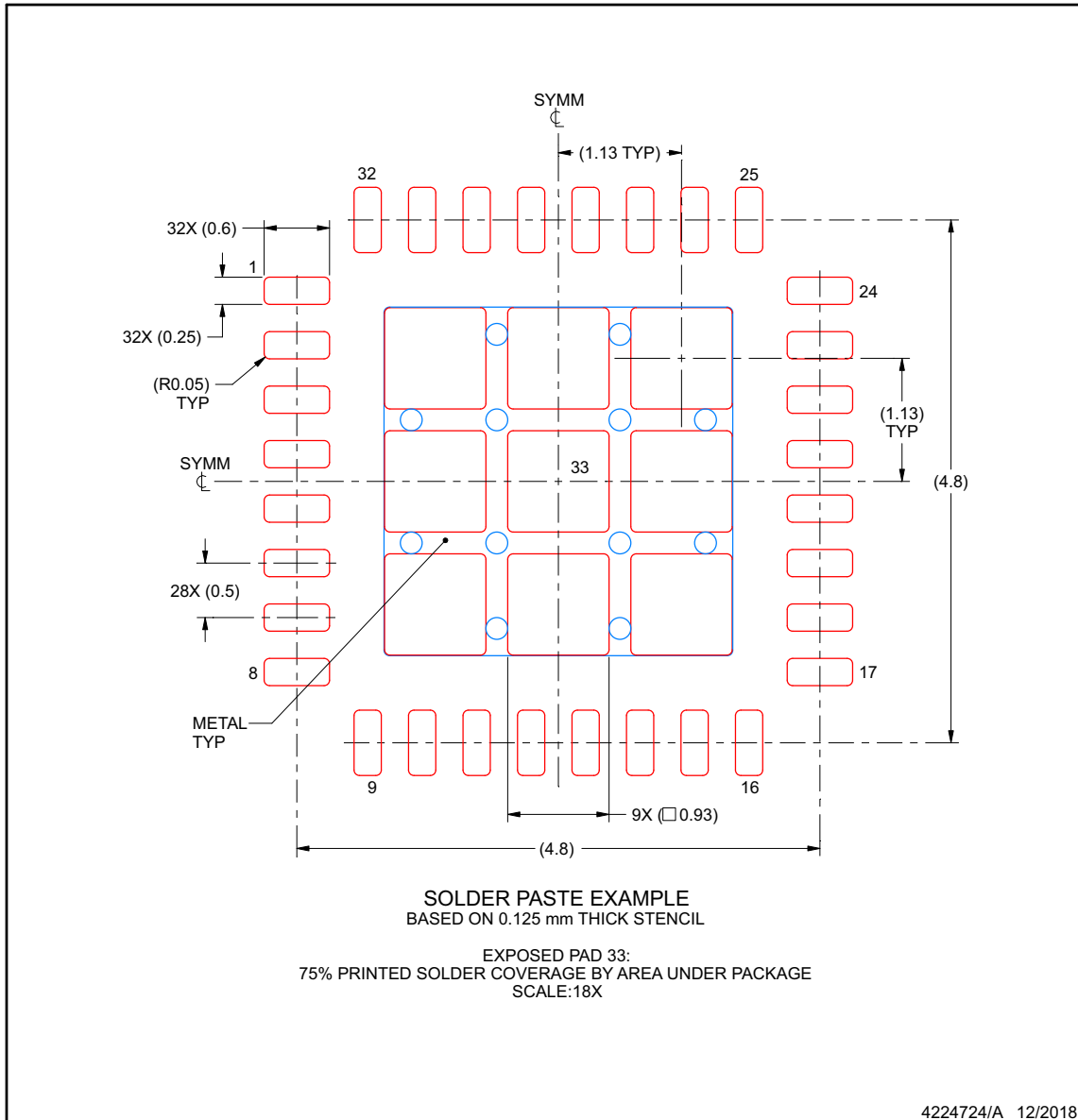
VQFN Package (continued)

EXAMPLE STENCIL DESIGN

RHM0032C

VQFNP - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPS92682QRHMQ1	ACTIVE	VQFN	RHM	32	100	TBD	Call TI	Call TI	-40 to 125		Samples
TPS92682QRHMQ1	PREVIEW	VQFN	RHM	32	100	TBD	Call TI	Call TI	-40 to 125	TPS 92682Q	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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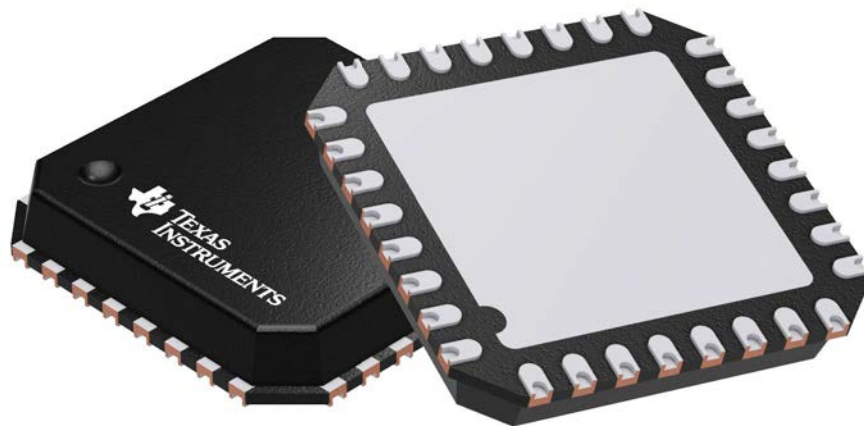
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GENERIC PACKAGE VIEW

RHM 32

VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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