TPSM82480 5.5V 输入、6A 降压转换器模块

1 选项
- 超小型 7.9 x 3.6 x 1.5mm 电源模块
- 输出电流为 6A
- 反馈电压精度为 ±1%
- 输入电压范围：2.4V 至 5.5V
- 输出电压范围：0.6V 至 5.5V
- 典型静态电流为 23μA
- 输出电压选择
- 相移操作
- 自动节能模式
- 强制 PWM 模式 选项
- 可调节软启动
- 电源正常和温度正常输出
- 欠压锁定
- 过流和短路保护
- 过热保护
- 工作温度范围：-40°C 至 125°C

2 应用
- 薄型负载点电源
- 存储、服务器、适配器
- 工业 PC/嵌入式 PC/FPGA 电源
- 无线基站
- 测试和测量

3 说明
TPSM82480 是一款适用于低厚度负载点电源的同步降压直流/直流转换器模块。2.4V 至 5.5V 的输入电源范围使其既可以通过典型的 3.3V 或 5V 接口电源运行，也可以通过低至 2.4V 的备份电路运行。

输出电流最大可达 6A，由每相各为 3A 的两相电源持续提供，能够以异相运行，显著降低脉冲电流噪声。

TPSM82480 可在超轻负载时自动进入省电模式，并能保持高效率。其中包含自动增加/减少相位功能，具体使用一个相位还是两个相位视实际负载情况而定。可通过“模式”功能关闭省电模式。

器件可提供电源正常信号和可调软启动。此外，该器件还具有温度正常信号指示内部温度过高。通过 VSEL 引脚可将输出电压更改为预选值。TPSM82480 能够以 100% 的占空比模式运行。

器件信息(1)

<table>
<thead>
<tr>
<th>器件型号</th>
<th>封装</th>
<th>封装尺寸（标称值）</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPSM82480MOP</td>
<td>QFM (24)</td>
<td>7.90 x 3.60 x 1.55mm</td>
</tr>
</tbody>
</table>

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用电路原理图

效率与输出电流间的关系
目录

1 选项................................................................. 1
2 应用............................................................. 1
3 说明............................................................... 1
4 修订历史记录 ................................................ 2
5 Pin Configuration and Functions ..................... 3
6 Specifications................................................ 4
   6.1 Absolute Maximum Ratings ...................... 4
   6.2 ESD Ratings ............................................ 4
   6.3 Recommended Operating Conditions .......... 4
   6.4 Thermal Information ................................. 4
   6.5 Electrical Characteristics ....................... 5
   6.6 Typical Characteristics ............................ 7
7 Detailed Description ..................................... 8
   7.1 Overview ............................................... 8
   7.2 Functional Block Diagram ....................... 8
   7.3 Feature Description ................................. 9
   7.4 Device Functional Modes ....................... 10
8 Application and Implementation ................... 12
   8.1 Application Information ......................... 12
   8.2 Typical Application ............................... 12
   8.3 System Examples ................................ 22
9 Power Supply Recommendations .................... 22
10 Layout......................................................... 23
   10.1 Layout Guidelines ................................. 23
   10.2 Layout Example ..................................... 23
11 器件和文档支持 ........................................ 24
   11.1 文档支持 .......................................... 24
   11.2 接收文档更新通知 .............................. 24
   11.3 社区资源 .......................................... 24
   11.4 商标 ................................................. 24
   11.5 静电放电警告 .................................... 24
   11.6 Glossary .............................................. 24
12 机械、封装和可订购信息 ......................... 24

4 修订历史记录

Changes from Original (July 2017) to Revision A  Page

• 已更改 将数据表状态从“预告信息”更改成了“生产数据”。 ..................................................... 1
5 Pin Configuration and Functions

MOP Package
24-Pin QFM

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>VOUT1</td>
<td>1</td>
<td>Output Voltage Node Phase 1 (master), Must be connect with VOUT2</td>
</tr>
<tr>
<td>PGND1</td>
<td>2, 3, 20, 21</td>
<td>Power Ground Phase 1 (master)</td>
</tr>
<tr>
<td>VIN1</td>
<td>4, 24</td>
<td>Supply voltage Phase 1 (master)</td>
</tr>
<tr>
<td>EN</td>
<td>5</td>
<td>Enable input (High=Enabled, Low = Disabled)</td>
</tr>
<tr>
<td>PG</td>
<td>6</td>
<td>Power Good (open drain, requires pull-up resistor)</td>
</tr>
<tr>
<td>VSEL</td>
<td>7</td>
<td>Output Voltage Select (High = VOUT2, Low=VOUT1) , VOUT1 &lt; VOUT2</td>
</tr>
<tr>
<td>TG</td>
<td>8</td>
<td>Thermal Good (open drain, requires pull-up resistor)</td>
</tr>
<tr>
<td>MODE</td>
<td>9</td>
<td>Operating mode selection (Low=Automatic PWM/PSM, High = Forced PWM)</td>
</tr>
<tr>
<td>VIN2</td>
<td>10, 23</td>
<td>Supply voltage Phase 2</td>
</tr>
<tr>
<td>PGND2</td>
<td>11, 12, 14, 22</td>
<td>Power Ground Phase 2</td>
</tr>
<tr>
<td>VOUT2</td>
<td>13</td>
<td>Output Voltage Node Phase 2, Must be connected with VOUT1</td>
</tr>
<tr>
<td>SS/TR</td>
<td>15</td>
<td>Soft-Start / Tracking. An external capacitor connected to this pin sets the output voltage rise time.</td>
</tr>
<tr>
<td>AGND</td>
<td>16</td>
<td>Analog Ground</td>
</tr>
<tr>
<td>FB</td>
<td>17</td>
<td>Output voltage feedback for the adjustable version. Connect resistive voltage divider to this pin.</td>
</tr>
<tr>
<td>RS</td>
<td>18</td>
<td>Resistor Select. Connect resistor that sets the level for the second output voltage here (activated by VSEL= High)</td>
</tr>
<tr>
<td>VO</td>
<td>19</td>
<td>VOUT detection (connect to VOUT, output discharge is internally connected to this pin)</td>
</tr>
</tbody>
</table>
6 Specifications

6.1 Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Pin Voltage Range</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN</td>
<td>-0.3</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>EN, VSEL, MODE, SS/TR, PG, TG</td>
<td>-0.3</td>
<td>6</td>
<td>V</td>
</tr>
<tr>
<td>FB, RS</td>
<td>-0.3</td>
<td>3</td>
<td>V</td>
</tr>
<tr>
<td>Power Good / Thermal Good Sink Current</td>
<td>PG, TG</td>
<td>10</td>
<td>mA</td>
</tr>
<tr>
<td>Operating Junction Temperature Range, $T_J$</td>
<td>-40</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature Range, $T_{stg}$</td>
<td>-65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) All voltages are with respect to network ground terminal.

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>Electrostatic discharge</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins</td>
<td>±1000</td>
<td>V</td>
</tr>
<tr>
<td>Charged device model (CDM), per JEDEC specification JESD22-C101, all pins</td>
<td>±500</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

| Supply Voltage Range, $V_{IN}$ | MIN | TYP | MAX | UNIT |
| Output Voltage Range, $V_{OUT}$ | 2.4 | 5.5 | V   |
| Maximum Output Current, $I_{OUT}$ | 0.6 | 5.5 | A   |
| Operating junction temperature, $T_J$ | -40 | 125 | °C  |

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC</th>
<th>TPSM82480</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{JA}$</td>
<td>Junction-to-ambient thermal resistance</td>
</tr>
<tr>
<td>$R_{JC(top)}$</td>
<td>Junction-to-case (top) thermal resistance</td>
</tr>
<tr>
<td>$R_{JB}$</td>
<td>Junction-to-board thermal resistance</td>
</tr>
<tr>
<td>$\psi_{JT}$</td>
<td>Junction-to-top characterization parameter</td>
</tr>
<tr>
<td>$\psi_{JB}$</td>
<td>Junction-to-board characterization parameter</td>
</tr>
<tr>
<td>$R_{JC(bot)}$</td>
<td>Junction-to-case (bottom) thermal resistance</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
### 6.5 Electrical Characteristics

over operating junction temperature range \((T_J = -40^\circ C \text{ to } 125^\circ C)\) and \(V_{IN} = 2.4 \text{ V to } 5.5 \text{ V}\). Typical values at \(V_{IN} = 3.6 \text{ V}\) and \(T_J = 25^\circ C\) (unless otherwise noted).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SUPPLY</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{IN}) Input Voltage Range</td>
<td>(V_{IN}) rising</td>
<td>2.6</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(V_{IN}) falling</td>
<td>2.4</td>
<td>5.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_Q) Operating Quiescent Current</td>
<td>(EN = \text{High}, V_{IN} \geq 3 \text{ V}, I_{OUT} = 0 \text{ mA}, \text{device not switching}), (T_J = -40^\circ C \text{ to } +85^\circ C)</td>
<td>23</td>
<td>38</td>
<td>(\mu A)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>100% Mode operation</td>
<td>3.5</td>
<td>6.5</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>(I_{SD}) Shutdown Current</td>
<td>(EN = \text{Low} (\leq 0.3 \text{ V}), T_J = -40^\circ C \text{ to } +85^\circ C)</td>
<td>0.5</td>
<td>18.5</td>
<td>(\mu A)</td>
<td></td>
</tr>
<tr>
<td>(V_{UVLO}) Undervoltage Lockout Threshold</td>
<td>Falling Input Voltage</td>
<td>2.2</td>
<td>2.3</td>
<td>2.4</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Hysteresis</td>
<td>200</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>(T_{SD}) Thermal Shutdown Temperature</td>
<td>PWM Mode, Rising Junction Temperature</td>
<td>160</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td>Thermal Shutdown Hysteresis</td>
<td>10</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>CONTROL (EN, VSEL, MODE, SS/TR, PG, TG)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_H) Input Threshold Voltage (EN, VSEL, MODE)</td>
<td>to ensure High Level</td>
<td>1.2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>(V_L) Input Threshold Voltage (EN, VSEL, MODE)</td>
<td>to ensure Low Level</td>
<td></td>
<td>0.4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{LKG(EN)}) Input Leakage Current (EN)</td>
<td>(EN = V_{IN}) or GND</td>
<td>10</td>
<td>200</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>(I_{LKG(MODE)}) Input Leakage Current (MODE, VSEL)</td>
<td></td>
<td>10</td>
<td>200</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>(I_{SS/TR}) SS/TR pin source current</td>
<td></td>
<td>4.7</td>
<td>5.25</td>
<td>5.8</td>
<td>(\mu A)</td>
</tr>
<tr>
<td>(V_{TH(TG)}) Thermal Good Threshold Temperature</td>
<td>PWM Mode</td>
<td>120</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td>Thermal Good Hysteresis</td>
<td>PWM Mode</td>
<td>10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{TH(PG)}) Power Good Threshold Voltage</td>
<td>Rising (%(V_{OUT}))</td>
<td>93%</td>
<td>96%</td>
<td>99%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Falling (%(V_{OUT}))</td>
<td>89%</td>
<td>92%</td>
<td>95%</td>
<td></td>
</tr>
<tr>
<td>(V_{L(PG)}) Output Low Threshold (PG, TG)</td>
<td>(I_{PG} = -2 \text{ mA})</td>
<td></td>
<td>0.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>(I_{LKG(PG)}) Input Leakage Current (PG)</td>
<td></td>
<td>2</td>
<td>700</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>(I_{LKG(TG)}) Input Leakage Current (TG)</td>
<td></td>
<td>2</td>
<td>100</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>(I_{SS}) Internal Soft-Start Time</td>
<td>SS/TR = (V_{IN}) or floating</td>
<td>80</td>
<td></td>
<td></td>
<td>(\mu s)</td>
</tr>
<tr>
<td>(I_{DELAY}) Time from EN rising until start switching</td>
<td></td>
<td>100</td>
<td>200</td>
<td>400</td>
<td>(\mu s)</td>
</tr>
<tr>
<td><strong>POWER SWITCH</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(R_{DS(ON)}) High-Side MOSFET ON-Resistance</td>
<td>(V_{IN} \geq 3 \text{ V})</td>
<td>Phase1</td>
<td>36</td>
<td>98</td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Phase2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Low-Side MOSFET ON-Resistance</td>
<td>Phase1</td>
<td>29</td>
<td>72</td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Phase2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(I_{LIM}) High-Side MOSFET Current Limit</td>
<td>per phase</td>
<td>4.2</td>
<td>5.0</td>
<td>5.8</td>
<td>A</td>
</tr>
</tbody>
</table>
Electrical Characteristics (continued)

over operating junction temperature range \( T_J = -40^\circ C \) to 125°C and \( V_{IN} = 2.4 \) V to 5.5 V. Typical values at \( V_{IN} = 3.6 \) V and \( T_J = 25^\circ C \) (unless otherwise noted).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{REF} )</td>
<td>Internal Reference Voltage</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( I_{LKG(FB)} )</td>
<td>Input Leakage Current (FB)</td>
<td></td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>( I_{LKG(RS)} )</td>
<td>Input Leakage Current (RS)</td>
<td></td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>( R_{RS} )</td>
<td>Internal resistance (RS to GND)</td>
<td></td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>( V_{OUT} )</td>
<td>Output Voltage Range ( V_{IN} \geq V_{OUT} )</td>
<td>0.6</td>
<td></td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>( V_{OUT} )</td>
<td>Feedback Voltage Accuracy ( PWM ) Mode, ( V_{IN} \geq V_{OUT} + 1 )</td>
<td></td>
<td>-1%</td>
<td>1%</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>-1.4%</td>
<td>1.3%</td>
<td>%</td>
</tr>
<tr>
<td>( V_{OUT} )</td>
<td>Feedback Voltage Accuracy ( Power ) Save Mode, ( L = 0.47 ) μH, ( C_{OUT} = 4 \times 22 ) μF(1)</td>
<td></td>
<td>-1.4%</td>
<td>2.5%</td>
<td>%</td>
</tr>
<tr>
<td>( V_{OUT} )</td>
<td>Output Discharge Current(2) ( EN ) = Low, ( V_{OUT} = 2.5 ) V</td>
<td></td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Load Regulation</td>
<td>( V_{OUT} = 1.8 ) V, PWM mode operation</td>
<td>120</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Line Regulation</td>
<td>2.6 V \leq V_{IN} \leq 5.5 V, ( V_{OUT} = 1.8 ) V, ( I_{OUT} = 6 ) A, PWM mode operation</td>
<td>0.02</td>
<td></td>
<td></td>
<td>%/V</td>
</tr>
</tbody>
</table>

(1) The output voltage accuracy in Power Save Mode can be improved by increasing the output capacitor value, reducing the output voltage ripple.

(2) For detailed information on output discharge see Active Output Discharge.
6.6 Typical Characteristics

图 2. Quiescent Current

图 3. Shutdown Current

图 4. High-Side Switch Resistance

图 5. Low-Side Switch Resistance
7 Detailed Description

7.1 Overview

The TPSM82480 is a high efficiency synchronous switched mode step-down converter module based on a 2-phase peak current control topology. It is designed for smallest solution size low-profile applications, converting a 2.4 V to 5.5 V input voltage into a lower 0.6 V to 5.5 V output voltage. While an outer voltage loop sets the regulation threshold for the inner current loop, based on the actual $V_{OUT}$ level, the inner current loop regulates to the actual peak inductor current level for every switching cycle. The regulation network is internally compensated. While the ON-time is determined by duty cycle, inductance and cycle peak current, the switching frequency of typically 2.2 MHz is set by a predicted OFF-time. The device features a Power Save Mode (PSM) to keep the conversion efficiency high over the whole load current range.

The TPSM82480 is a 2-phase converter, sharing the load among the phases. Identical in construction, the second phase control is connected with an adaptive delay to the first phase. Both the phases use the same regulation threshold and cycle-by-cycle peak current setpoint. This ensures a phase-shifted as well as current-balanced operation. Using the advantages of the 2-phase topology, a 6-A continuous output current is provided with high performance and as small as possible solution size.

7.2 Functional Block Diagram
7.3 Feature Description

7.3.1 Enable / Shutdown (EN)
The device starts operation, when VIN is present and enable (EN) is set High. Since the boundary EN thresholds are specified with 1.2 V for rising and 0.4 V for falling voltages, the typical values are 0.85 V (rising) and 0.65 V (falling). The device is disabled by pulling EN Low. Leaving the EN pin floating is not recommended.

7.3.2 Soft Start (SS), Pre-biased Output
The internal soft start circuit controls the output voltage slope during startup. This avoids excessive inrush current and provides an adjustable controlled output-voltage rise time. The soft start also prevents unwanted voltage drop from high impedance power sources or batteries.

When EN is set to start device operation, the device starts switching after a delay of typically 200 µs and VOUT rises with a slope, controlled by the external capacitor which is connected to the SS/TR pin (soft start). Leaving the SS/TR pin floating or connecting to VIN provides internally set fastest startup with a soft start slope of about 80us. See Application Curves for typical startup operation.

The device can start into a pre-biased output. In this case, the device starts switching, only when the internal set point for VOUT increases above the pre-biased voltage level.

7.3.3 Tracking (TR)
The device tracks an external voltage applied to the SS/TR pin. The FB voltage tracks the external voltage as long as it is below about 0.6V. Above 0.6V the device goes to normal operation. If the voltage at the SS/TR pin decreases below about 0.6V, the FB voltage tracks again this voltage. See Tracking for further details.

7.3.4 Output Voltage Select (VSEL)
A resistive divider (VOUT to FB to AGND) sets the output voltage of the TPSM82480. Providing a logic High level at the VSEL pin, the RS pin is pulled to ground, so that a resistor, between FB and RS pins is connected in parallel to the lower resistor of the divider. This sets a different higher output voltage and can be used for dynamic voltage scaling (see Setting \( V_{OUT2} \) Using the VSEL Feature).

If the VSEL pin is set Low, the device connects an internal pull down resistor to the pin, keeping the internal logic level Low, even if the pin is floating afterwards. The device disconnects the resistor, if the pin is set to High.

7.3.5 Forced PWM (MODE)
To avoid Power Save Mode (PSM) Operation, the device can be forced to PWM mode operation by pulling the MODE pin High. In this case the device operates continuously with it's nominal switching frequency and the minimum peak current can go as low as -500 mA.

If the MODE pin is set Low, the device connects an internal pull down resistor to keep the internal logic level Low, even if the pin is floating afterwards. The device disconnects the resistor, if the pin is set to High.

7.3.6 Power Good (PG)
The TPSM82480 has a built in power good function. The PG pin goes High, when the output voltage has reached its nominal value. Otherwise, including when disabled, in UVLO or thermal shutdown, PG is Low. The PG pin is an open drain output that requires a pull-up resistor and can sink typically 2mA. If not used, the PG pin can be left floating or grounded.

7.3.7 Thermal Good (TG)
As long as the junction temperature of the TPSM82480 is below the thermal good temperature of typically 120°C, the logic level at the TG pin is High. If the junction temperature exceeds that temperature, the TG pin goes Low. This can be used for the system to take action preventing excessive heating or even thermal shutdown. The TG pin is an open drain output that requires a pull-up resistor and can sink typically 2mA. If not used, the TG pin can be left floating or grounded.
Feature Description (接下页)

7.3.8 Active Output Discharge

The VO pin, connected to the output voltage, provides an active discharge path when the device is switched off by setting EN Low or UVLO event. In case of being activated, this discharge circuit sinks typically 120mA for output voltages of typically 1 V and above. If \( V_{OUT} \) is lower, the active current sink enters linear operation mode and the discharge current decreases.

7.3.9 Undervoltage Lockout (UVLO)

The undervoltage lockout prevents misoperation of the device, if the input voltage drops below the UVLO threshold which is set to typically 2.3 V. The converter starts operation again once the input voltage exceeds the threshold by a hysteresis of typically 200 mV.

7.3.10 Thermal Shutdown

The junction temperature (\( T_J \)) of the device is monitored by an internal temperature sensor. If \( T_J \) exceeds 160°C (typical), the device goes in thermal shutdown with a hysteresis of about 10°C. Both the power FETs are turned off and the PG pin goes Low. Once \( T_J \) has decreased enough, the device resumes normal operation with Soft Start.

7.4 Device Functional Modes

7.4.1 Pulse Width Modulation (PWM) Operation

The TPSM82480 is based on a predictive OFF-time peak current control topology, operating with PWM in continuous conduction mode for current loads larger than half the ripple current. The switching frequency is typically 2.2MHz. Both the master and follower phase regulate to the same \( V_{OUT} \) level, each with a separate current loop, using the same peak current set point, cycle by cycle. This provides excellent peak current balancing, independent of inductor dc resistance matching. Since the follower phase operates with an adaptive delay to the master phase, phase shifted operation is always obtained. If the load current decreases, the device runs with the master phase only (see Phase Add/Shed and Current Balancing).

PWM only mode can be forced by pulling MODE pin High. If MODE is set Low, the device features an automatic transition into Power Save Mode, entered at light loads, running in discontinuous conduction mode (DCM).

7.4.2 Power Save Mode (PSM) Operation

As the load current decreases to half the ripple current, the converter enters Power Save Mode operation. During PSM, the converter operates with reduced switching frequency maintaining high conversion efficiency. Power Save Mode is based on an adaptive peak current target, to keep output voltage ripple low. Since each pulse shifts \( V_{OUT} \) up, a pause time happens until \( V_{OUT} \) trips the internal \( V_{OUT\_Low} \) threshold again and the next pulse takes place.

The switching frequency in PSM (one phase operation) calculates as:

\[
 f_{SW(PSM)} = \frac{2 \cdot I_{OUT} \cdot V_{OUT} \cdot (V_{IN} - V_{OUT})}{L \cdot I_{PEAK} \cdot V_{IN}}
\]  

(1)

7.4.3 Minimum Duty Cycle and 100% Mode Operation

The minimum on-time, which is typically 70ns, normally determines a limit on the minimum operating duty cycle. The calculation is:

\[
 DC_{min} = 70ns \cdot 100% \cdot f_{SW}[Hz]
\]  

(2)

However, a frequency foldback lowers the switching frequency depending on the duty cycle and ensures proper regulation for every duty cycle.
Device Functional Modes (接下页)

There is no limit towards maximum duty cycle. When the input voltage becomes close to the output voltage, the
device enters automatically 100% duty cycle mode and both high-side FETs switch on as long as VOUT remains
below the regulation setpoint. In this case, the voltage drop across the high-side FETs and the inductors
determines the output voltage level. An estimate for the minimum input voltage to maintain output voltage
regulation is:

\[
V_{\text{IN(min)}} = V_{\text{OUT(min)}} + I_{\text{OUT}} \left( \frac{R_{\text{DS(ON)}}}{2} + 13.5 \text{m}\Omega \right)
\]  

(3)

Where the maximum DCR of the inductors is 27mΩ.

In 100% duty cycle mode, the low-side FETs are switched off. The typical quiescent current in 100% mode is
3.5 mA.

7.4.4 Phase Shifted Operation

Using an inherent benefit of the two-phase conversion, the two phases of TPSM82480 run out of phase. For
every switching cycle, the second phase is not allowed to turn on its high-side FET until the master phase has
reached its peak current value. This limits the input RMS current and corresponding switching noise.

7.4.5 Phase Add/Shed and Current Balancing

When the load current is below the internal threshold, only the master phase operates. The second phase
activates, if the load current exceeds the threshold of typically 1.7 A. The second phase powers off with a
hysteresis of about 0.5 A, when the load current decreases.

7.4.6 Current Limit and Short Circuit Protection

Each phase has a separate integrated peak current limit. The dc values are specified in the Electrical
Characteristics. While its minimum value limits the output current of the phase, the maximum number gives the
current that must be considered to flow in some operating case (e.g. overload). At the peak current limit, the
device provides its maximum output current.

However, if the current limit situation remains for 512 consecutive switching cycles, the peak current folds back to
about 1/3 of the regular limit. This limits the output power for over current and short circuit events. The foldback
current limit is released to the normal one only if the load current has decreased as far as needed to undercut
the (foldback) peak current limit.
8 Application and Implementation

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information
The TPSM82480 is a switched mode step-down converter module, able to convert a 2.4-V to 5.5-V input voltage into a lower 0.6-V to 5.5-V output voltage, providing up to 6 A continuous output current. It needs a minimum amount of external components. Apart from the output and input capacitors, additional resistors or capacitors are only needed to enable features like soft start, adjustable and selectable output voltage as well as Power Good and/or Thermal Good.

8.2 Typical Application

![Diagram of TPSM82480](image)

图 7. Typical Application using TPSM82480 for a 6A Point-Of-Load Power Supply

8.2.1 Design Requirements
The following design guideline provides a range for the component selection to operate within the recommended operating conditions. 表 1 shows the components selection that was used for the measurements shown in the Application Curves.
Typical Application

### Table 1. List of Components

<table>
<thead>
<tr>
<th>REFERENCE</th>
<th>DESCRIPTION</th>
<th>MANUFACTURER</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Module</td>
<td>5.5-V, 6-A step-down module with integrated inductor</td>
<td>TPSM82480MOP, Texas Instruments</td>
</tr>
<tr>
<td>C1, C2</td>
<td>2x22-µF, 10-V, ceramic, 0603, X5R</td>
<td>GRM188R61A226ME15#, muRata</td>
</tr>
<tr>
<td>C3, C4, C7, C8</td>
<td>4x22-µF, 25-V, ceramic, 0805, X5R</td>
<td>GRM21BR61E226ME44L, muRata</td>
</tr>
<tr>
<td>C5</td>
<td>3300-pF, 10-V, ceramic, 0402</td>
<td>Standard</td>
</tr>
<tr>
<td>R1, R2, R3</td>
<td>Depending on Vout1 and Vout2, chip, 0402, 0.1%</td>
<td>Standard</td>
</tr>
<tr>
<td>R4, R5</td>
<td>470-kΩ, chip, 0603, 1/16-W, 1%</td>
<td>Standard</td>
</tr>
</tbody>
</table>

8.2.2 Detailed Design Procedure

#### 8.2.2.1 Setting the Adjustable Output Voltage

While the device regulates the FB voltage to 0.6V, the output voltage is specified from 0.6 to 5.5 V. A resistive divider (from VOUT to FB to AGND) sets the actual output voltage of the TPSM82480. 公式 4 and 公式 5 are calculating the values of the resistors. First, determining the current through the resistive divider leads to the total resistance \((R_1 + R_2)\). A minimum divider current of about 5 µA is recommended and can be higher if needed.

\[
R_1 + R_2 = \frac{V_{OUT}}{I_{FB}} \tag{4}
\]

\[
R_2 = \frac{V_{REF}}{V_{OUT}} (R_1 + R_2) \tag{5}
\]

#### 8.2.2.2 Setting \(V_{OUT2}\) Using the VSEL Feature

A \(V_{OUT}\) level, different as set with \(R_1\) and \(R_2\) (see Setting the Adjustable Output Voltage), can be forced by connecting \(R_3\) between FB and RS pins and pulling VSEL High. \(R_3\) is calculated using 公式 6.

\[
R_3 = \frac{V_1 \cdot R_1 \cdot R_2^2}{(V_2 - V_1) \cdot (R_1 \cdot R_2 + R_2^2)} \quad \text{for} \quad (V_2 > V_1) \tag{6}
\]

where:

- \(V_1\) is the lower level output voltage and
- \(V_2\) the higher level output voltage.

#### 8.2.2.3 Output Capacitor Selection

The recommended minimum output capacitance is 4 x 22 µF, that can be ceramic capacitors exclusively. A larger value of \(C_{OUT}\) might be needed for \(V_{OUT} \leq 1.8\) V, to improve transient response performance, as well as for \(V_{OUT} > 3.3\) V to compensate for voltage bias effects of the ceramic capacitors. The usage of an additional feed forward capacitor can help reducing amount of output capacitance that is needed to achieve a certain transient response target (see 表 3).

The TPSM82480 provides a wide output voltage range of 0.6 V to 5.5 V. While stability is a critical criteria for the output filter selection, the output capacitor value also determines transient response behavior, ripple and accuracy of \(V_{OUT}\). The internal compensation is designed for an output capacitance range from about 50 µF to 150 µF effectively. Since ceramic capacitors are used preferably, this translates into nominal values of 4 x 22 µF to 4 x 47 µF and mainly depends on the output voltage. The following values are recommended:
### Table 2. Recommended Output Capacitor Values (nominal)

<table>
<thead>
<tr>
<th>$V_{OUT}$</th>
<th>2x22µF</th>
<th>4x22µF</th>
<th>4x47µF</th>
<th>6x47µF</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OUT} \leq 1.0V$</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>$1.0V \leq V_{OUT} \leq 3.3V$</td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OUT} \geq 3.3V$</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
</tbody>
</table>

Beyond the recommendations in Table 2, other values can be chosen and might be suitable depending on VOUT and actual effective capacitance. In such case, stability needs to be checked within the actual environment.

Even if the output capacitance is sufficient for stability, a different value might be desirable to improve the transient response behavior. Table 3 can be used to determine capacitor values for specific transient response targets:

### Table 3. Recommended Output Capacitor Values (nominal)

<table>
<thead>
<tr>
<th>Output Voltage [V]</th>
<th>Load Step [A]</th>
<th>Output Capacitor Value(1)</th>
<th>Feedforward Capacitor(1)</th>
<th>Typical Transient Response Accuracy</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0 - 3</td>
<td>4 x 47µF</td>
<td>-</td>
<td>±50 ±5</td>
</tr>
<tr>
<td></td>
<td>3 - 6</td>
<td></td>
<td></td>
<td>50 5</td>
</tr>
<tr>
<td>1.0</td>
<td>0 - 3</td>
<td>4 x 22µF</td>
<td>36pF</td>
<td>±50 ±3</td>
</tr>
<tr>
<td></td>
<td>3 - 6</td>
<td></td>
<td></td>
<td>50 3</td>
</tr>
<tr>
<td>1.8</td>
<td>0 - 3</td>
<td>4 x 22µF</td>
<td>36pF</td>
<td>±50 ±2</td>
</tr>
<tr>
<td></td>
<td>3 - 6</td>
<td></td>
<td></td>
<td>50 2</td>
</tr>
<tr>
<td>2.5</td>
<td>0 - 3</td>
<td>4 x 22µF</td>
<td>36pF</td>
<td>±100 ±3</td>
</tr>
<tr>
<td></td>
<td>3 - 6</td>
<td></td>
<td></td>
<td>80 2.5</td>
</tr>
<tr>
<td>3.3</td>
<td>0 - 3</td>
<td>4 x 47µF</td>
<td>36pF</td>
<td></td>
</tr>
<tr>
<td></td>
<td>3 - 6</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) The values in the table are nominal values. The effective capacitance can differ significantly, depending on package size, voltage rating and dielectric material.

The architecture of the TPSM82480 allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, it is recommended to use X5R or X7R dielectrics. Using even higher values than demanded for stability and transient response has further advantages like smaller voltage ripple and tighter dc output accuracy in Power Save Mode.

#### 8.2.2.4 Input Capacitor Selection

The input current of a buck converter is pulsating. Therefore, a low ESR input capacitor is required to prevent large voltage transients at the source but still providing peak currents to the device. The recommended Capacitance value for most applications is 2 x 10 µF, split between the VIN1 and VIN2 inputs and placed as close as possible to these pins and PGND pins. If additional capacitance is needed, it can be added as bulk capacitance. To ensure proper operation, the effective capacitance at the VIN pins must not fall below 2 x 5 µF.

Low ESR multilayer ceramic capacitors are recommended for best filtering. Increasing with input voltage, the dc bias effect reduces the nominal capacitance value significantly. To decrease input ripple current further, larger values of input capacitors can be used.

#### 8.2.2.5 Soft Start Capacitor Selection

The soft start ramp time can be set externally connecting a capacitor between the SS/TR and AGND pins. The capacitor value $C_{SS}$ that is needed to get a specific rising time $\Delta t_{SS}$ calculates as:

$$C_{SS} = \Delta t_{SS} \cdot \frac{5.25 \mu A}{0.6V}$$ (7)
Since the device has an internal delay time $\Delta t_{\text{DELAY}}$ from EN=High to start switching, the overall startup time is longer as shown in 图 8.

![Diagram](image)

图 8. Soft Start $\Delta t_{\text{SS}}$

If very large output capacitances are used (e.g. $>4\times47\mu F$), the use of a soft start capacitor is mandatory to avoid current limit foldback during startup (see Current Limit and Short Circuit Protection).

### 8.2.2.6 Tracking

For values up to 0.6V, an external voltage, connected to the SS/TR pin, drives the voltage level at the FB pin. In doing so, the voltage at the FB pin is directly proportional to the voltage at the SS/TR pin.

When choosing the resistive divider proportion according to 公式 8, $V_{\text{OUT}}$ tracks $V_{\text{TR}}$ simultaneously.

$$\frac{R_1}{R_2} = \frac{R_3}{R_4}$$  (8)

![Diagram](image)

图 9. Voltage Tracking

Copyright © 2017, Texas Instruments Incorporated
Following the example of Setting the Adjustable Output Voltage with $V_{OUT} = 1.8\, \text{V}$, $R_1 = 240\, \text{k\Omega}$ and $R_2 = 120\, \text{k\Omega}$, \ref{eq:9} and \ref{eq:10} calculate $R_3$ and $R_4$, connected to the SS/TR pin. Different to the resistive divider at the FB pin, a larger current must be chosen, to avoid a tracking offset caused by the $5.25\, \mu\text{A}$ current that flows out of the SS/TR pin. Assuming a $250\, \mu\text{A}$ current, $R_4$ calculates as follows:

$$R_4 = \frac{0.6\, \text{V}}{250\, \mu\text{A}} = 2.4\, \text{k\Omega}$$

\hspace{1cm} \text{(9)}

$R_3$ calculates now rearranging \ref{eq:8}:

$$R_3 = R_4 \cdot \frac{R_1}{R_2} = 2.4\, \text{k\Omega} \cdot \frac{240\, \text{k\Omega}}{120\, \text{k\Omega}} = 4.8\, \text{k\Omega}$$

\hspace{1cm} \text{(10)}

However, the following limitations can influence the tracking accuracy:

- The upper limit of the SS/TR voltage that can be tracked is about $0.6\, \text{V}$. Since it is detected internally by a comparator, process variation and ramp speed can cause up to $\pm30\, \text{mV}$ different threshold.
- In case that the voltage at SS/TR ramps up immediately when $V_{IN}$ is supplied or EN is set High, the internal startup delay, $\Delta t_{\text{DELAY}}$, delays the ramp of $V_{OUT}$. The internal ramp starts after $\Delta t_{\text{DELAY}}$ at the voltage level, which is actually present at the SS/TR pin.
- The tracking down speed is limited by the RC time constant of the internal output discharge (always connected when tracking down) and the actual load with the output capacitance. Note: The device tracks down with the same behavior for MODE High (Forced PWM) and Low (Auto PSM).

### 8.2.2.7 Thermal Good

The Thermal Good pin provides an open drain output. The logic level is given by the pull up source which can be $V_{OUT}$. In this case, TG goes or stays Low, when the device switches off due to EN, UVLO or Thermal Shutdown.

When using an independent source for the pull up logic, the logic behavior at shutdown differs, because the TG pin internally goes high impedance. As before, TG goes Low when TG threshold is reached, but goes back High in the event of being switched off (e.g. Thermal Shutdown).
8.2.3 Application Curves

$V_{IN} = 3.6 \text{ V}, V_{OUT} = 1.8\text{V} \ (R1 / R2 = 240 \text{k} / 120 \text{k}), T_A = 25\text{°C}, \ (\text{unless otherwise noted})$

![Efficiency vs Output Current](image1)

*图 10. Efficiency vs Output Current*

![Efficiency vs Input Voltage](image2)

*图 11. Efficiency vs Input Voltage*

![Efficiency vs Output Current](image3)

*图 12. Efficiency vs Output Current*

![Efficiency vs Output Voltage](image4)

*图 13. Efficiency vs Output Voltage*

![Efficiency vs Output Current](image5)

*图 14. Efficiency vs Output Current*

![Efficiency vs Input Voltage](image6)

*图 15. Efficiency vs Input Voltage*
图 16. Output Voltage vs Output Current (Load Regulation)

图 17. Output Voltage vs Input Voltage (Line Regulation)

图 18. Maximum Output Current

图 19. Maximum Output Current

图 20. Switching Frequency vs Output Current

图 21. Switching Frequency vs Output Current
图 22. Startup into 3.3 Ω resistor

图 23. Startup into 0.3 Ω resistor

图 24. Output Discharge

图 25. Output Discharge

图 26. Typical Operation PWM

图 27. Typical Operation PSM

$V_{OUT} = 1.8$ V

$V_{OUT} = 2.5$ V  no load

$V_{OUT} = 1$ V  no load

$I_{OUT} = 50$ mA
28. Adding 2nd Phase

29. Shedding 2nd Phase

30. Load Transient Response (PSM-PWM), Load Step 0 to 3 A

$$C_{ff} = 36 \text{ pF (nom)}$$

31. Load Transient Response (PSM-PWM), Load Step 0 to 3 A

$$C_{ff} = 36 \text{ pF (nom)}$$

32. Load Transient Response (PWM-PWM), Load Step 3 to 6 A

33. Load Transient Response (PWM-PWM), Load Step 3 to 6 A
图 34. Load Transient Response (PWM-PWM),
Load Step 0 to 6 A

图 35. Current Limit Fold-Back at Overload

图 36. Maximum Ambient Temperature for $T_J=125^\circ\text{C}$
(TPSM82480 EVM)

图 37. Device Temperature (TPSM82480 EVM)
8.3 System Examples

This section provides typical schematics for commonly used output voltage values.

![Typical Schematic](image)

**图 38. A typical 1.8 V & 2.5 V, 6 A Power Supply**

**表 4. Resistive Divider Values for different Combinations of V_{OUT}**

<table>
<thead>
<tr>
<th>OUTPUT VOLTAGE</th>
<th>R1</th>
<th>R2</th>
<th>R3</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5V and 3.3V</td>
<td>380kΩ</td>
<td>120kΩ</td>
<td>285kΩ</td>
</tr>
<tr>
<td>1.2V and 1.8V</td>
<td>120kΩ</td>
<td>120kΩ</td>
<td>120kΩ</td>
</tr>
<tr>
<td>0.9V and 1.0V</td>
<td>60kΩ</td>
<td>120kΩ</td>
<td>360kΩ</td>
</tr>
</tbody>
</table>

9 Power Supply Recommendations

The TPSM82480 is designed to operate from a 2.4-V to 5.5-V input voltage supply. The input power supply's output current needs to be rated according to the output voltage and the output current of the power rail application.
10 Layout

10.1 Layout Guidelines

A recommended PCB layout for the TPSM82480 dual phase solution is shown below. It ensures best electrical and optimized thermal performance considering the following important topics:

- Both V\textsubscript{OUT1} and V\textsubscript{OUT2} must be connected to build a common VOUT structure.

- The input capacitors must be placed as close as possible to the appropriate pins of the device. This provides low resistive and inductive paths for the high di/dt input current. The input capacitance is split, as is the V\textsubscript{IN} connection, to avoid interference between the input lines.

- The V\textsubscript{OUT} regulation loop is closed with C\textsubscript{OUT} and its ground connection. To avoid PGND noise crosstalk, PGND is kept split for the regulation loop. If a ground layer or plane is used, a direct connection by vias, as shown, is recommended. Otherwise the connection of C\textsubscript{OUT} to GND must be short for good load regulation.

- The FB node is sensitive to dv/dt signals. Therefore the resistive divider should be placed close to the FB (and RS pin in case of using R\textsubscript{3}) pin, avoiding long trace distance.

For more detailed information about the actual EVM solution, see SLVUA16.

10.2 Layout Example

![TPSM82480 Board Layout](image-url)
11 器件和文档支持

11.1 文档支持

11.1.1 相关文档
如需相关文档，请参阅:
- 《TPSM82480EVM-BSR002 评估模块用户指南》，SLVUB57

11.2 接收文档更新通知
要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。请单击右上角的提醒我 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源
下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

**TI E2E™ 在线社区** TI 的工程师对工程师 (E2E) 社区。此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

**设计支持** TI 参考设计支持 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

11.4 商标
E2E是Texas Instruments的商标。所有其他商标均是其各自所有者的财产。

11.5 静电放电警告
这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 Glossary
SLYZ022 — Ti Glossary.
This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息
以下页面包含机械、封装和可订购信息。这些信息是写定器件的最新可用数据。数据如有变更，恕不另行通知，也不会对此文档进行修订。如欲获取此数据表的浏览器版本，请参阅左侧的导航。
 PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPSM82480MOPR</td>
<td>ACTIVE</td>
<td>QFM</td>
<td>MOP</td>
<td>24</td>
<td>3000</td>
<td>RoHS &amp; Green</td>
<td>Call TI</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>82480</td>
<td>Samples</td>
</tr>
<tr>
<td>TPSM82480MOPT</td>
<td>ACTIVE</td>
<td>QFM</td>
<td>MOP</td>
<td>24</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>Call TI</td>
<td>Level-2-260C-1 YEAR</td>
<td>-40 to 125</td>
<td>82480</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
obsolete: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp: The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is designed to be soldered to thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view.
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
重要声明和免责声明

TI 均以“原样”提供技术性及可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用TI产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的TI产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI对您使用所述资源的授权仅限于开发资源所涉及TI产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它TI或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI对此概不负责，并且您须赔偿由此对TI及其代表造成的损害。


邮寄地址：上海市浦东新区世纪大道1568号中建大厦32楼，邮政编码：200122
Copyright © 2019 德州仪器半导体技术（上海）有限公司