

CD74AC238 3 线至 8 线解码器/多路信号分离器

1 特性

- 交流类型的工作电压范围为 1.5V 至 5.5V，并在电源电压的 30% 时具有平衡的抗噪性能
- 双极 F、AS 和 S 的速度，同时功耗显著降低
- 专门为高速存储器解码器和数据传输系统设计
- 包含三个使能输入以简化级联和/或数据接收
- 平衡传播延迟
- $\pm 24mA$ 输出驱动电流
 - 扇出至 15 个 F 器件
- 防 SCR 闩锁 CMOS 工艺和电路设计
- ESD 保护超过 2kV (根据 MIL-STD-883 方法 3015)

2 说明

CD74AC238 解码器/多路信号分离器设计用于需要极短传播延迟时间的高性能存储器解码和数据路由应用。在高性能存储器系统中，可使用此解码器来尽可能地消除系统解码的影响。

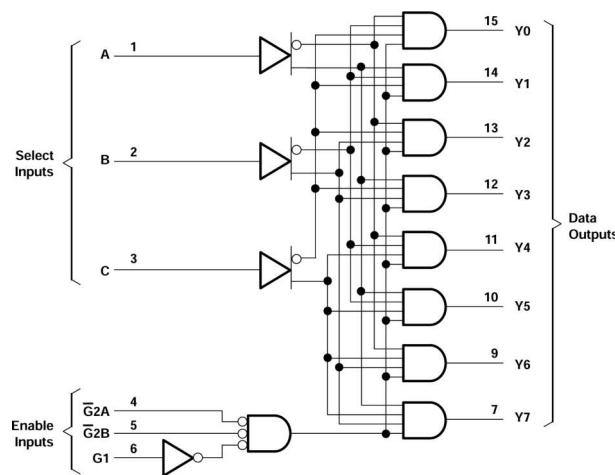
封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾	本体尺寸 ⁽³⁾
CD74AC238	M (SOIC, 20)	9.9mm x 6mm	9.9mm x 3.9mm

(1) 有关更多信息，请参阅 [节 10](#)。

(2) 封装尺寸 (长 x 宽) 为标称值，并包括引脚 (如适用)。

(3) 本体尺寸 (长 x 宽) 为标称值，不包括引脚。



本资源的原文使用英文撰写。为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

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3 Pin Configuration and Functions

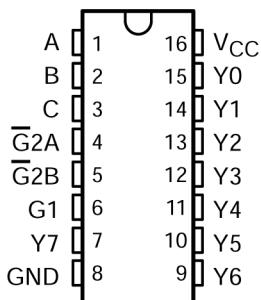


图 3-1. M Package (Top View)

表 3-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
A	1	I	Input A
B	2	I	Input B
C	3	I	Input C
G2A	4	I	Strobe Input 2A, active low
G2B	5	I	Strobe Input 2B, active low
G1	6	I	Strobe Input
Y7	7	O	Output 7
GND	8	G	Ground
Y6	9	O	Output 6
Y5	10	O	Output 5
Y4	11	O	Output 4
Y3	12	O	Output 3
Y2	13	O	Output 2
Y1	14	O	Output 1
Y0	15	O	Output 0
V _{cc}	16	P	Positive Supply
Thermal Pad ⁽²⁾		—	Thermal Pad

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

(2) BQB package only

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		- 0.5	6	V
I _{IK} ⁽²⁾	Input clamp current	(V _I < 0 V or V _I > V _{CC})		±20	mA
I _{OK} ⁽²⁾	Output clamp current	(V _O < 0 V or V _O > V _{CC})		±50	mA
I _O	Continuous output current	(V _O > 0 V or V _O < V _{CC})		±50	mA
	Continuous current through V _{CC} or GND			±200	mA
T _{stg}	Storage temperature range		- 65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

4.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)⁽¹⁾

		T _A = 25°C		-55°C to 125°C		-40°C to 85°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	1.5	5.5	1.5	5.5	1.5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 1.5 V		1.2		1.2		V
		V _{CC} = 3 V		2.1		2.1		
		V _{CC} = 5.5 V		3.85		3.85		
V _{IL}	Low-level input voltage	V _{CC} = 1.5 V		0.3		0.3		V
		V _{CC} = 3 V		0.9		0.9		
		V _{CC} = 5.5 v		1.65		1.65		
V _I	Input voltage		0	V _{CC}		0	V _{CC}	V
V _O	Output voltage		0	V _{CC}		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 4.5 V to 5.5 V		-24		-24		mA
I _{OL}	Low-level output current	V _{CC} = 4.5 V to 5.5 V		24		24		mA
$\Delta t / \Delta v$	Input transition rise or fall rate	V _{CC} = 1.5 V to 3 V		50		50		ns/V
		V _{CC} = 3.6 V to 5.5 V		20		20		

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

4.4 Thermal Information

THERMAL METRIC ⁽¹⁾				CD74AC238	UNIT
				M	
				16 PINS	
$R_{\theta JA}$ Junction-to-ambient thermal resistance				106.6	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ C$		$-55^\circ C \text{ to } 125^\circ C$		$-40^\circ C \text{ to } 85^\circ C$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL}	$I_{OH} = -50 \mu A$	1.5 V	1.4	1.4	1.4	1.4	1.4	V
			3 V	2.9	2.9	2.9	2.9	2.9	
			4.5 V	4.4	4.4	4.4	4.4	4.4	
		$I_{OH} = -4 \text{ mA}$	3 V	2.58	2.4	2.48			
		$I_{OH} = -24 \text{ mA}$	4.5 V	3.94	3.7	3.8			
		$I_{OH} = -50 \text{ mA}^{(1)}$	5.5 V		3.85				
V_{OL}	$V_I = V_{IH}$ or V_{IL}	$I_{OL} = 50 \mu A$	1.5 V	0.1	0.1	0.1	0.1	0.1	V
			3 V	0.1	0.1	0.1	0.1	0.1	
			4.5 V	0.1	0.1	0.1	0.1	0.1	
		$I_{OL} = 12 \text{ mA}$	3 V	0.36	0.5	0.44			
		$I_{OL} = 24 \text{ mA}$	4.5 V	0.36	0.5	0.44			
		$I_{OL} = 50 \text{ mA}^{(1)}$	5.5 V		1.65				
I_I	$V_I = V_{CC}$ or GND		5.5 V	± 0.1	± 1	± 1	± 1	μA	
I_{CC}	$V_I = V_{CC}$ or GND,	$I_O = 0$	5.5 V		8	160	80	μA	
C_i					10	10	10	pF	

(1) Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum $50-\Omega$ transmission-line drive capability at $85^\circ C$ and $75-\Omega$ transmission-line drive capability at $125^\circ C$.

4.6 Switching Characteristics, $V_{CC} = 1.5 \text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 1.5 \text{ V}$, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$-55^\circ C \text{ to } 125^\circ C$		$-40^\circ C \text{ to } 85^\circ C$		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	A, B, C	Any Y		187		170	ns
t_{PHL}				187		170	
t_{PLH}	G1	Any Y		208		189	ns
t_{PHL}				208		189	
t_{PLH}	G2A, G2B	Any Y		149		135	ns
t_{PHL}				149		135	

4.7 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, $C_L = 50\text{ pF}$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	A, B, C	Any Y	5.3	21	5.4	19.1	ns
t_{PHL}			5.3	21	5.4	19.1	
t_{PLH}	G1	Any Y	5.8	23.2	6	21.1	ns
t_{PHL}			5.8	23.2	6	21.1	
t_{PLH}	$\overline{G}2A, \overline{G}2B$	Any Y	4.2	16.7	4.3	15.2	ns
t_{PHL}			4.2	16.7	4.3	15.2	

4.8 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$, $C_L = 50\text{ pF}$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

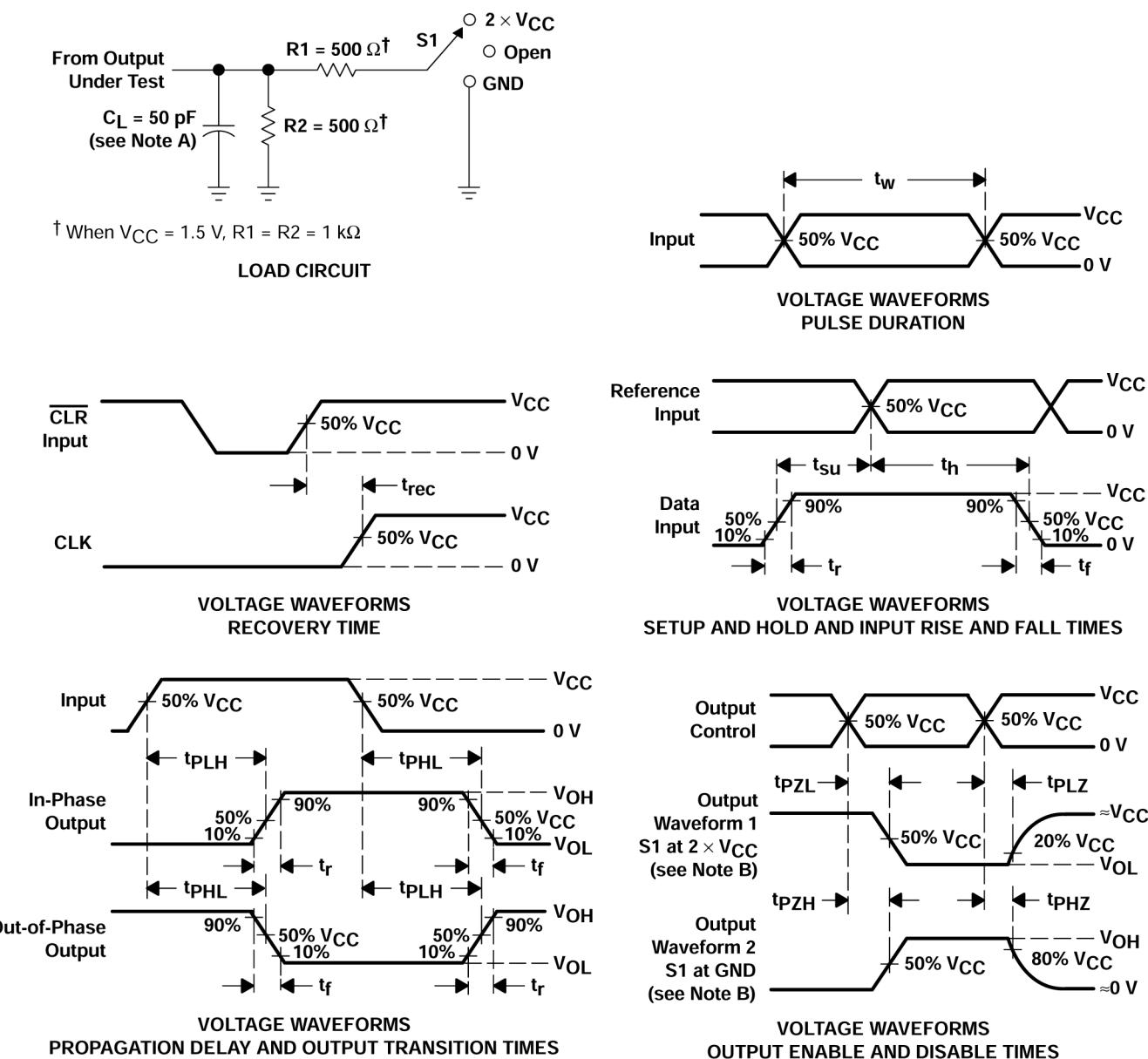
PARAMETER	FROM (INPUT)	TO (OUTPUT)	-55°C to 125°C		-40°C to 85°C		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	A, B, C	Any Y	3.8	15	3.9	13.6	ns
t_{PHL}			3.8	15	3.9	13.6	
t_{PLH}	G1	Any Y	4.2	16.6	4.3	15.1	ns
t_{PHL}			4.2	16.6	4.3	15.1	
t_{PLH}	$\overline{G}2A, \overline{G}2B$	Any Y	3	11.9	3.1	10.7	ns
t_{PHL}			3	11.9	3.1	10.7	

4.9 Operating Characteristics

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TYP	UNIT
C_{pd}	Power dissipation capacitance	110	pF

5 Parameter Measurement Information



- A. C_L includes probe and test-fixture capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω , t_r = 3 ns, t_f = 3 ns. Phase relationships between waveforms are arbitrary.
- D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
- E. The outputs are measured one at a time with one input transition per measurement.
- F. t_{PLH} and t_{PHL} are the same as t_{pd}.
- G. t_{PZL} and t_{PZH} are the same as t_{en}.
- H. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- I. All parameters and waveforms are not applicable to all devices.

图 5-1. Load Circuit and Voltage Waveforms

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

6 Detailed Description

6.1 Overview

When employed with high-speed memories utilizing a fast enable circuit, the delay times of these decoders and the enable time of the memory usually are less than the typical access time of the memory. This means that the effective system delay introduced by the decoders is negligible.

The conditions at the binary-select inputs and the three enable inputs select one of eight output lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications (see Application Information).

6.2 Functional Block Diagram

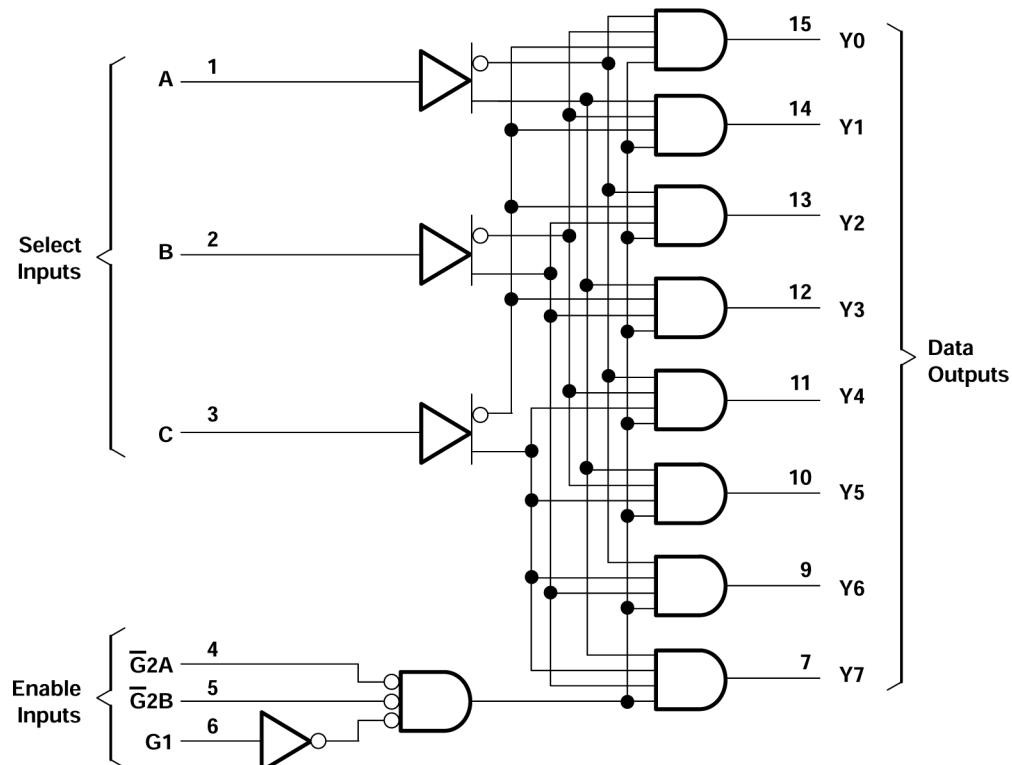


图 6-1. Logic Diagram (Positive Logic)

6.3 Device Functional Modes

表 6-1. Function Table

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	$\overline{G2A}$	$\overline{G2B}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	L	L	L	L	L	L	L	L
X	X	H	X	X	X	L	L	L	L	L	L	L	L
L	X	X	X	X	X	L	L	L	L	L	L	L	L
H	L	L	L	L	L	H	L	L	L	L	L	L	L
H	L	L	L	L	H	L	L	H	L	L	L	L	L
H	L	L	L	H	H	L	L	L	H	L	L	L	L
H	L	L	H	L	L	L	L	L	L	H	L	L	L

表 6-1. Function Table (续)

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
G1	ȐG2A	ȐG2B	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
H	L	L	H	L	H	L	L	L	L	L	H	L	L
H	L	L	H	H	L	L	L	L	L	L	L	H	L
H	L	L	H	H	H	L	L	L	L	L	L	L	H

7 Application Information

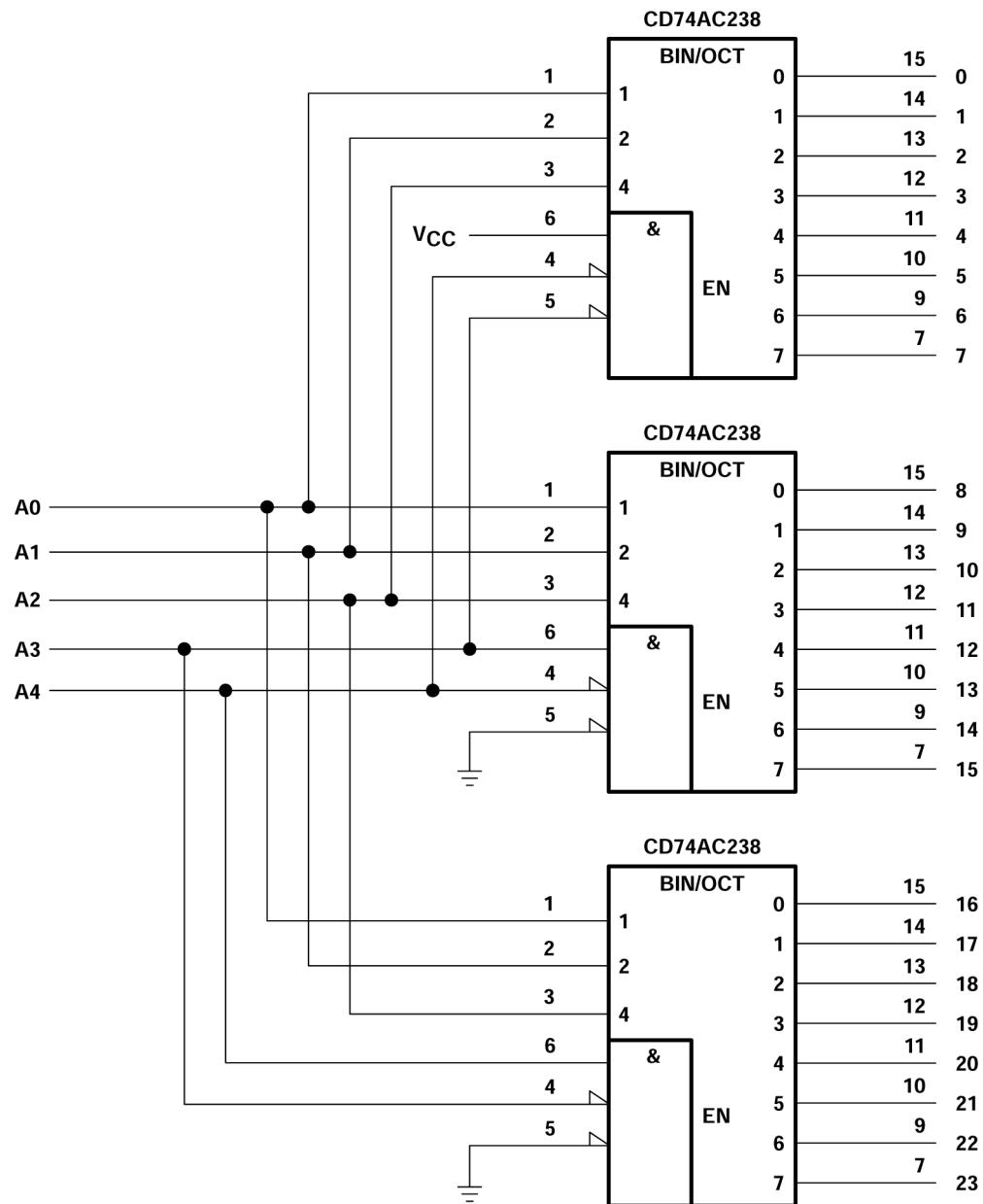


图 7-1. 24-Bit Decoding Scheme

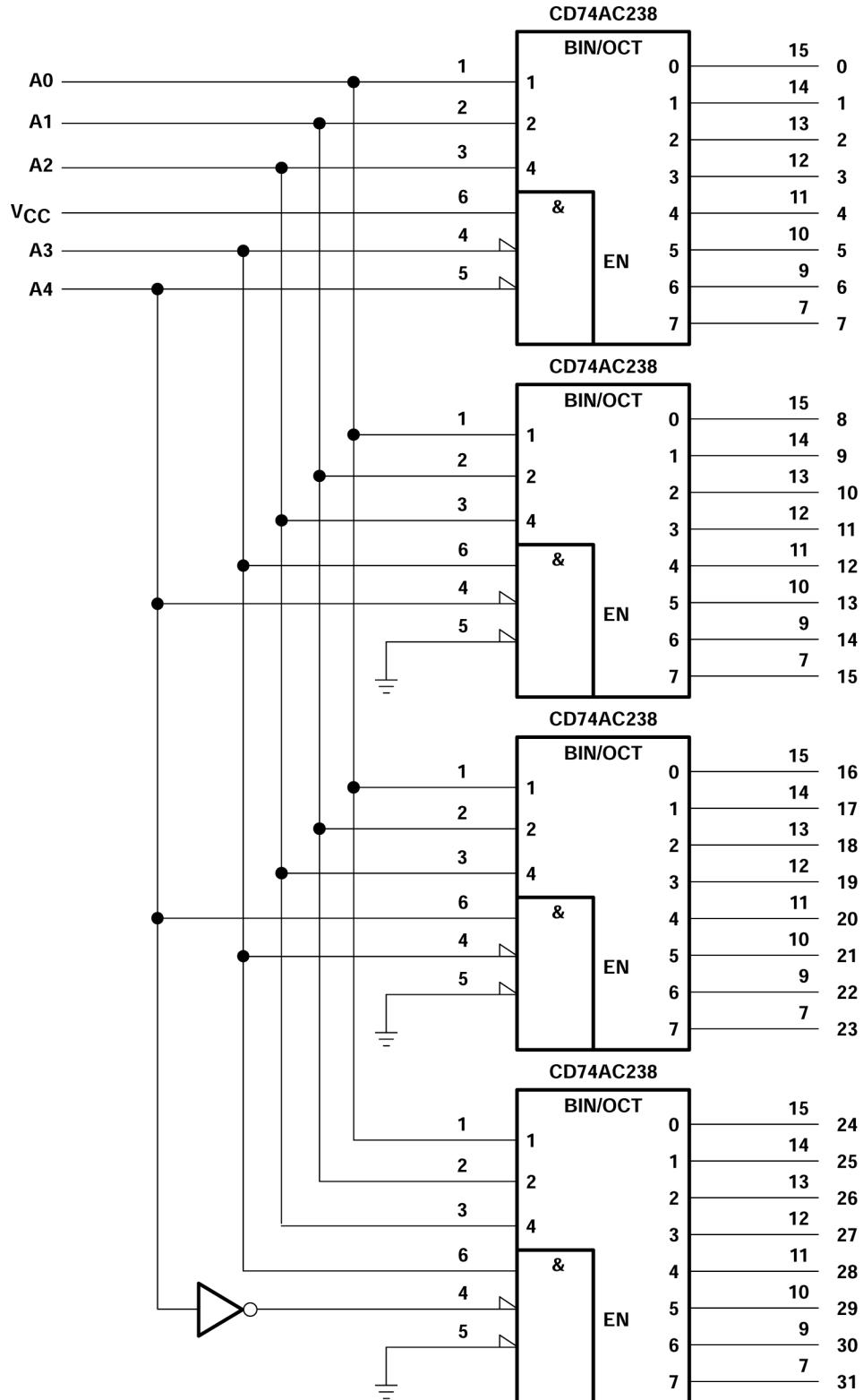


图 7-2. 32-Bit Decoding Scheme

7.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A $0.1 \mu F$ capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The $0.1 \mu F$ and $1 \mu F$ capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

7.2 Layout

7.2.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

7.2.2 Layout Example

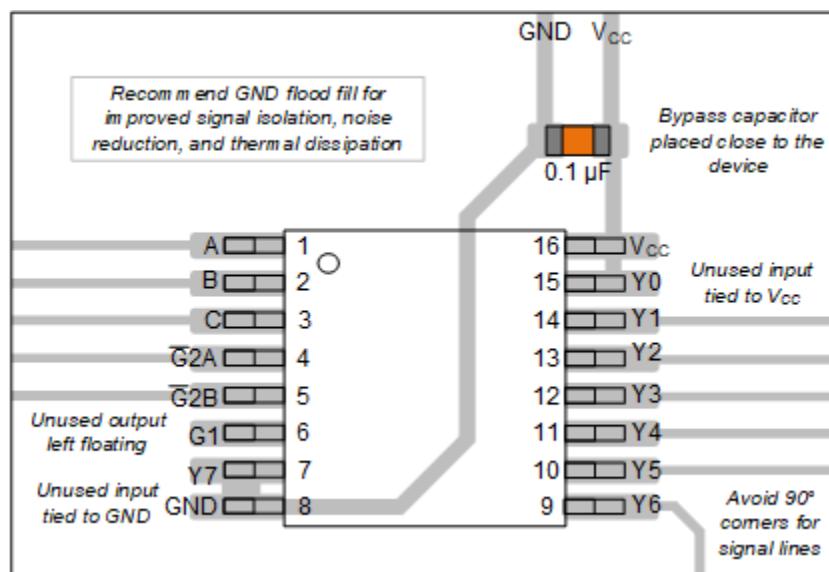


图 7-3. Example Layout for the CD74AC238

8 Device and Documentation Support

8.1 Documentation Support (Analog)

8.1.1 Related Documentation

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
CD74AC238	Click here				

8.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](#) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

8.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表

本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

Changes from Revision * (February 2003) to Revision A (April 2024)	Page
• 添加了封装信息表、引脚功能表、ESD 等级表、热性能信息表、器件功能模式、“应用和实施”部分、器件和文档支持部分以及机械、封装和可订购信息部分.....	1
• Updated R _θ JA values: M = 73 to 106.6, all values in °C/W	5

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74AC238M96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC238M	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

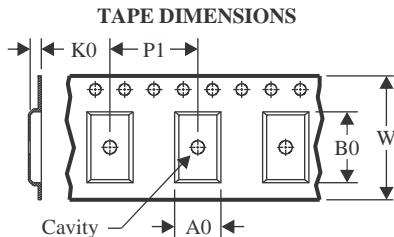
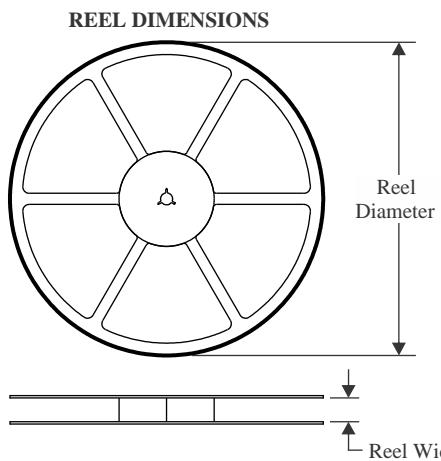
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

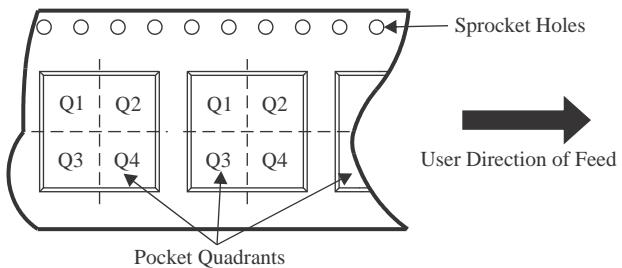
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



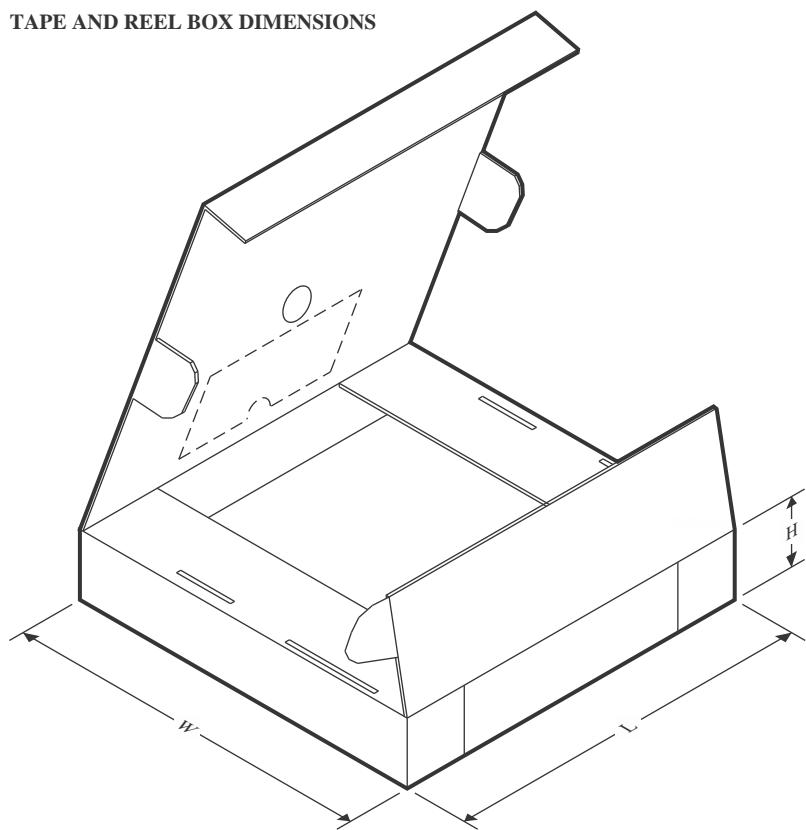
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC238M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

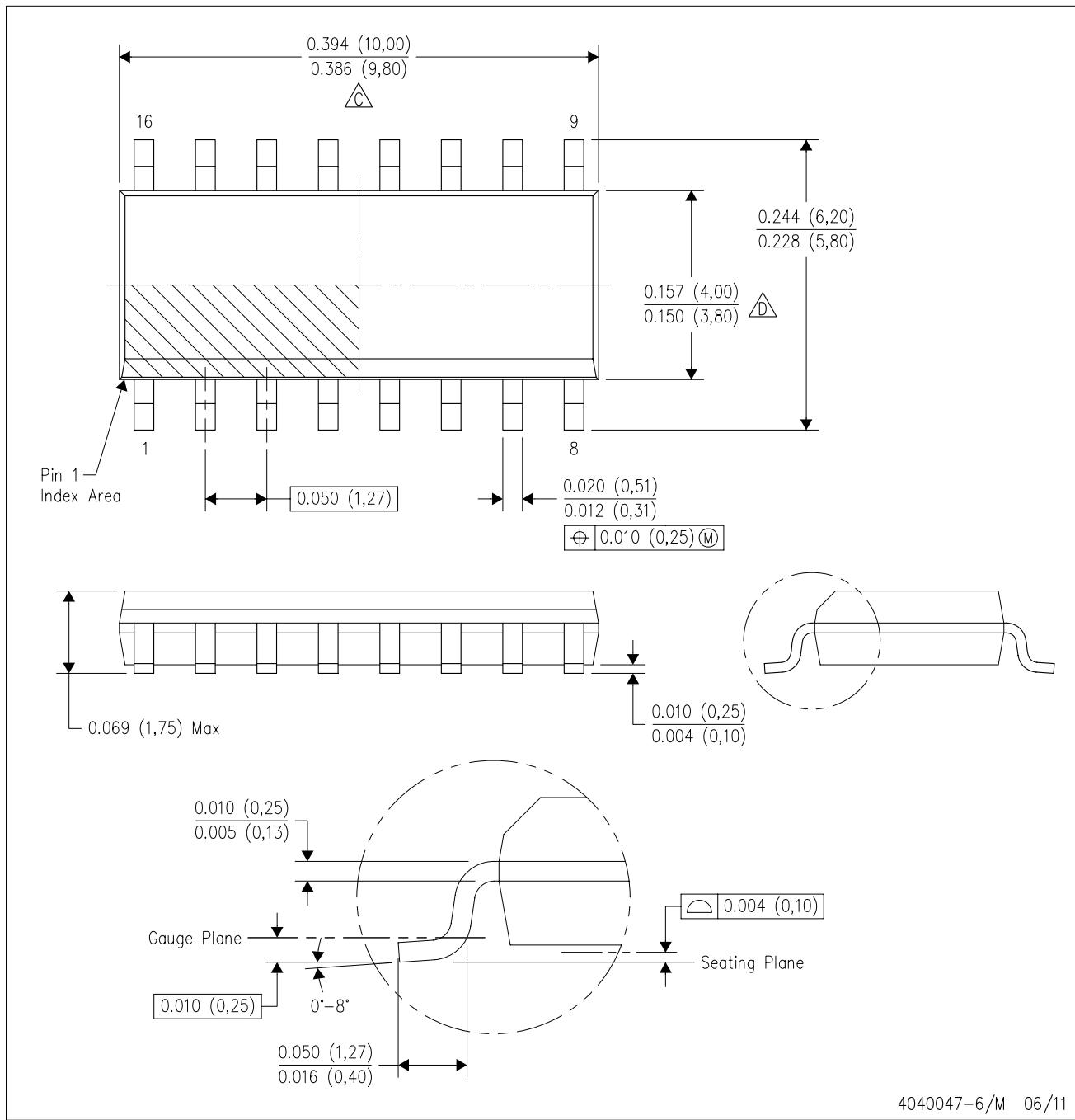
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC238M96	SOIC	D	16	2500	340.5	336.1	32.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

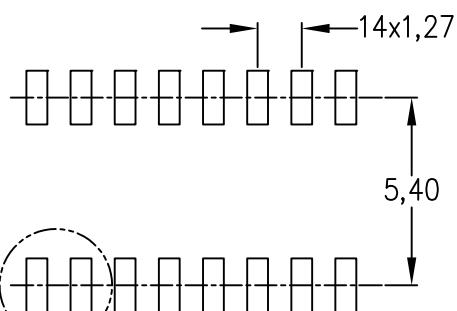
4040047-6/M 06/11

LAND PATTERN DATA

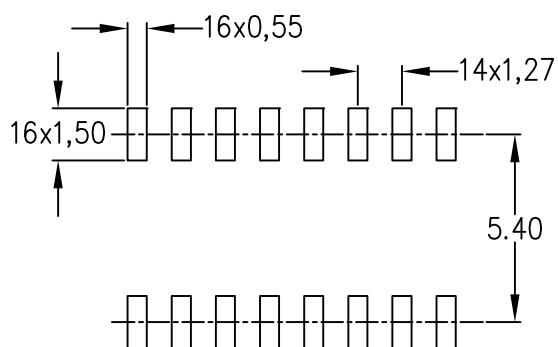
D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

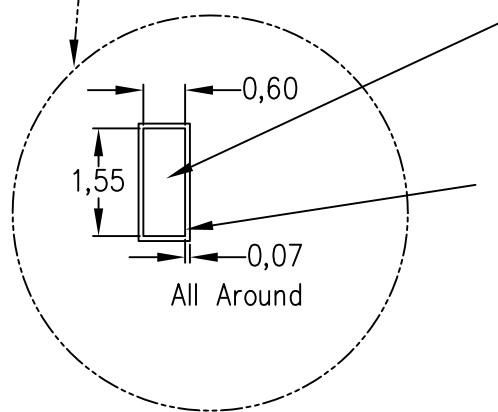
Example Board Layout
(Note C)



Stencil Openings
(Note D)



Example
Non Soldermask Defined Pad



Example
Pad Geometry
(See Note C)

Example
Solder Mask Opening
(See Note E)

4211283-4/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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