

# CSD18534Q5A 60V N 沟道 NexFET™ 功率 MOSFET

## 1 特性

- 超低  $Q_g$  和  $Q_{gd}$
- 低热阻
- 雪崩额定值
- 逻辑电平
- 无铅引脚镀层
- 符合 RoHS 标准
- 无卤素
- 小外形尺寸无引线 (SON) 5mm x 6mm 塑料封装

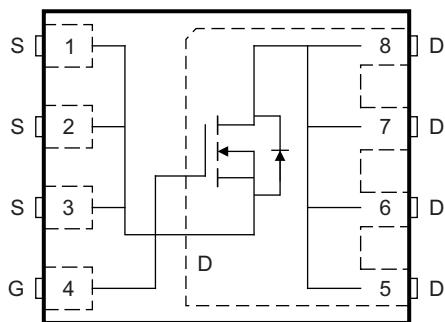
## 2 应用

- 直流 - 直流转换
- 次级侧同步整流器
- 隔离式转换器主级侧开关
- 电机控制

## 3 说明

此 7.8mΩ、60V、SON 5 × 6mm NexFET™ 功率 MOSFET 旨在最大限度地降低功率转换应用中的损耗。

顶视图



P0093-01

### 产品概要

$T_A = 25^\circ\text{C}$		典型值		单位
$V_{DS}$	漏源电压	60		V
$Q_g$	栅极电荷总量 (10V)	17		nC
$Q_{gd}$	栅极电荷 (栅极到漏极)	3.5		nC
$R_{DS(on)}$	漏源导通电阻	$V_{GS} = 4.5\text{V}$	9.9	mΩ
		$V_{GS} = 10\text{V}$	7.8	mΩ
$V_{GS(th)}$	阈值电压	1.9		V

### 订购信息(1)

器件	数量	包装介质	封装	发货
CSD18534Q5A	2500	13 英寸卷带	小外形尺寸无引线 (SON) 5mm × 6mm 塑料封装	卷带封装
CSD18534Q5AT	250	7 英寸卷带		

(1) 如需了解所有可用封装, 请参阅产品说明书末尾的可订购产品附录。

### 绝对最大额定值

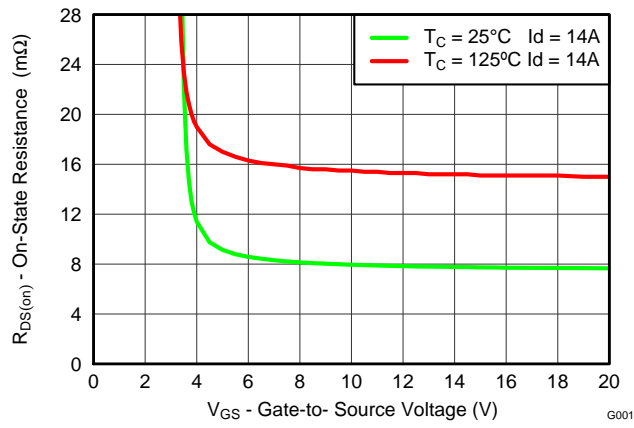
$T_A = 25^\circ\text{C}$		值	单位
$V_{DS}$	漏源电压	60	V
$V_{GS}$	栅源电压	±20	V
$I_D$	持续漏极电流 (受封装限制)	50	A
	持续漏极电流 (受芯片限制), $T_C = 25^\circ\text{C}$ 时测得	69	
	持续漏极电流, $T_A = 25^\circ\text{C}$ 时测得(1)	13	
$I_{DM}$	脉冲漏极电流, $T_A = 25^\circ\text{C}$ (2)	229	A
$P_D$	功耗(1)	3.1	W
	功耗, $T_C = 25^\circ\text{C}$	77	
$T_J, T_{stg}$	工作结温, 储存温度	-55 至 150	°C
$E_{AS}$	雪崩能量, 单一脉冲 $I_D = 40\text{A}, L = 0.1\text{mH}, R_G = 25\Omega$	80	mJ

(1)  $R_{\theta JA} = 40^\circ\text{C}/\text{W}$ , 这是在厚度为 0.06 英寸的环氧板 (FR4) 印刷电路板 (PCB) 上的 1 英寸<sup>2</sup> 2 盎司的铜过渡垫片上测得的典型值。

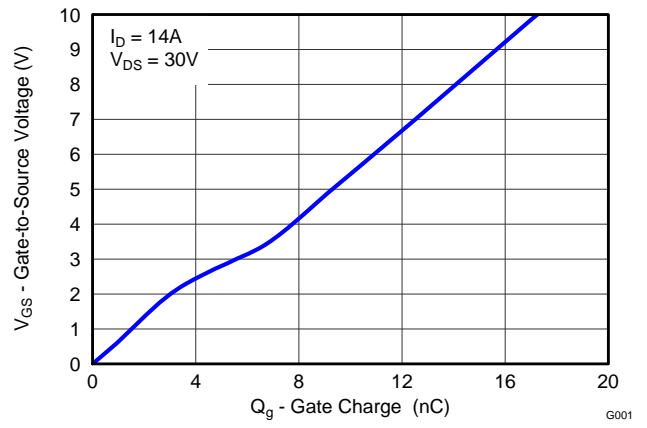
(2) 最大  $R_{\theta JC} = 2.0^\circ\text{C}/\text{W}$ , 脉冲持续时间 ≤ 100μs, 占空比 ≤ 1%



**$R_{DS(on)}$  与  $V_{GS}$  对比**



**栅极电荷**



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## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

### Changes from Revision C (August 2014) to Revision D Page

•	已更改 将说明中的电压更改成了 60V .....	1
•	已添加 <a href="#">社区资源</a> .....	8

### Changes from Revision B (July 2014) to Revision C Page

•	向订购信息表中添加了 7 英寸卷带 .....	1
•	脉冲电流增加至 229A .....	1
•	Updated the SOA in <a href="#">Figure 10</a> .....	7

### Changes from Revision A (January 2013) to Revision B Page

•	添加了外壳温度保持在 25°C 时的功率耗散参数 .....	1
•	更新了脉冲电流条件 .....	1
•	Updated <a href="#">Figure 1</a> to a normalized $R_{\theta JC}$ curve .....	5

### Changes from Original (October 2012) to Revision A Page

•	Changed $g_{fs}$ , Transconductance from: 122 to: 72 .....	4
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## 5 Specifications

### 5.1 Electrical Characteristics

 (T<sub>A</sub> = 25°C unless otherwise stated)

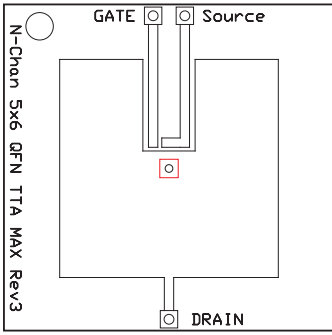
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>STATIC CHARACTERISTICS</b>						
V <sub>DSS</sub>	Drain-to-source voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	60			V
I <sub>DSS</sub>	Drain-to-source leakage current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 48 V			1	μA
I <sub>GSS</sub>	Gate-to-source leakage current	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 20 V			100	nA
V <sub>GS(th)</sub>	Gate-to-source threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.5	1.9	2.3	V
R <sub>DS(on)</sub>	Drain-to-source on-resistance	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 14 A		9.9	12.4	mΩ
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 14 A		7.8	9.8	mΩ
g <sub>fs</sub>	Transconductance	V <sub>DS</sub> = 30 V, I <sub>D</sub> = 14 A		72		S
<b>DYNAMIC CHARACTERISTICS</b>						
C <sub>iss</sub>	Input capacitance	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 30 V, f = 1 MHz		1360	1770	pF
C <sub>oss</sub>	Output capacitance			167	217	pF
C <sub>rss</sub>	Reverse transfer capacitance			5	6.5	pF
R <sub>G</sub>	Series gate resistance			1.5	3	Ω
Q <sub>g</sub>	Gate charge total (4.5 V)	V <sub>DS</sub> = 30 V, I <sub>D</sub> = 14 A		8.5	11.1	nC
Q <sub>g</sub>	Gate charge total (10 V)			17	22	
Q <sub>gd</sub>	Gate charge gate-to-drain			3.5		nC
Q <sub>gs</sub>	Gate charge gate-to-source			3.2		nC
Q <sub>g(th)</sub>	Gate charge at V <sub>th</sub>			2.6		nC
Q <sub>oss</sub>	Output charge		V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V		19	
t <sub>d(on)</sub>	Turn on delay time	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 10 V, I <sub>DS</sub> = 14 A, R <sub>G</sub> = 0 Ω		5.2		ns
t <sub>r</sub>	Rise time			5.5		ns
t <sub>d(off)</sub>	Turn off delay time			15		ns
t <sub>f</sub>	Fall time			2		ns
<b>DIODE CHARACTERISTICS</b>						
V <sub>SD</sub>	Diode forward voltage	I <sub>SD</sub> = 14 A, V <sub>GS</sub> = 0 V		0.8	1	V
Q <sub>rr</sub>	Reverse recovery charge	V <sub>DS</sub> = 30 V, I <sub>F</sub> = 14 A, di/dt = 300 A/μs		54		nC
t <sub>rr</sub>	Reverse recovery time			40		ns

### 5.2 Thermal Information

 (T<sub>A</sub> = 25°C unless otherwise stated)

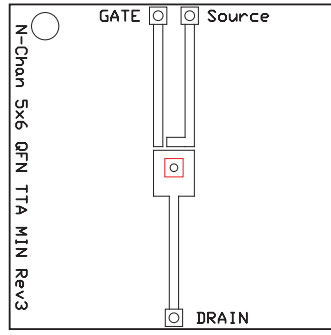
THERMAL METRIC		MIN	TYP	MAX	UNIT
R <sub>θJC</sub>	Junction-to-case thermal resistance <sup>(1)</sup>			2.0	°C/W
R <sub>θJA</sub>	Junction-to-ambient thermal resistance <sup>(1)(2)</sup>			50	°C/W

- (1) R<sub>θJC</sub> is determined with the device mounted on a 1 inch<sup>2</sup> (6.45 cm<sup>2</sup>), 2 oz. (0.071 mm thick) Cu pad on a 1.5 inches × 1.5 inches (3.81 cm × 3.81 cm), 0.06 inch (1.52 mm) thick FR4 PCB. R<sub>θJC</sub> is specified by design, whereas R<sub>θJA</sub> is determined by the user's board design.
- (2) Device mounted on FR4 material with 1 inch<sup>2</sup> (6.45 cm<sup>2</sup>), 2 oz. (0.071 mm thick) Cu.



M0137-01

Max  $R_{\theta JA} = 50^{\circ}\text{C/W}$   
when mounted on  
1 inch<sup>2</sup> (6.45 cm<sup>2</sup>) of  
2 oz. (0.071 mm thick)  
Cu.

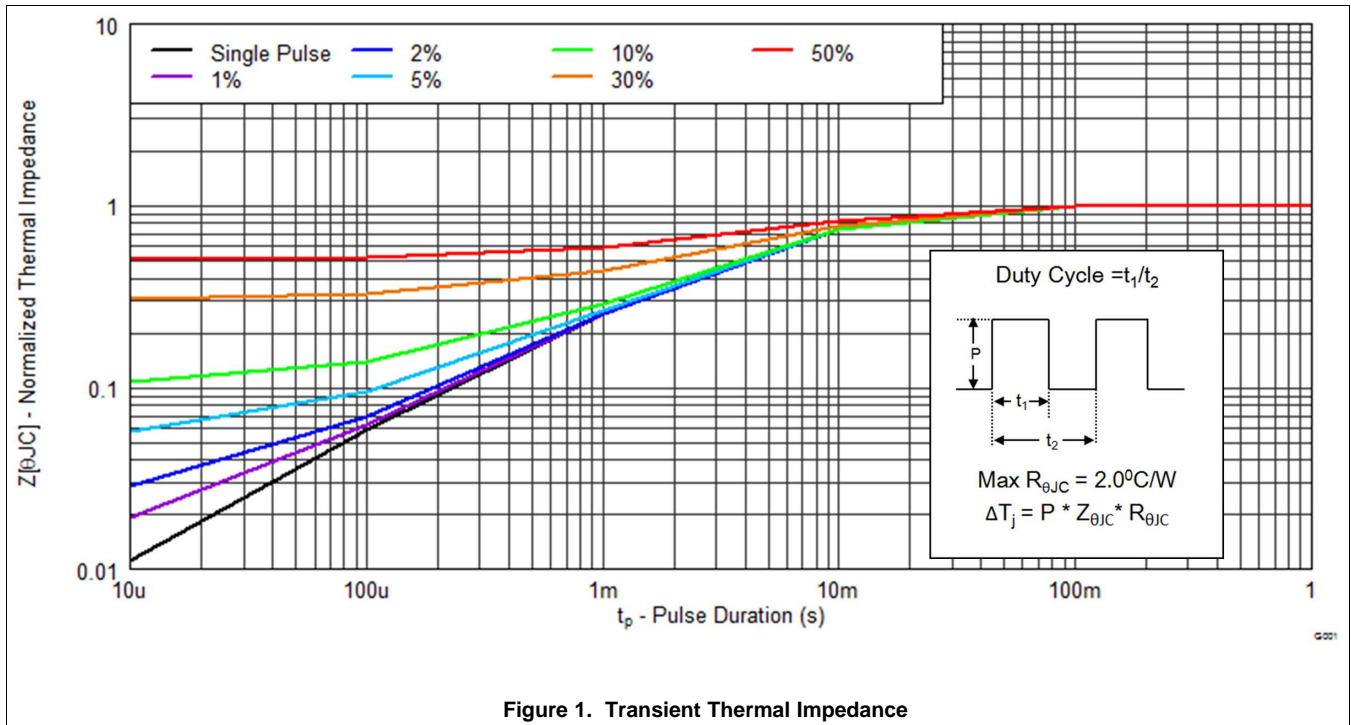


M0137-02

Max  $R_{\theta JA} = 125^{\circ}\text{C/W}$   
when mounted on a  
minimum pad area of  
2 oz. (0.071 mm thick)  
Cu.

### 5.3 Typical MOSFET Characteristics

( $T_A = 25^{\circ}\text{C}$  unless otherwise stated)



Typical MOSFET Characteristics (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

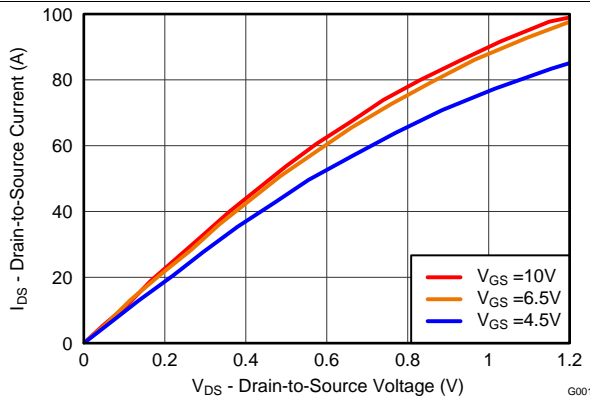


Figure 2. Saturation Characteristics

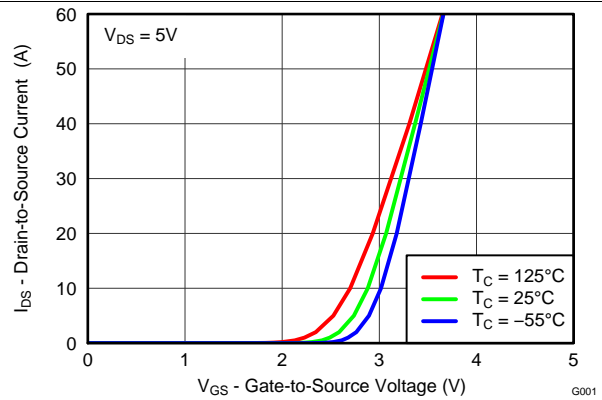


Figure 3. Transfer Characteristics

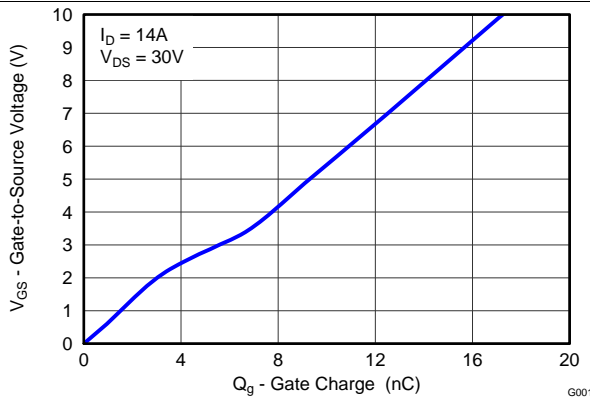


Figure 4. Gate Charge

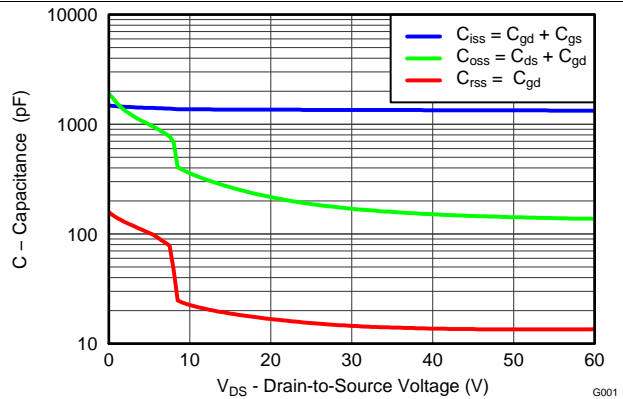


Figure 5. Capacitance

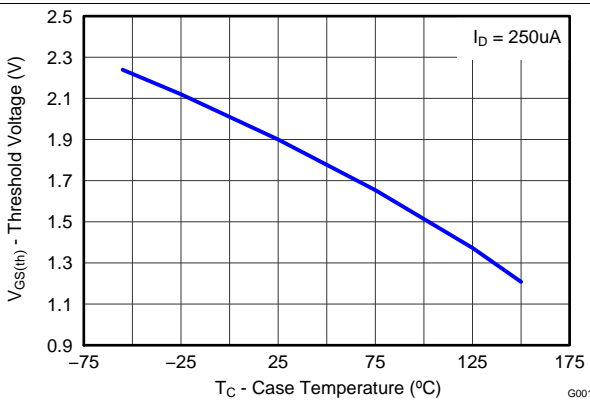


Figure 6. Threshold Voltage vs Temperature

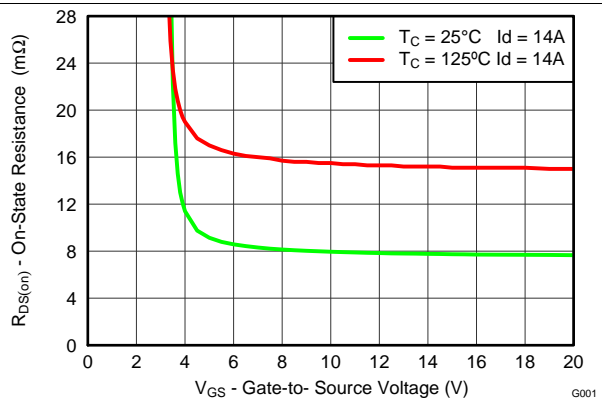


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

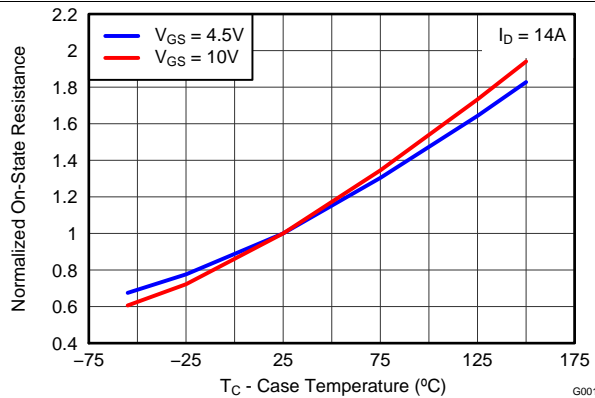


Figure 8. Normalized On-State Resistance vs Temperature

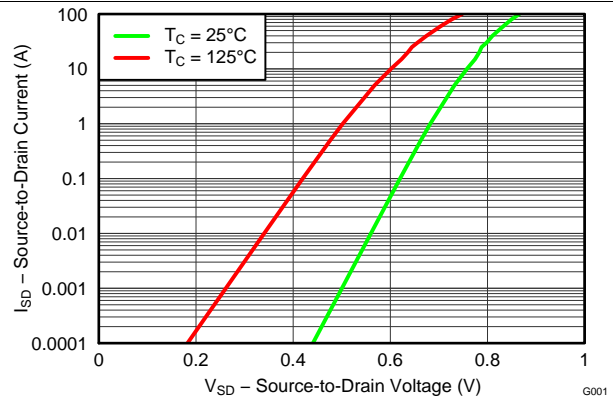


Figure 9. Typical Diode Forward Voltage

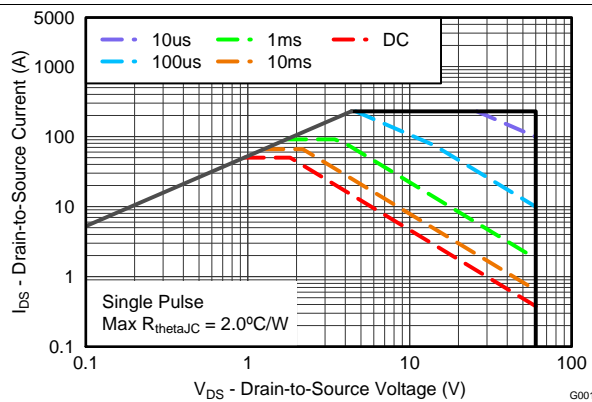


Figure 10. Maximum Safe Operating Area

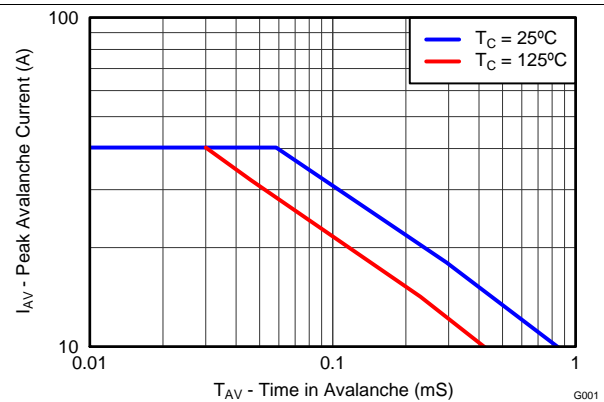


Figure 11. Single Pulse Unclamped Inductive Switching

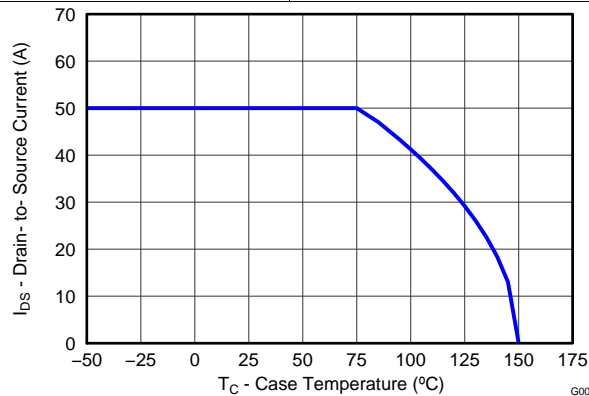


Figure 12. Maximum Drain Current vs Temperature

## 6 器件和文档支持

### 6.1 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

**TI E2E™ 在线社区** *TI 的工程师对工程师 (E2E) 社区*。此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

**设计支持** *TI 参考设计支持* 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

### 6.2 商标

NexFET, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 6.3 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 6.4 Glossary

**SLYZ022** — *TI Glossary*.

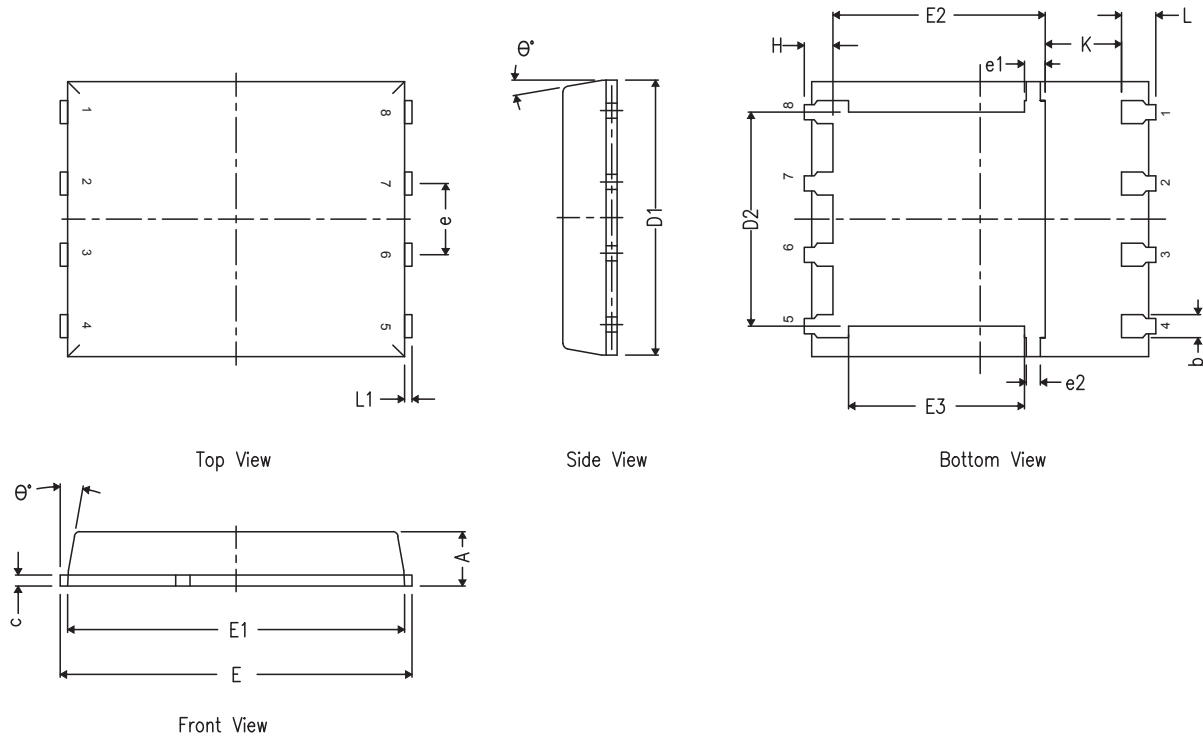
This glossary lists and explains terms, acronyms, and definitions.



## 7 机械、封装和可订购信息

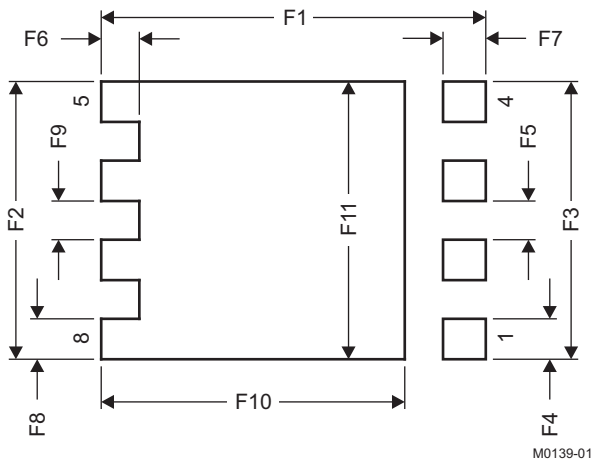
以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

### 7.1 Q5A 封装尺寸



DIM	毫米		
	最小值	标称值	最大值
A	0.90	1.00	1.10
b	0.33	0.41	0.51
c	0.20	0.25	0.34
D1	4.80	4.90	5.00
D2	3.61	3.81	4.02
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
E3	3.03	3.13	3.23
e	1.17	1.27	1.37
e1	0.27	0.37	0.47
e2	0.15	0.25	0.35
H	0.41	0.56	0.71
K	1.10	—	—
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
$\theta$	0°	—	12°

### 7.2 建议印刷电路板 (PCB) 布局

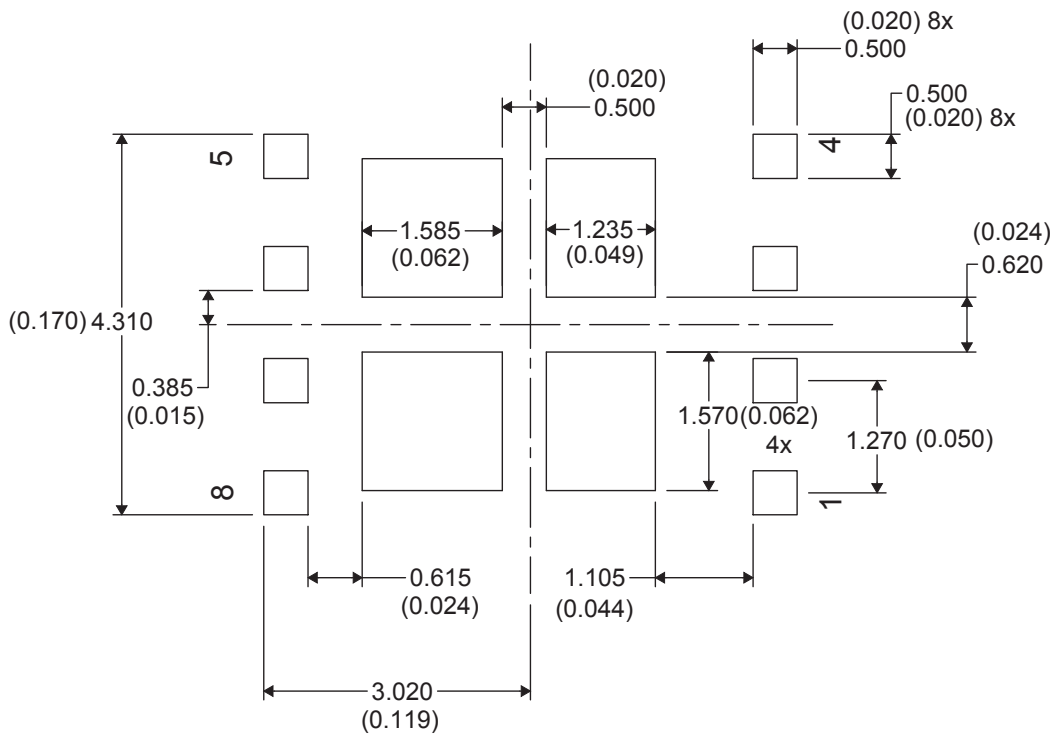


### 建议印刷电路板 (PCB) 布局 (接下页)

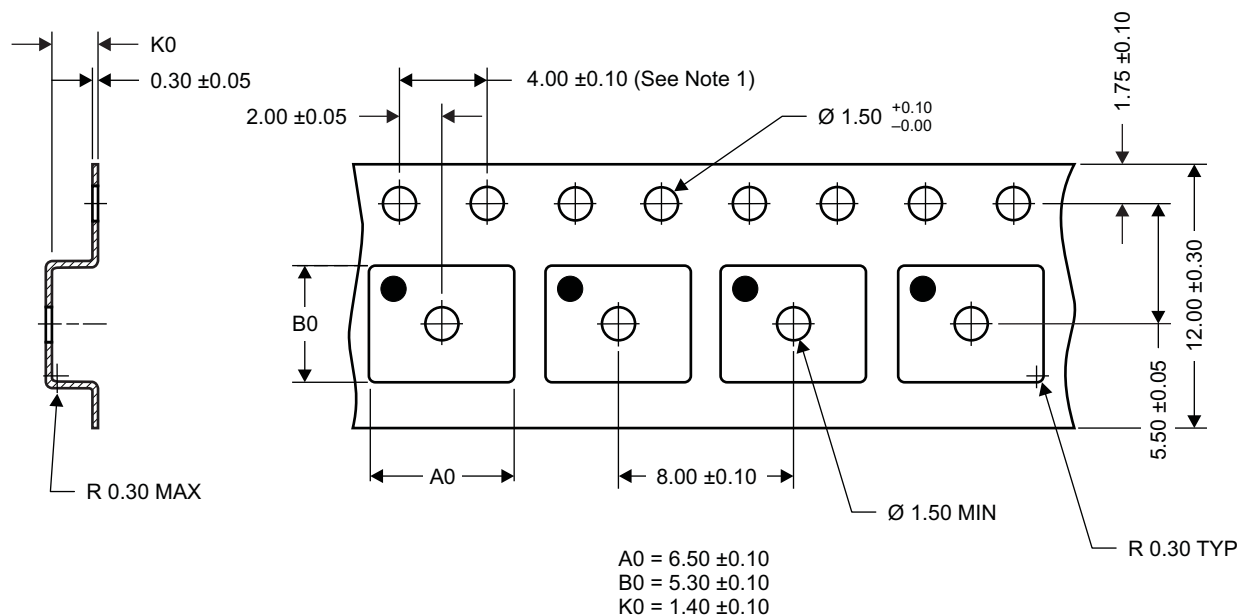
DIM	毫米		英寸	
	最小值	最大值	最小值	最大值
F1	6.205	6.305	0.244	0.248
F2	4.46	4.56	0.176	0.18
F3	4.46	4.56	0.176	0.18
F4	0.65	0.7	0.026	0.028
F5	0.62	0.67	0.024	0.026
F6	0.63	0.68	0.025	0.027
F7	0.7	0.8	0.028	0.031
F8	0.65	0.7	0.026	0.028
F9	0.62	0.67	0.024	0.026
F10	4.9	5	0.193	0.197
F11	4.46	4.56	0.176	0.18

要获得与印刷电路板 (PCB) 设计相关的建议电路布局布线, 请参见应用说明《通过 PCB 布局布线技巧来减少振铃》, [SLPA005](#)。

### 7.3 建议模板开口



## 7.4 Q5A 卷带信息



M0138-01

注:

1. 10 个链齿孔的累积容差为  $\pm 0.2$
2. 每 100mm 长度的翘曲不能超过 1mm, 在 250mm 长度上不累积
3. 材料: 黑色抗静电聚苯乙烯
4. 全部尺寸为 mm (除非另外注明)。
5. 高于孔眼底部 0.3mm 的平面上测量得到 A0 和 B0 值。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD18534Q5A	ACTIVE	VSONP	DQJ	8	2500	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD18534	<a href="#">Samples</a>
CSD18534Q5AT	ACTIVE	VSONP	DQJ	8	250	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	CSD18534	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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