CSD25484F4 -20V P 沟道 FemtoFET™ MOSFET

1 特性

- 低导通电阻
- 超低 Q_g 和 Q_{gd}
- 低阈值电压
- 超小封装尺寸（0402 外壳尺寸）
  - 1.0mm × 0.6mm
- 超薄型封装
  - 厚度为 0.2mm
- 集成型 ESD 保护二极管
  - 额定值 > 4kV HBM
  - 额定值 > 2kV CDM
- 无铅且无卤素
- 符合 RoHS

2 应用

- 针对负载开关应用进行了优化
- 针对通用开关应用进行了优化
- 电池应用
- 手持式和移动类应用

3 说明

该 80mΩ、-20V P 沟道 FemtoFET™ MOSFET 经过设计和优化，能够最大限度地减小在许多手持式和移动应用中占用的空间。这项技术能够在替代标准小信号 MOSFET 的同时将封装尺寸减小至少 60%。

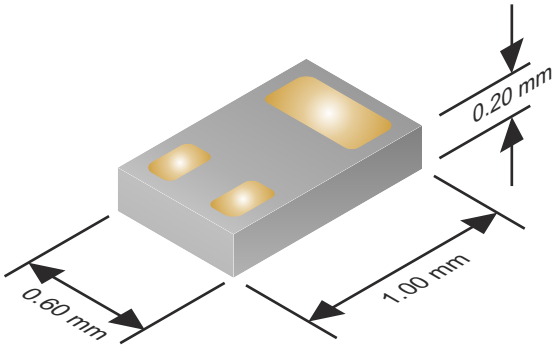

图 3-1. 典型封装尺寸

产品概要

T_A = 25°C		典型值	单位
V_{DS}	漏源电压	-20	V

产品概要 (continued)

T_A = 25°C		典型值		单位
Q_g	栅极电荷总量 (-4.5V)	1090		pC
Q_{gd}	栅极电荷（栅漏极）	150		pC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = –1.8V	405	mΩ
		V_{GS} = -2.5V	150	
		V_{GS} = –4.5V	93	
		V_{GS} = -8.0V	80	
$V_{GS(th)}$	阈值电压	-0.95		V

器件信息

器件	数量	介质	封装(1)	配送
CSD25484F4	3000	7 英寸卷带	Femto (0402) 1.00mm × 0.60mm 基板栅格阵列 (LGA)	卷带包装
CSD25484F4T	250			

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

绝对最大额定值

T_A = 25°C		值	单位
V_{DS}	漏源电压	-20	V
V_{GS}	栅源电压	–12	V
I_D	持续漏极电流(1)	-2.5	A
I_{DM}	脉冲漏极电流(1) (2)	–22	A
I_G	持续栅极钳位电流	-35	mA
	脉冲栅极钳位电流(2)	-350	
P_D	功率耗散(1)	500	mW
$V_{(ESD)}$	人体放电模式 (HBM)	4	kV
	充电器件模型 (CDM)	2	
T_J、T_{stg}	工作结温，贮存温度	–55 至 150	°C

(1) 典型 $R_{\theta JA}$ = 85°C/W（在 0.06 英寸 (1.52mm) 厚的 FR4 PCB 上安装 1 平方英寸 (6.45cm²)、2oz、0.071mm 厚的铜焊盘时）。
(2) 脉冲持续时间 ≤ 100μs，占空比 ≤ 1%。

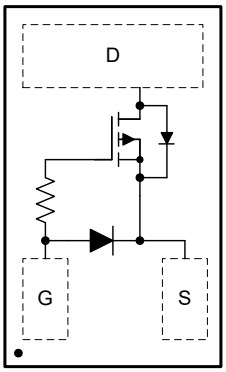

图 3-2. 顶视图

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4 Revision History

Changes from Revision A (August 2017) to Revision B (February 2022) **Page**

- Added FemtoFET Surface Mount Guide note 9

Changes from Revision * (May 2015) to Revision A (August 2017) **Page**

- Added the 节 *6.1* and the 节 *6*section 7
- Updated the 节 *7.2* and the 节 *7.3* sections 8

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_{DS} = –250 μA	–20			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = –16 V			–100	nA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = –12 V			–50	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = –250 μA	–0.7	–0.95	–1.2	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = –1.8 V, I_{DS} = –0.1 A		405	825	mΩ
		V_{GS} = –2.5 V, I_{DS} = –0.5 A		150	180	
		V_{GS} = –4.5 V, I_{DS} = –0.5 A		93	109	
		V_{GS} = –8 V, I_{DS} = –0.5 A		80	94	
g_{fs}	Transconductance	V_{DS} = –10 V, I_{DS} = –0.5 A		3.5		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = –10 V, f = 1 MHz		175	230	pF
C_{oss}	Output capacitance			78	102	pF
C_{rss}	Reverse transfer capacitance			5.5	7.2	pF
R_G	Series gate resistance			20		Ω
Q_g	Gate charge total (–4.5 V)	V_{DS} = –10 V, I_{DS} = –0.5 A		1090	1415	pC
Q_{gd}	Gate charge gate-to-drain			150		pC
Q_{gs}	Gate charge gate-to-source			350		pC
$Q_{g(th)}$	Gate charge at V_{th}			210		pC
Q_{oss}	Output charge	V_{DS} = –10 V, V_{GS} = 0 V		1290		pC
$t_{d(on)}$	Turnon delay time	V_{DS} = –10 V, V_{GS} = –4.5 V, I_{DS} = –0.5 A, R_G = 10 Ω		9.5		ns
t_r	Rise time			5		ns
$t_{d(off)}$	Turnoff delay time			18		ns
t_f	Fall Time			8.5		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = –0.5 A, V_{GS} = 0 V		–0.75		V
Q_{rr}	Reverse recovery charge	V_{DS}= –10 V, I_F = –0.5 A, di/dt = 100 A/μs		970		pC
t_{rr}	Reverse recovery time			7.5		ns

5.2 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		TYPICAL VALUES	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	85	°C/W
	Junction-to-ambient thermal resistance(2)	245	

(1) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

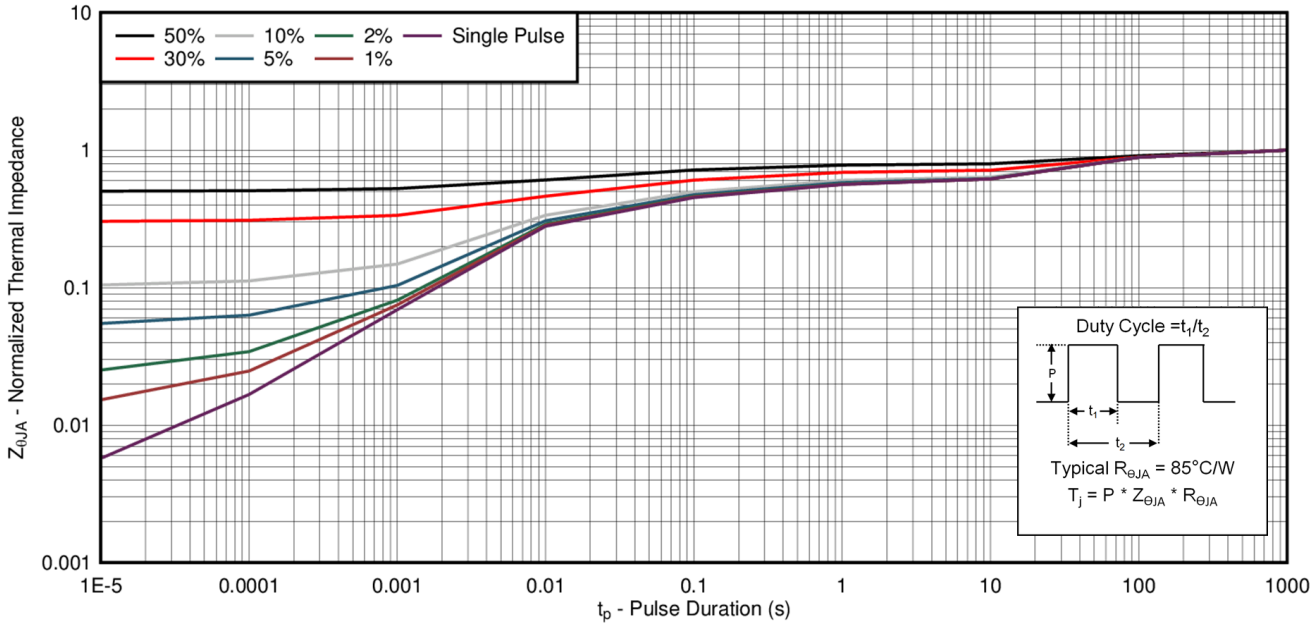


图 5-1. Transient Thermal Impedance

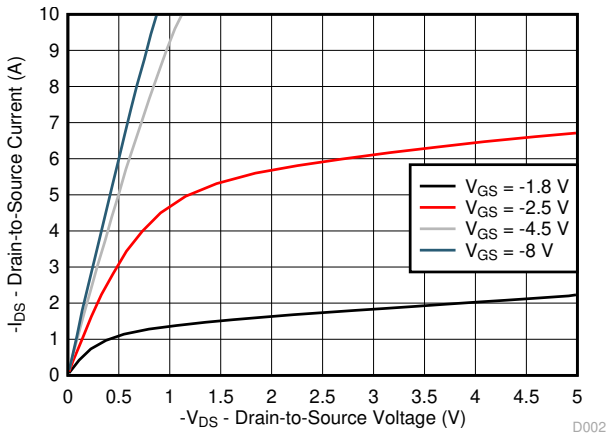
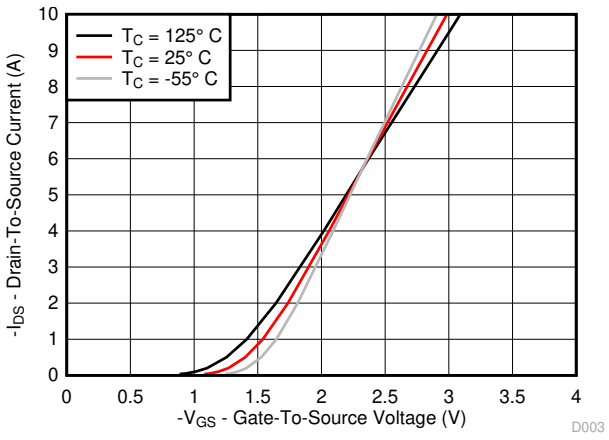
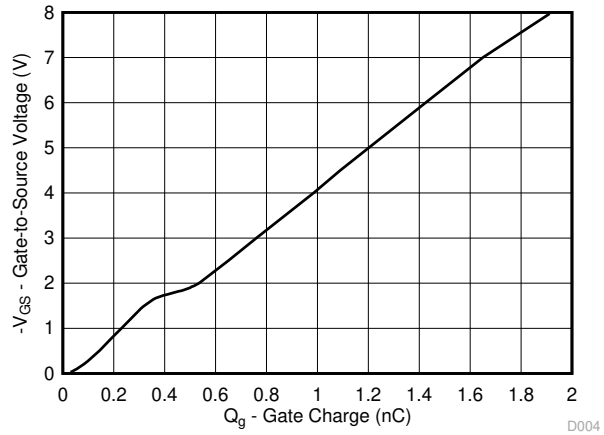


图 5-2. Saturation Characteristics



V_{DS} = – 5V

图 5-3. Transfer Characteristics



I_D = – 0.5 A V_{DS} = – 10 V

图 5-4. Gate Charge

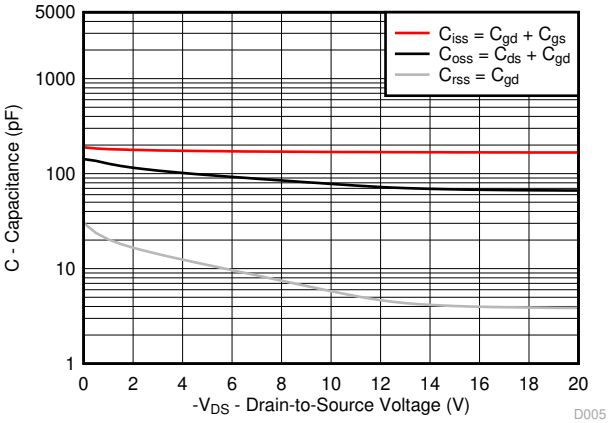
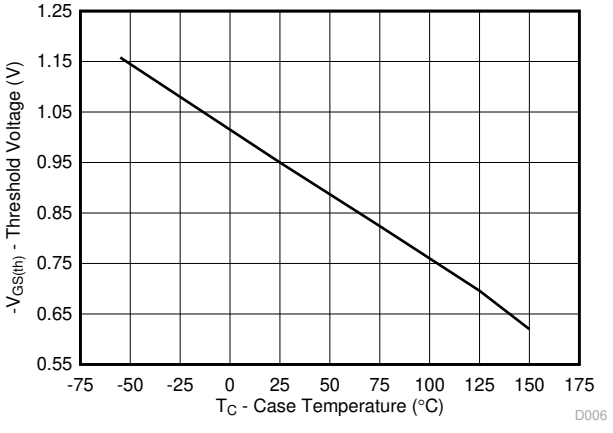


图 5-5. Capacitance



I_D = – 250 µA

图 5-6. Threshold Voltage vs Temperature

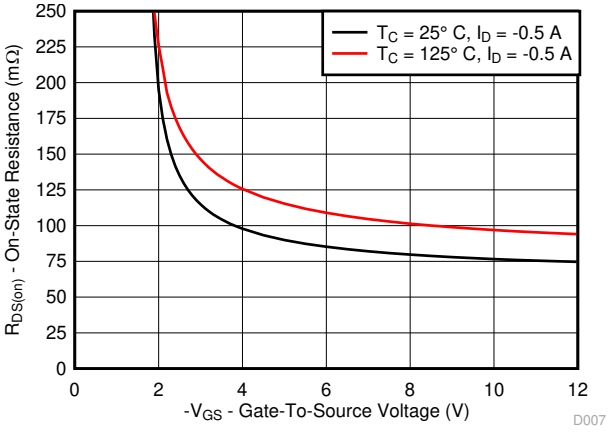
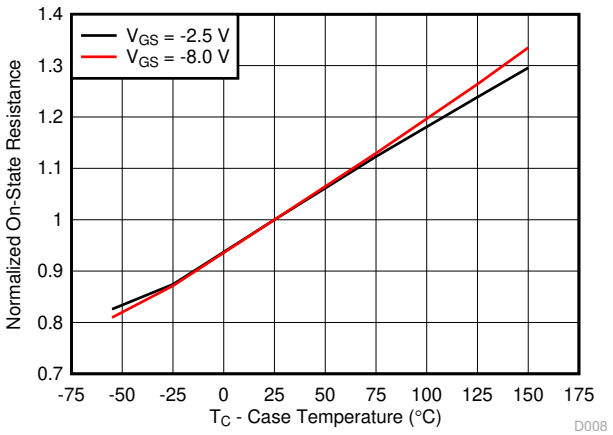


图 5-7. On-State Resistance vs Gate-to-Source Voltage



I_D = –0.5 A

图 5-8. Normalized On-State Resistance vs Temperature

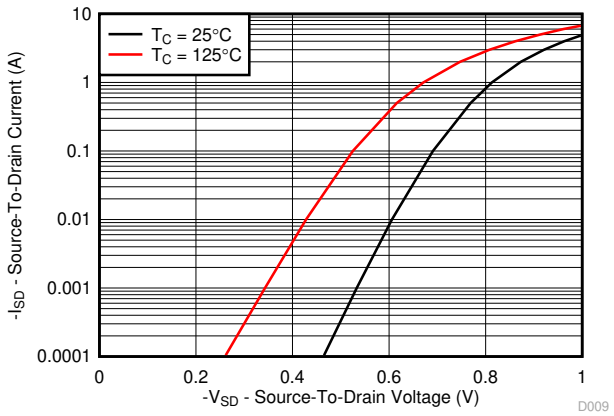
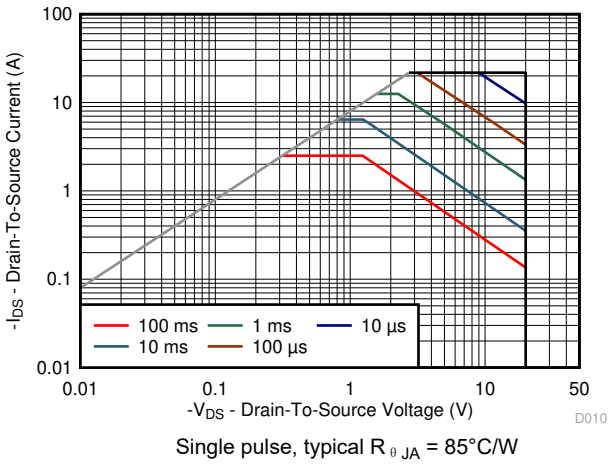


图 5-9. Typical Diode Forward Voltage



Single pulse, typical $R_{\theta JA}$ = 85°C/W

图 5-10. Maximum Safe Operating Area

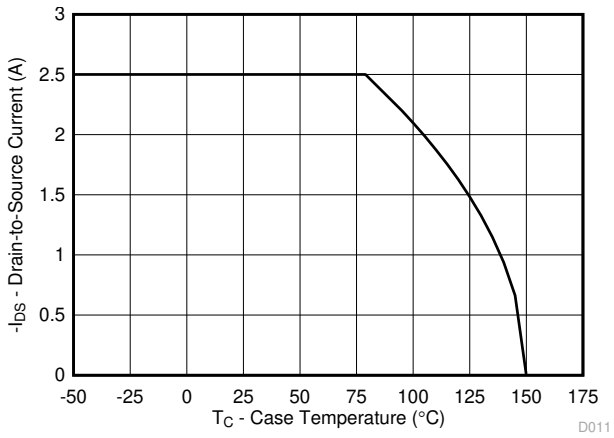


图 5-11. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

6.3 Trademarks

FemtoFET™ is a trademark of Texas Instruments.
TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

6.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

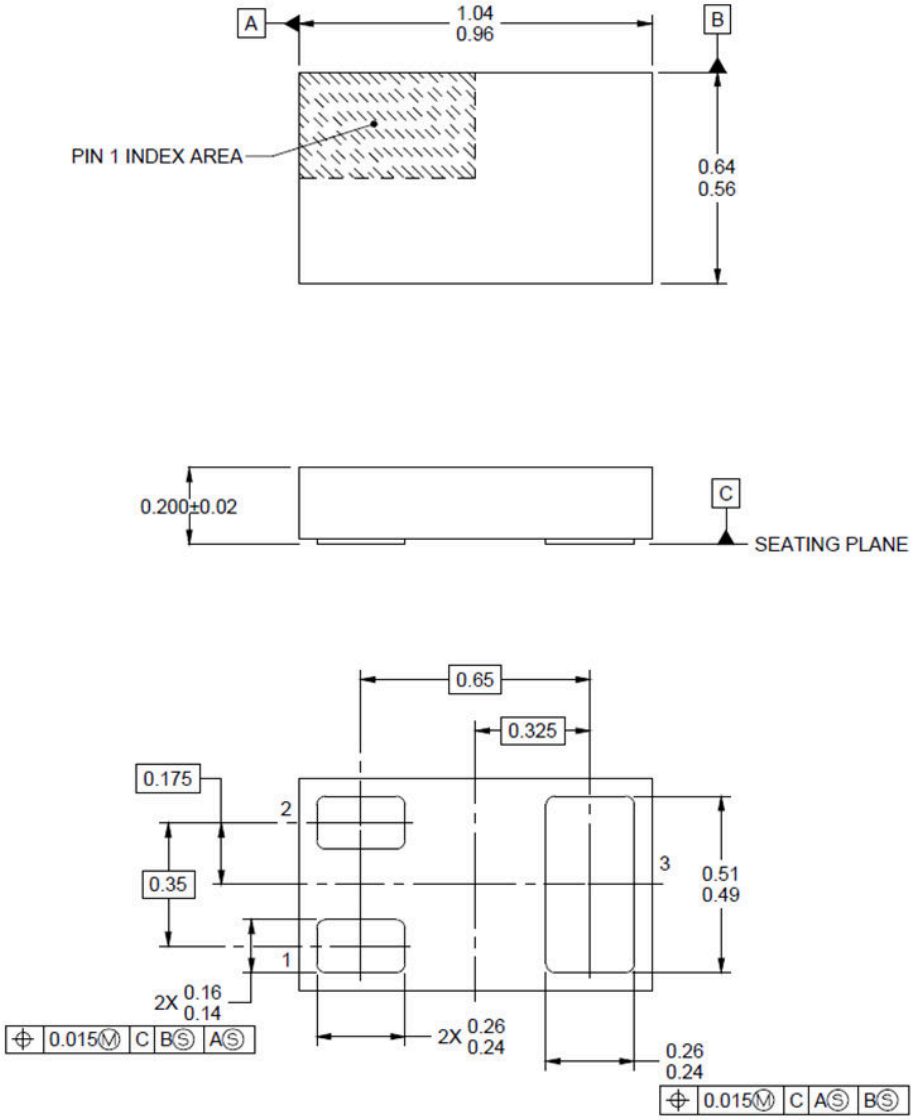
6.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Mechanical Dimensions

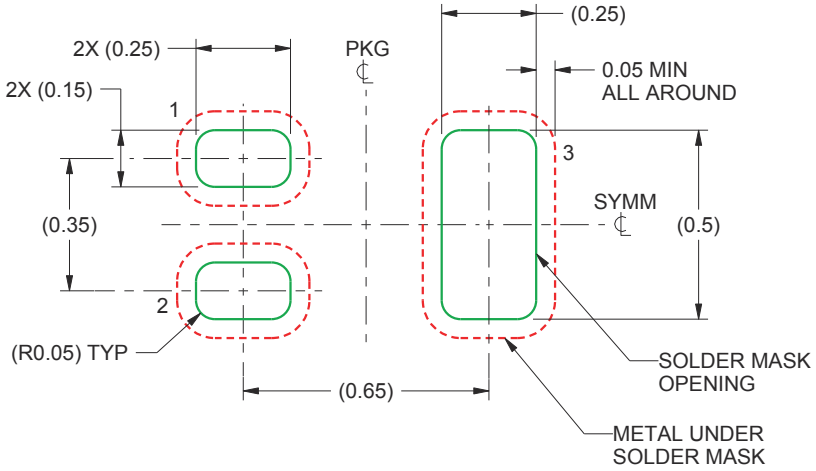


A. All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).
B. This drawing is subject to change without notice.
C. This package is a PB-free solder land design.

表 7-1. Pin Configuration

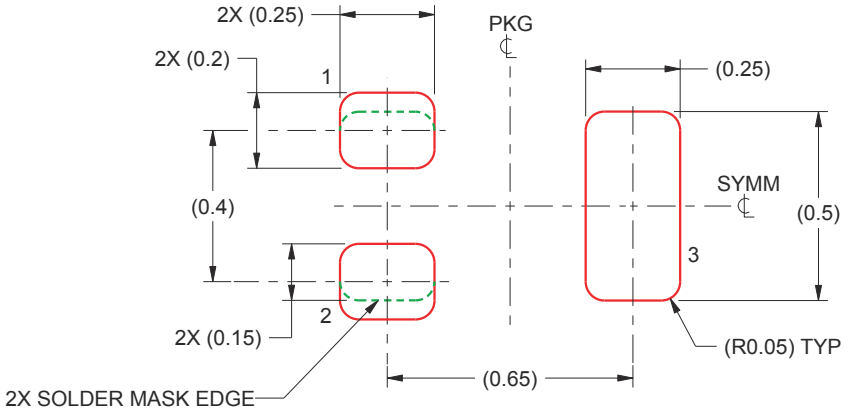
POSITION	DESIGNATION
Pin 1	Gate
Pin 2	Source
Pin 3	Drain

7.2 Recommended Minimum PCB Layout



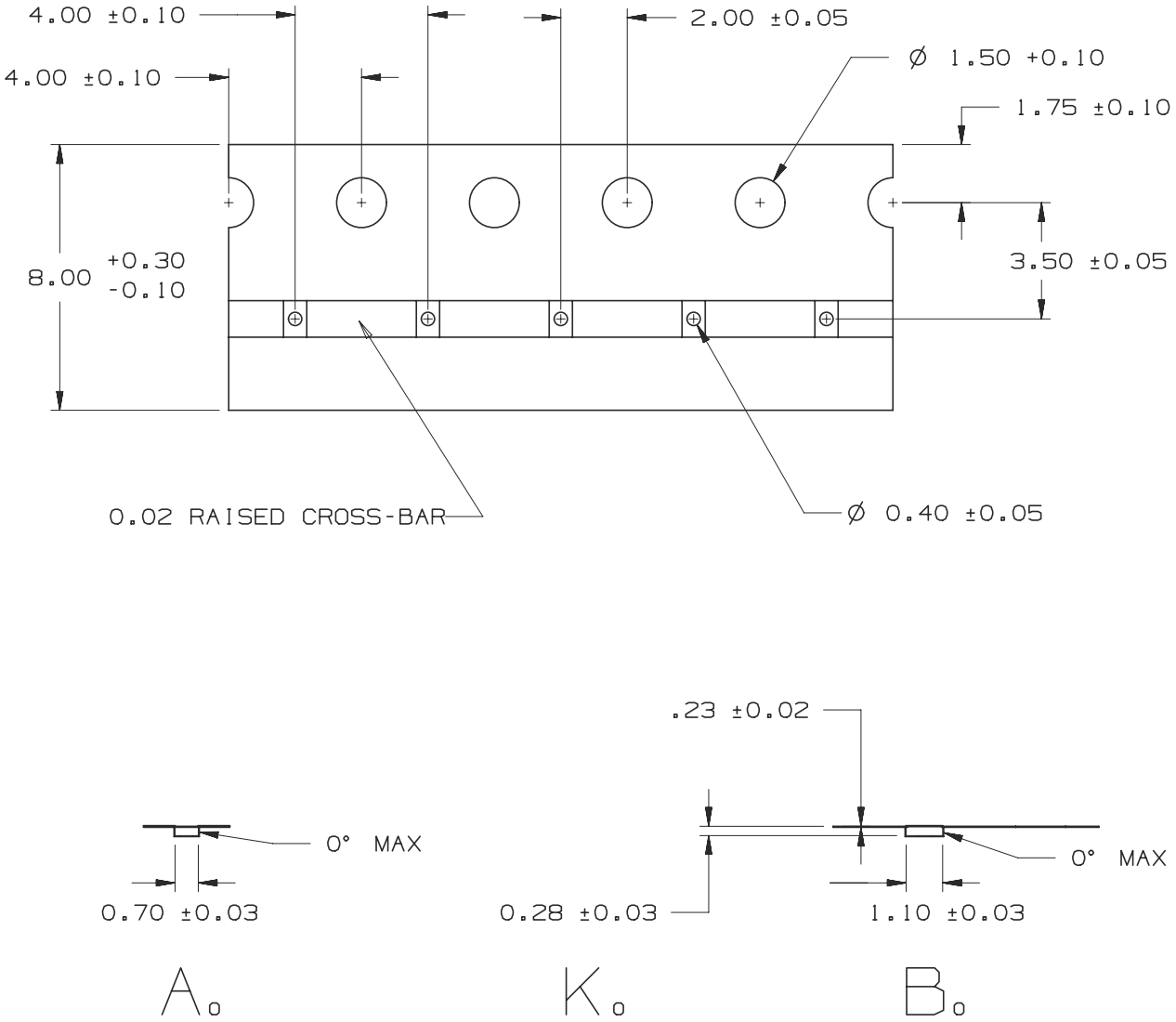
A. All dimensions are in millimeters.
B. For more information, see *FemtoFET Surface Mount Guide* (SLRA003D).

7.3 Recommended Stencil Pattern



A. All dimensions are in millimeters.

7.4 CSD68830F4 Embossed Carrier Tape Dimensions



A. Pin 1 is oriented in the top-right quadrant of the tape enclosure (quadrant 2), closest to the carrier tape sprocket holes.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD25484F4	ACTIVE	PICOSTAR	YJJ	3	3000	RoHS & Green	NIAU	Level-1-260C-UNLIM	-55 to 150	G3	Samples
CSD25484F4T	ACTIVE	PICOSTAR	YJJ	3	250	RoHS & Green	NIAU	Level-1-260C-UNLIM	-55 to 150	G3	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

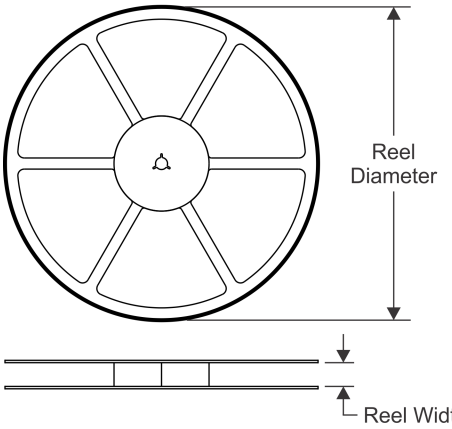
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

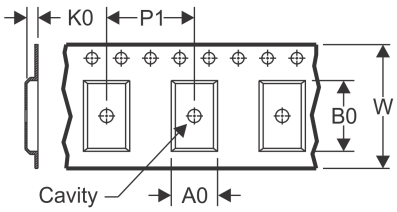
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

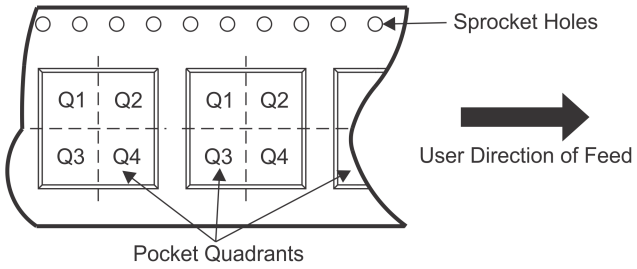


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

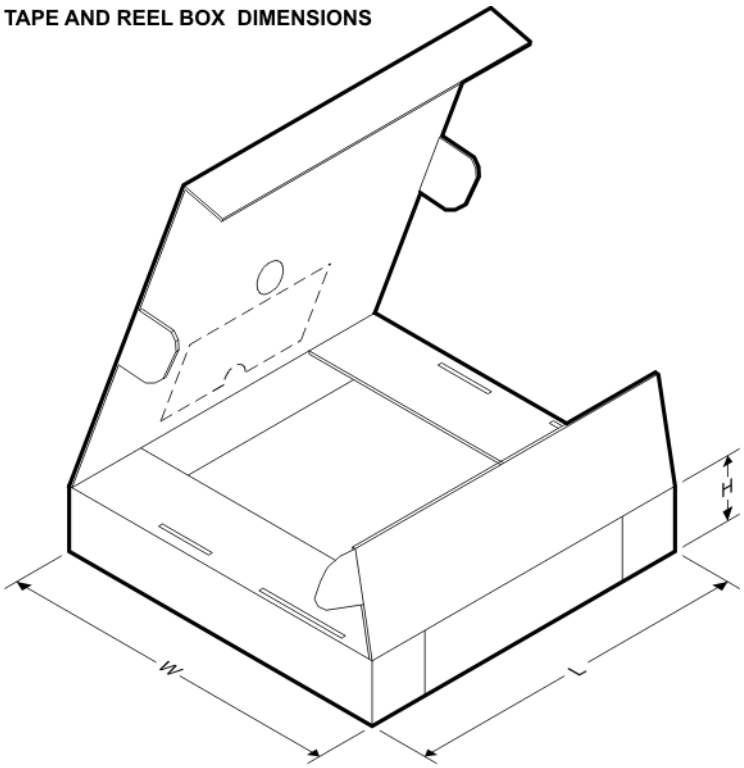
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD25484F4	PICOSTAR	YJJ	3	3000	178.0	9.2	0.7	1.1	0.28	4.0	8.0	Q2
CSD25484F4T	PICOSTAR	YJJ	3	250	178.0	9.2	0.7	1.1	0.28	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

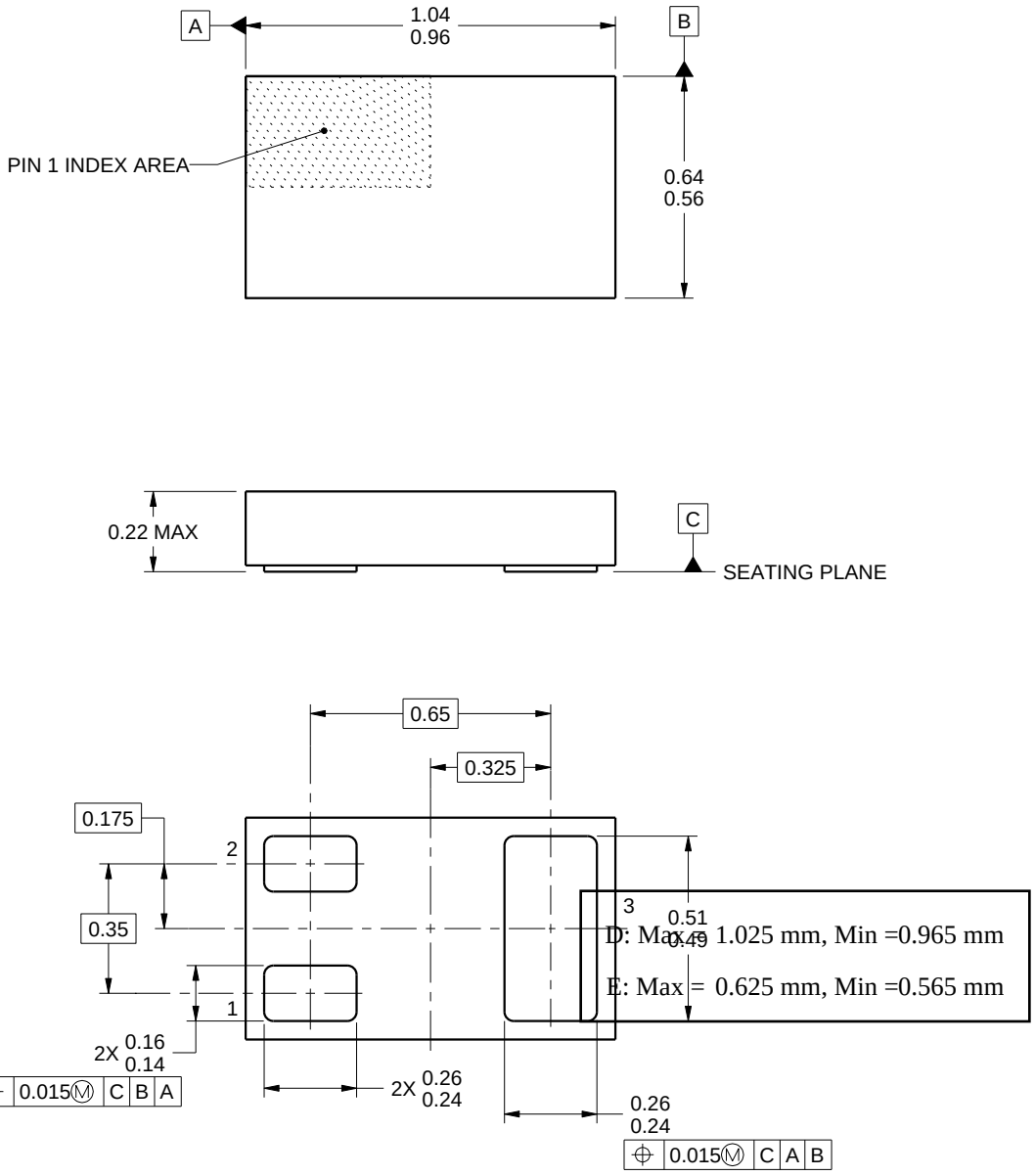
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD25484F4	PICOSTAR	YJJ	3	3000	220.0	220.0	35.0
CSD25484F4T	PICOSTAR	YJJ	3	250	220.0	220.0	35.0

PACKAGE OUTLINE

YJJ0003A

PicoStar™ - 0.22 mm max height

PicoStar™

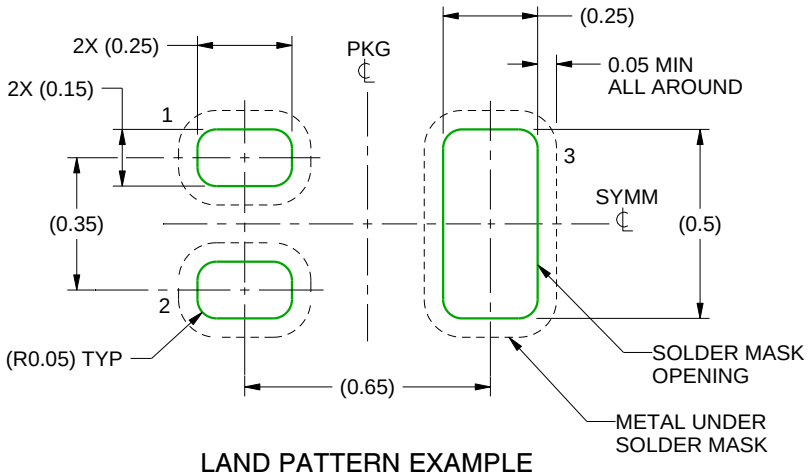


4221828/B 08/2016

PicoStar is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.
3. This package is a Pb-free bump design. Bump finish may vary. To determine the exact finish, refer to the device datasheet or contact a local TI representative.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:50X

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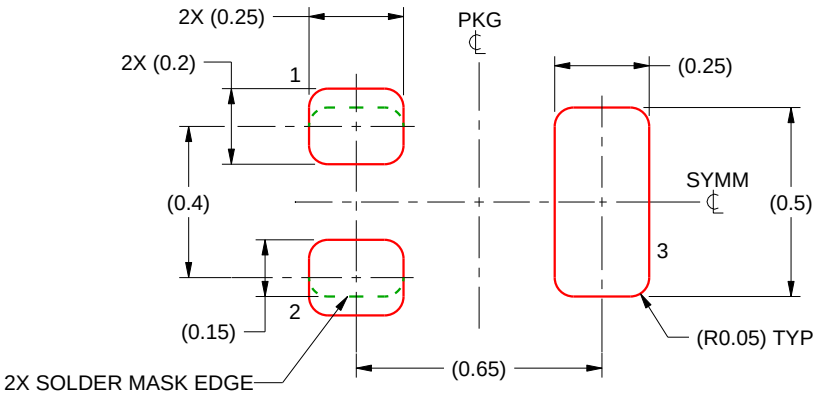
NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:50X

4221828/B 08/2016

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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