

## DLP470TE 0.47 4K UHD 数字微镜器件

### 1 特性

- 0.47 英寸对角线微镜阵列
  - 4K 超高清 (3840 × 2160) 显示分辨率
  - 5.4 微米微镜间距
  - ±17° 微镜倾斜度 (相对于平坦表面)
  - 底部照明
- 2xLVDS 输入数据总线
- DLP470TE 芯片组包括：
  - [DLP470TE DMD](#)
  - [DLPC4420 控制器](#)
  - [DLPA100 控制器电源管理和电机驱动器 IC](#)

### 2 应用

- [4K 超高清显示](#)
- [激光电视](#)
- [商业和教育](#)
- [数字标牌](#)
- [游戏](#)
- [家庭影院](#)

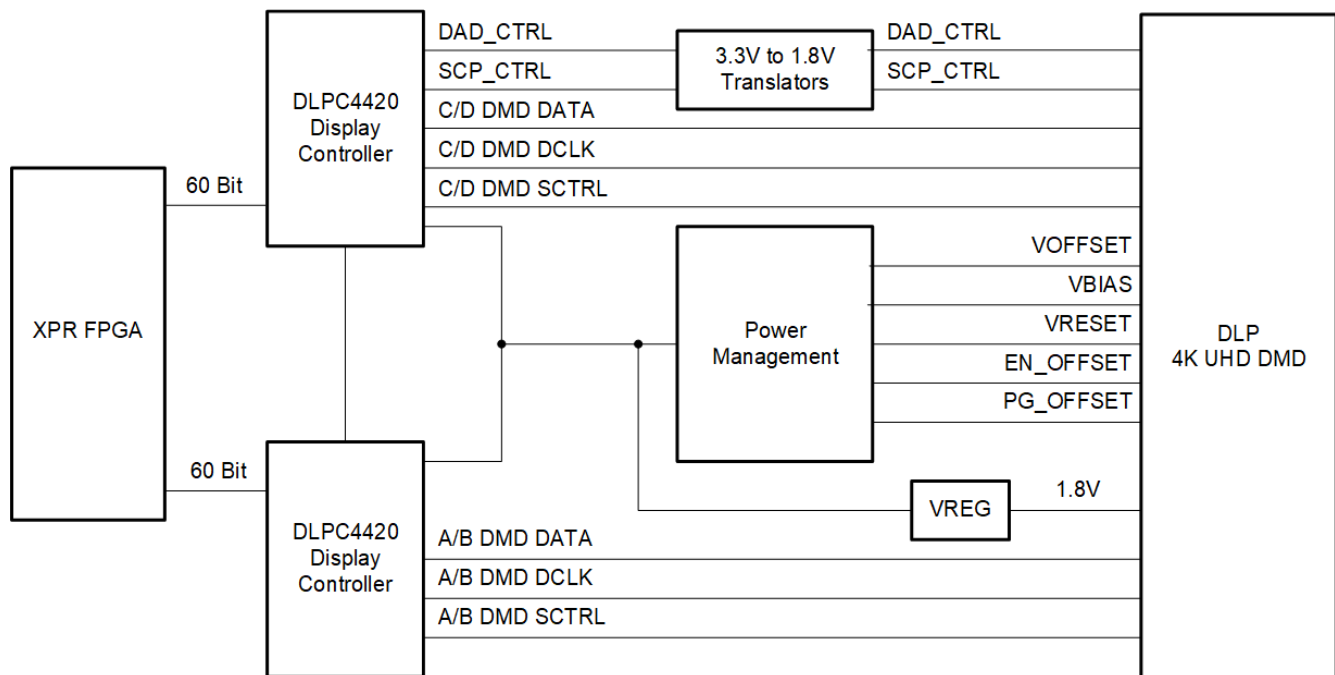
### 3 说明

TI DLP470TE [数字微镜器件 \(DMD\)](#) 是一款数控微机电系统 (MEM) 空间光调制器 (SLM)，可用于实现明亮的全 4K UHD 显示解决方案。与适当的光学系统配合使用时，DLP470TE DMD 可以显示[真正的 4K 超高清分辨率](#) (屏幕像素超过 800 万像素)，并且能够向各种显示介质投射准确且清晰的图像。DLP470TE DMD 通过与 [DLPC4420 显示控制器](#)、[DLPA100 控制器电源和电机驱动器](#) 配合使用，可实现高性能系统，而且非常适合采用更小封装的 [4K UHD 高亮度显示应用](#)。

#### 器件信息

器件型号	封装 <sup>(1)</sup>	封装尺寸 (标称值)
DLP470TE	FXJ (257)	32.2mm × 22.3mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



DLP470TE 简化应用



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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (June 2022) to Revision B (September 2022)	Page
• 将控制器更改为 DLPC4420，将芯片组元件链接到产品页面.....	1
• 将控制器更改为 DLPC4420，更新了应用图.....	1
• Changed the controller to DLPC4420, added the lamp illumination section.....	11
• Added the DMD efficiency specification.....	22
• Changed the controller to DLPC4420.....	24
• Changed the controller to DLPC4420.....	25
• Changed the controller to DLPC4420, added a table with legacy part numbers and mechanical ICD.....	30
• Changed the controller to DLPC4420, updated the application diagrams.....	30
• Changed the controller to DLPC4420.....	31
• Changed the controller to DLPC4420.....	32
• Changed the controller to DLPC4420.....	32
• Changed the controller to DLPC4420.....	37
• Changed the controller to DLPC4420, updated the link.....	40

Changes from Revision * (April 2019) to Revision A (June 2022)	Page
• 根据最新的德州仪器 (TI) 和行业数据表标准对本文档进行了更新.....	1
• Updated <a href="#">SCP Specifications</a> .....	16
• Updated <a href="#">图 6-3</a> .....	18

### 5 Pin Configuration and Functions

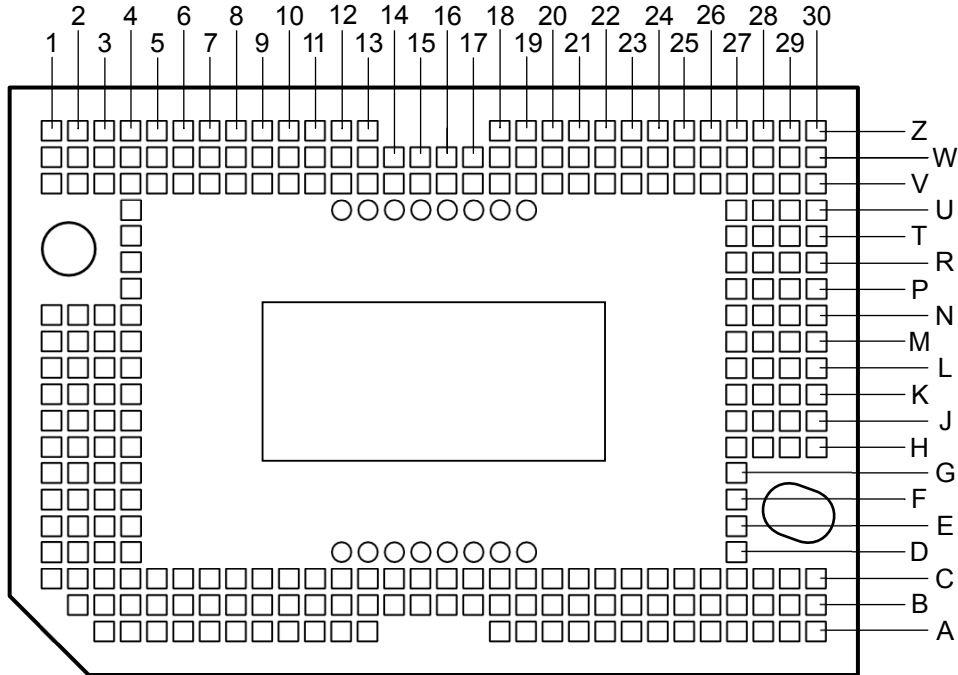


图 5-1. Series 410 Package. 257-pin FXJ. Bottom View.

**CAUTION**

To ensure reliable, long-term operation of the .47-inch 4K UHD S410 DMD, it is critical to properly manage the layout and operation of the signals identified in the table below. For specific details and guidelines, refer to the [PCB Design Requirements for TI DLP Standard TRP Digital Micromirror Devices](#) application report before designing the board.

表 5-1. Pin Functions

PIN		I/O <sup>(1)</sup>	SIGNAL	DATA RATE	INTERNAL TERMINATION	DESCRIPTION	TRACE LENGTH (mil)
NAME	NO.						
D_AN(0)	C6	I	LVDS	DDR	Differential	Data negative	805.0
D_AN(1)	C3						
D_AN(2)	E1						
D_AN(3)	C4						
D_AN(4)	D1						
D_AN(5)	B8						
D_AN(6)	F4						
D_AN(7)	E3						
D_AN(8)	C11						
D_AN(9)	F3						
D_AN(10)	K4						
D_AN(11)	H3						
D_AN(12)	J3						
D_AN(13)	C13						
D_AN(14)	A5						
D_AN(15)	A3						

表 5-1. Pin Functions (continued)

PIN		I/O <sup>(1)</sup>	SIGNAL	DATA RATE	INTERNAL TERMINATION	DESCRIPTION	TRACE LENGTH (mil)
NAME	NO.						
D_AP(0)	C7	I	LVDS	DDR	Differential	Data positive	805.0
D_AP(1)	C2						
D_AP(2)	E2						
D_AP(3)	B4						
D_AP(4)	C1						
D_AP(5)	B7						
D_AP(6)	E4						
D_AP(7)	D3						
D_AP(8)	C12						
D_AP(9)	F2						
D_AP(10)	J4						
D_AP(11)	G3						
D_AP(12)	J2						
D_AP(13)	C14						
D_AP(14)	A6						
D_AP(15)	A4						
D_BN(0)	N4	I	LVDS	DDR	Differential	Data negative	805.0
D_BN(1)	Z11						
D_BN(2)	W4						
D_BN(3)	W10						
D_BN(4)	L1						
D_BN(5)	V8						
D_BN(6)	W6						
D_BN(7)	M1						
D_BN(8)	R4						
D_BN(9)	W1						
D_BN(10)	U4						
D_BN(11)	V2						
D_BN(12)	Z5						
D_BN(13)	N3						
D_BN(14)	Z2						
D_BN(15)	L4						

**表 5-1. Pin Functions (continued)**

PIN		I/O <sup>(1)</sup>	SIGNAL	DATA RATE	INTERNAL TERMINATION	DESCRIPTION	TRACE LENGTH (mil)
NAME	NO.						
D_BP(0)	M4	I	LVDS	DDR	Differential	Data positive	805.0
D_BP(1)	Z12						
D_BP(2)	Z4						
D_BP(3)	Z10						
D_BP(4)	L2						
D_BP(5)	V9						
D_BP(6)	W7						
D_BP(7)	N1						
D_BP(8)	P4						
D_BP(9)	V1						
D_BP(10)	T4						
D_BP(11)	V3						
D_BP(12)	Z6						
D_BP(13)	N2						
D_BP(14)	Z3						
D_BP(15)	L3						
D_CN(0)	H27	I	LVDS	DDR	Differential	Data negative	805.0
D_CN(1)	A20						
D_CN(2)	H28						
D_CN(3)	K28						
D_CN(4)	K30						
D_CN(5)	C23						
D_CN(6)	G27						
D_CN(7)	J30						
D_CN(8)	B24						
D_CN(9)	A21						
D_CN(10)	A27						
D_CN(11)	C29						
D_CN(12)	A26						
D_CN(13)	C25						
D_CN(14)	A29						
D_CN(15)	C30						

表 5-1. Pin Functions (continued)

PIN		I/O <sup>(1)</sup>	SIGNAL	DATA RATE	INTERNAL TERMINATION	DESCRIPTION	TRACE LENGTH (mil)
NAME	NO.						
D_CP(0)	J27	I	LVDS	DDR	Differential	Data positive	805.0
D_CP(1)	A19						
D_CP(2)	H29						
D_CP(3)	K27						
D_CP(4)	K29						
D_CP(5)	C22						
D_CP(6)	F27						
D_CP(7)	H30						
D_CP(8)	B25						
D_CP(9)	B21						
D_CP(10)	B27						
D_CP(11)	C28						
D_CP(12)	A25						
D_CP(13)	C24						
D_CP(14)	A28						
D_CP(15)	B30						
D_DN(0)	V25	I	LVDS	DDR	Differential	Data negative	805.0
D_DN(1)	V28						
D_DN(2)	T30						
D_DN(3)	V27						
D_DN(4)	U30						
D_DN(5)	W23						
D_DN(6)	R27						
D_DN(7)	T28						
D_DN(8)	V20						
D_DN(9)	R28						
D_DN(10)	L27						
D_DN(11)	N28						
D_DN(12)	M28						
D_DN(13)	V18						
D_DN(14)	Z26						
D_DN(15)	Z28						

**表 5-1. Pin Functions (continued)**

PIN		I/O <sup>(1)</sup>	SIGNAL	DATA RATE	INTERNAL TERMINATION	DESCRIPTION	TRACE LENGTH (mil)
NAME	NO.						
D_DP(0)	V24	I	LVDS	DDR	Differential	Data positive	805.0
D_DP(1)	V29						
D_DP(2)	T29						
D_DP(3)	W27						
D_DP(4)	V30						
D_DP(5)	W24						
D_DP(6)	T27						
D_DP(7)	U28						
D_DP(8)	V19						
D_DP(9)	R29						
D_DP(10)	M27						
D_DP(11)	P28						
D_DP(12)	M29						
D_DP(13)	V17						
D_DP(14)	Z25						
D_DP(15)	Z27						
SCTRL_AN	G1	I	LVDS	DDR	Differential	Serial control negative <sup>(2)</sup>	805.0
SCTRL_AP	F1	I	LVDS	DDR	Differential	Serial control negative <sup>(2)</sup>	805.0
SCTRL_BN	V5	I	LVDS	DDR	Differential	Serial control negative <sup>(2)</sup>	805.0
SCTRL_BP	V4	I	LVDS	DDR	Differential	Serial control negative <sup>(2)</sup>	805.0
SCTRL_CN	C26	I	LVDS	DDR	Differential	Serial control negative <sup>(2)</sup>	805.0
SCTRL_CP	C27	I	LVDS	DDR	Differential	Serial control positive <sup>(2)</sup>	805.0
SCTRL_DN	P30	I	LVDS	DDR	Differential	Serial control negative <sup>(2)</sup>	805.0
SCTRL_DP	R30	I	LVDS	DDR	Differential	Serial control positive <sup>(2)</sup>	805.0
DCLK_AN	H2	I	LVDS		Differential	Clock negative <sup>(2)</sup>	805.0
DCLK_AP	H1	I	LVDS		Differential	Clock positive <sup>(2)</sup>	805.0
DCLK_BN	V6	I	LVDS		Differential	Clock negative <sup>(2)</sup>	805.0
DCLK_BP	V7	I	LVDS		Differential	Clock positive <sup>(2)</sup>	805.0
DCLK_CN	D27	I	LVDS		Differential	Clock negative <sup>(2)</sup>	805.0
DCLK_CP	E27	I	LVDS		Differential	Clock positive <sup>(2)</sup>	805.0
DCLK_DN	N29	I	LVDS		Differential	Clock negative <sup>(2)</sup>	805.0
DCLK_DP	N30	I	LVDS		Differential	Clock positive <sup>(2)</sup>	805.0
SCPCLK	A10	I	LVC MOS		Pulldown	Serial communications port clock. Active only when SCPENZ is logic low <sup>(2)</sup>	
SCPDI	A12	I	LVC MOS	SDR	Pulldown	Serial communications port data input. Synchronous to SCPCLK rising edge <sup>(2)</sup>	
SCPENZ	C10	I	LVC MOS		Pulldown	Serial communications port enable active low <sup>(2)</sup>	
SCPDO	A11	O	LVC MOS	SDR		Serial communications port output	
RESET_ADDR(0)	Z13	I	LVC MOS		Pulldown	Reset driver address select <sup>(2)</sup>	
RESET_ADDR(1)	W13						
RESET_ADDR(2)	V10						
RESET_ADDR(3)	W14						

表 5-1. Pin Functions (continued)

PIN		I/O <sup>(1)</sup>	SIGNAL	DATA RATE	INTERNAL TERMINATION	DESCRIPTION	TRACE LENGTH (mil)
NAME	NO.						
RESET_MODE(0)	W9	I	LVCMOS		Pulldown	Reset driver mode select <sup>(2)</sup>	
RESET_SEL(0)	V14					Reset driver level select <sup>(2)</sup>	
RESET_SEL(1)	Z8					Reset driver level select <sup>(2)</sup>	
RESET_STROBE	Z9	I	LVCMOS		Pulldown	Rising edge latches in RESET_ADDR, RESET_MODE, and RESET_SEL. <sup>(2)</sup>	
PWRDNZ	A8	I	LVCMOS		Pulldown	Active low device reset. <sup>(2)</sup>	
RESET_OEZ	W15	I	LVCMOS		Pullup	Active low output enable for internal reset driver circuits. <sup>(2)</sup>	
RESET_IRQZ	V16	O	LVCMOS			Active low output interrupt to the DLP® display controller	
EN_OFFSET	C9	O	LVCMOS			Active high enable for external V <sub>OFFSET</sub> regulator	
PG_OFFSET	A9	I	LVCMOS		Pullup	Active low fault from external V <sub>OFFSET</sub> regulator <sup>(2)</sup>	
TEMP_N	B18		Analog			Temperature sensor diode cathode	
TEMP_P	B17		Analog			Temperature sensor diode anode	
RESERVED **MUST VERIFY WITH SRC DATA SHEET	D12, D13, D14, D15, D16, D17, D18, D19, U12, U13, U14, U15	NC	Analog		Pulldown	Do not connect on the DLP® system board. No connect. No electrical connections from CMOS bond pad to package pin	
No Connect	U16, U17, U18, U19	NC				No connect. No electrical connection from the CMOS bond pad to package pin	
RESERVED_BA	W11	O	LVCMOS			Do not connect on the DLP system board.	
RESERVED_BB	B11						
RESERVED_BC	Z20						
RESERVED_BD	C18						
RESERVED_PFE	A18	I	LVCMOS		Pulldown	Connect to ground on the DLP system board.	
RESERVED_TM	C8	I	Analog			Do not connect on the DLP system board.	
RESERVED_TP0	Z19						
RESERVED_TP1	W20						
RESERVED_TP2	W19						
V <sub>BIAS</sub> <sup>(3)</sup>	C15, C16, V11, V12	P	Analog			Supply voltage for positive bias level of micromirror reset signal	
V <sub>RESET</sub> <sup>(3)</sup>	G4, H4, J1, K1	P	Analog			Supply voltage for negative reset level of micromirror reset signal	
V <sub>OFFSET</sub> <sup>(3)</sup>	A30, B2, M30, Z1, Z30	P	Analog			Supply voltage for HVCMOS logic. Supply voltage for positive offset level of micromirror reset signal. Supply voltage for stepped high voltage at micromirror address electrodes	



**表 5-1. Pin Functions (continued)**

PIN		I/O <sup>(1)</sup>	SIGNAL	DATA RATE	INTERNAL TERMINATION	DESCRIPTION	TRACE LENGTH (mil)
NAME	NO.						
$V_{CC}$ <sup>(3)</sup>	A24, A7, B10, B13, B16, B19, B22, B28, B5, C17, C20, D4, J29, K2, L29, M2, N27, U27, V13, V15, V22, W17, W21, W26, W29, W3, Z18, Z23, Z29, Z7	P	Analog			Supply voltage for LVCMOS core. Supply voltage for positive offset level of micromirror reset signal during power down. Supply voltage for normal high level at micromirror address electrodes	
$V_{SS}$ <sup>(4)</sup>	A13, A22, A23, B12, B14, B15, B20, B23, B26, B29, B3, B6, B9, C19, C21, C5, D2, G2, J28, K3, L28, L30, M3, P27, P29, U29, V21, V23, V26, W12, W16, W18, W2, W22, W25, W28, W30, W5, W8, Z21, Z22, Z24	G				Device ground. Common return for all power	

- (1) I = Input, O = Output, P = Power, G = Ground, NC = No connect
- (2) These signals are very sensible to noise or intermittent power connections, which can cause irreversible DMD micromirror array damage or, to a lesser extent, image disruption. Consider this precaution during DMD board design and manufacturer handling of the DMD subassemblies.
- (3)  $V_{BIAS}$ ,  $V_{CC}$ ,  $V_{OFFSET}$ , and  $V_{RESET}$  power supplies must be connected for proper DMD operation.
- (4)  $V_{SS}$  must be connected for proper DMD operation.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted). Stresses beyond those listed under [节 6.1](#) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device is not implied at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#). Exposure above or below the [Recommended Operating Conditions](#). Exposure above or below the [Recommended Operating Conditions](#) for extended periods may affect device reliability.

		MIN	MAX	UNIT
<b>SUPPLY VOLTAGES</b>				
$V_{CC}$	Supply voltage for LVCMOS core logic <sup>(1)</sup>	- 0.5	2.3	V
$V_{OFFSET}$	Supply voltage for HVCMOS and micromirror electrode <sup>(1) (2)</sup>	- 0.5	11	V
$V_{BIAS}$	Supply voltage for micromirror electrode <sup>(1)</sup>	- 0.5	19	V
$V_{RESET}$	Supply voltage for micromirror electrode <sup>(1)</sup>	- 15	- 0.3	V
$ V_{BIAS} - V_{OFFSET} $	Supply voltage difference (absolute value) <sup>(3)</sup>		11	V
$ V_{BIAS} - V_{RESET} $	Supply voltage difference (absolute value) <sup>(4)</sup>		34	V
<b>INPUT VOLTAGES</b>				
	Input voltage for all other LVCMOS input pins <sup>(1)</sup>	- 0.5	$V_{CC} + 0.5$	V
	Input voltage for all other LVDS input pins <sup>(1) (5)</sup>	- 0.5	$V_{CC} + 0.5$	V
$ V_{ID} $	Input differential voltage (absolute value) <sup>(6)</sup>		500	mV
$I_{ID}$	Input differential current <sup>(5)</sup>		6.3	mA
<b>Clocks</b>				
$f_{CLOCK}$	Clock frequency for LVDS interface, DCLK_A		400	MHz
$f_{CLOCK}$	Clock frequency for LVDS interface, DCLK_B		400	MHz
$f_{CLOCK}$	Clock frequency for LVDS interface, DCLK_C		400	MHz
$f_{CLOCK}$	Clock frequency for LVDS interface, DCLK_D		400	MHz
<b>ENVIRONMENTAL</b>				
$T_{ARRAY}$ and $T_{WINDOW}$	Temperature, operating <sup>(7)</sup>	0	90	°C
	Temperature, non - operating <sup>(7)</sup>	- 40	90	°C
$ T_{DELTA} $	Absolute temperature delta between any point on the window edge and the ceramic test point TP1 <sup>(8)</sup>		30	°C
$T_{DP}$	Dew point temperature, operating and non - operating (non-condensing)		81	°C

- (1) All voltages are referenced to common ground  $V_{SS}$ .  $V_{BIAS}$ ,  $V_{CC}$ ,  $V_{OFFSET}$ , and  $V_{RESET}$  power supplies are all required for proper DMD operation.  $V_{SS}$  must also be connected.
- (2)  $V_{OFFSET}$  supply transients must fall within specified voltages.
- (3) Exceeding the recommended allowable voltage difference between  $V_{BIAS}$  and  $V_{OFFSET}$  may result in excessive current draw.
- (4) Exceeding the recommended allowable voltage difference between  $V_{BIAS}$  and  $V_{RESET}$  may result in excessive current draw.
- (5) LVDS differential inputs must not exceed the specified limit or damage may result to the internal termination resistors.
- (6) This maximum LVDS input voltage rating applies when each input of a differential pair is at the same voltage potential.
- (7) The highest temperature of the active array (as calculated using [Micromirror Array Temperature Calculation](#)) or of any point along the window edge as defined in [图 7-1](#). The locations of thermal test points TP2, TP3, TP4, and TP5 in [图 7-1](#) are intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, use that location.
- (8) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in [图 7-1](#). The window test points TP2, TP3, TP4, and TP5 shown in [图 7-1](#) are intended to result in the worst case delta. If a particular application causes another point on the window edge to result in a larger delta temperature, use that location.

Applicable for the DMD as a component or non-operating in a system.

## 6.2 Storage Conditions

		MIN	MAX	UNIT
T <sub>DMD</sub>	DMD storage temperature	- 40	80	°C
T <sub>DP-AVG</sub>	Average dew point temperature (non-condensing) <sup>(1)</sup>		28	°C
T <sub>DP-ELR</sub>	Elevated dew point temperature range (non-condensing) <sup>(2)</sup>	28	36	°C
CT <sub>ELR</sub>	Cumulative time in elevated dew point temperature range		24	months

- (1) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.  
(2) Limit the exposure to dew point temperatures in the elevated range during storage and operation to less than a total cumulative time of CT<sub>ELR</sub>.

## 6.3 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by this table. No level of performance is implied when operating the device above or below these limits.

## 6.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
<b>VOLTAGE SUPPLY</b>					
V <sub>CC</sub>	LVC MOS logic supply voltage <sup>(1)</sup>	1.65	1.8	1.95	V
V <sub>OFFSET</sub>	Mirror electrode and HVC MOS voltage <sup>(1) (2)</sup>	9.5	10	10.5	V
V <sub>BIAS</sub>	Mirror electrode voltage <sup>(1)</sup>	17.5	18	18.5	V
V <sub>RESET</sub>	Mirror electrode voltage <sup>(1)</sup>	- 14.5	- 14	- 13.5	V
V <sub>BIAS</sub> - V <sub>OFFSET</sub>	Supply voltage difference (absolute value) <sup>(3)</sup>			10.5	V
V <sub>BIAS</sub> - V <sub>RESET</sub>	Supply voltage difference (absolute value) <sup>(4)</sup>			33	V
<b>LVC MOS INTERFACE</b>					
V <sub>IH(DC)</sub>	DC input high voltage <sup>(5)</sup>	0.7 × V <sub>CC</sub>		V <sub>CC</sub> + 0.3	V
V <sub>IL(DC)</sub>	DC input low voltage <sup>(5)</sup>	- 0.3	0.3 × V <sub>CC</sub>		V
V <sub>IH(AC)</sub>	AC input high voltage <sup>(5)</sup>	0.8 × V <sub>CC</sub>		V <sub>CC</sub> + 0.3	V
V <sub>IL(AC)</sub>	AC input low voltage <sup>(5)</sup>	- 0.3	0.2 × V <sub>CC</sub>		V
t <sub>PWRDZ</sub>	PWRDZ pulse duration <sup>(6)</sup>	10			ns
<b>SCP INTERFACE</b>					
f <sub>SCPCLK</sub>	SCP clock frequency <sup>(7)</sup>			500	kHz
t <sub>SCP_PD</sub>	Propagation delay, clock to Q, from rising-edge of SCPCLK to valid SCPDO <sup>(8)</sup>	0		900	ns
t <sub>SCP_NEG_ENZ</sub>	Time between falling-edge of SCPENZ and the first rising-edge of SCPCLK	1			µs
t <sub>SCP_POS_ENZ</sub>	Time between falling-edge of SCPCLK and the rising-edge of SCPENZ	1			µs
t <sub>SCP_DS</sub>	SCPDI clock setup time (before SCPCLK falling edge) <sup>(8)</sup>	800			ns
t <sub>SCP_DH</sub>	SCPDI hold time (after SCPCLK falling edge) <sup>(8)</sup>	900			ns
t <sub>SCP_PW_ENZ</sub>	SCPENZ inactive pulse duration (high level)	2			µs
f <sub>CLOCK</sub>	Clock frequency for LVDS interface (all channels), DCLK <sup>(9)</sup>			400	MHz
V <sub>ID</sub>	Input differential voltage (absolute value) <sup>(10)</sup>	150	300	440	mV

## 6.4 Recommended Operating Conditions (continued)

		MIN	NOM	MAX	UNIT
V <sub>CM</sub>	Common mode voltage <sup>(10)</sup>	1100	1200	1300	mV
V <sub>LVDS</sub>	LVDS voltage <sup>(10)</sup>	880		1520	mV
t <sub>LVDS_RSTZ</sub>	Time required for LVDS receivers to recover from PWRDNZ			2000	ns
Z <sub>IN</sub>	Internal differential termination resistance	80	100	120	Ω
Z <sub>LINE</sub>	Line differential impedance (PWB/trace)	90	100	110	Ω
<b>ENVIRONMENTAL</b>					
T <sub>ARRAY</sub>	Array temperature, long-term operational <sup>(11) (12) (13) (23)</sup>	10		40 to 70 <sup>(23)</sup>	°C
	Array temperature, short-term operational <sup>(12) (15)</sup>	0		10	°C
T <sub>WINDOW</sub>	Window temperature - operational <sup>(16) (17)</sup>			85	°C
T <sub>DELTA</sub>	Absolute temperature delta between any point on the window edge and the ceramic test point TP1 <sup>(18) (19)</sup>			14	°C
T <sub>DP-AVG</sub>	Average dew point temperature (non - condensing) <sup>(20)</sup>			28	°C
T <sub>DP-ELR</sub>	Elevated dew point temperature range (non-condensing) <sup>(21)</sup>	28		36	°C
CT <sub>ELR</sub>	Cumulative time in elevated dew point temperature range			24	months
		MIN	NOM	MAX	UNIT
<b>VOLTAGE SUPPLY</b>					
V <sub>CC</sub>	LVC MOS logic supply voltage <sup>(1)</sup>	1.65	1.8	1.95	V
V <sub>OFFSET</sub>	Mirror electrode and HVCMOS voltage <sup>(1) (2)</sup>	9.5	10	10.5	V
V <sub>BIAS</sub>	Mirror electrode voltage <sup>(1)</sup>	17.5	18	18.5	V
V <sub>RESET</sub>	Mirror electrode voltage <sup>(1)</sup>	- 14.5	- 14	- 13.5	V
V <sub>BIAS</sub> - V <sub>OFFSET</sub>	Supply voltage difference (absolute value) <sup>(3)</sup>			10.5	V
V <sub>BIAS</sub> - V <sub>RESET</sub>	Supply voltage difference (absolute value) <sup>(4)</sup>			33	V
<b>LVC MOS INTERFACE</b>					
V <sub>IH(DC)</sub>	DC input high voltage <sup>(5)</sup>	0.7 × V <sub>CC</sub>		V <sub>CC</sub> + 0.3	V
V <sub>IL(DC)</sub>	DC input low voltage <sup>(5)</sup>	- 0.3		0.3 × V <sub>CC</sub>	V
V <sub>IH(AC)</sub>	AC input high voltage <sup>(5)</sup>	0.8 × V <sub>CC</sub>		V <sub>CC</sub> + 0.3	V
V <sub>IL(AC)</sub>	AC input low voltage <sup>(5)</sup>	- 0.3		0.2 × V <sub>CC</sub>	V
t <sub>PWRDNZ</sub>	PWRDNZ pulse duration <sup>(6)</sup>	10			ns
<b>SCP INTERFACE</b>					
f <sub>SCPCLK</sub>	SCP clock frequency <sup>(7)</sup>			500	kHz
t <sub>SCP_PD</sub>	Propagation delay, Clock to Q, from rising - edge of SCPCLK to valid SCPDO <sup>(8)</sup>	0		900	ns

## 6.4 Recommended Operating Conditions (continued)

		MIN	NOM	MAX	UNIT
t <sub>SCP_NEG_ENZ</sub>	Time between falling-edge of SCPENZ and the first rising- edge of SCPCLK	1			μs
t <sub>SCP_POS_ENZ</sub>	Time between falling-edge of SCPCLK and the rising-edge of SCPENZ	1			μs
t <sub>SCP_DS</sub>	SCPDI Clock setup time (before SCPCLK falling edge) <sup>(8)</sup>	800			ns
t <sub>SCP_DH</sub>	SCPDI Hold time (after SCPCLK falling edge) <sup>(8)</sup>	900			ns
t <sub>SCP_PW_ENZ</sub>	SCPENZ inactive pulse duration (high level)	2			μs
<b>LVDS INTERFACE</b>					
f <sub>CLOCK</sub>	Clock frequency for LVDS interface (all channels), DCLK <sup>(10)</sup>			400	MHz
V <sub>ID</sub>	Input differential voltage (absolute value) <sup>(11)</sup>	150	300	440	mV
V <sub>CM</sub>	Common mode voltage <sup>(11)</sup>	1100	1200	1300	mV
V <sub>LVDS</sub>	LVDS voltage <sup>(11)</sup>	880		1520	mV
t <sub>LVDS_RSTZ</sub>	Time required for LVDS receivers to recover from PWRDNZ			2000	ns
Z <sub>IN</sub>	Internal differential termination resistance	80	100	120	Ω
Z <sub>LINE</sub>	Line differential impedance (PWB/trace)	90	100	110	Ω
<b>ENVIRONMENTAL</b>					
T <sub>ARRAY</sub>	Array temperature, long - term operational <sup>(13) (14) (16)</sup>	10		40 to 70 <sup>(15)</sup>	°C
	Array temperature, short - term operational <sup>(14) (17)</sup>	0		10	°C
T <sub>WINDOW</sub>	Window temperature - operational <sup>(21) (23)</sup>			85	°C
T <sub>DELTA</sub>	Absolute temperature delta between any point on the window edge and the ceramic test point TP1 <sup>(18) (19)</sup>			14	°C
T <sub>DP -AVG</sub>	Average dew point temperature (non-condensing) <sup>(20)</sup>			28	°C
T <sub>DP -ELR</sub>	Elevated dew point temperature range (non-condensing) <sup>(22)</sup>	28		36	°C
CT <sub>ELR</sub>	Cumulative time in elevated dew point temperature range			24	Months
<b>ILLUMINATION (Lamp)</b>					
L	Operating system luminance <sup>(19)</sup>			4000	lm
ILL <sub>UV</sub>	Illumination wavelengths < 395 nm <sup>(13)</sup>	0.68		2.00	mW/cm <sup>2</sup>
ILL <sub>VIS</sub>	Illumination wavelengths between 395 nm and 800 nm	Thermally limited			mW/cm <sup>2</sup>
ILL <sub>IR</sub>	Illumination wavelengths > 800 nm			10	mW/cm <sup>2</sup>
ILL <sub>θ</sub>	Illumination marginal ray angle <sup>(23)</sup>			55	deg
<b>ILLUMINATION (Solid State)</b>					
L	Operating system luminance <sup>(19)</sup>			5500	lm
ILL <sub>UV</sub>	Illumination wavelengths < 436 nm <sup>(13)</sup>			0.45	mW/cm <sup>2</sup>
ILL <sub>VIS</sub>	Illumination wavelengths between 436 nm and 800 nm	Thermally Limited			mW/cm <sup>2</sup>
ILL <sub>IR</sub>	Illumination wavelengths > 800 nm			10	mW/cm <sup>2</sup>
ILL <sub>θ</sub>	Illumination marginal ray angle <sup>(23)</sup>			55	deg

- (1) All voltages are referenced to common ground V<sub>SS</sub>. V<sub>BIAS</sub>, V<sub>CC</sub>, V<sub>OFFSET</sub>, and V<sub>RESET</sub> power supplies are all required for proper DMD operation. V<sub>SS</sub> must also be connected.
- (2) V<sub>OFFSET</sub> supply transients must fall within specified max voltages.
- (3) To prevent excess current, the supply voltage difference |V<sub>BIAS</sub> - V<sub>OFFSET</sub>| must be less than the specified limit. See [Power Supply Recommendations](#), 图 9-1, and 表 9-1.
- (4) To prevent excess current, the supply voltage difference |V<sub>BIAS</sub> - V<sub>RESET</sub>| must be less than the specified limit. See [Power Supply Recommendations](#), 图 9-1, and 表 9-1.
- (5) Low-speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, "Low-Power Double Data Rate (LPDDR)" JESD209B. Tester conditions for V<sub>IH</sub> and V<sub>IL</sub>.
  - Frequency = 60 MHz. Maximum rise time = 2.5 ns at 20/80
  - Frequency = 60 MHz. Maximum fall time = 2.5 ns at 80/20
- (6) PWRDNZ input pin resets the SCP and disables the LVDS receivers. PWRDNZ input pin overrides SCPENZ input pin and tristates the SCPDO output pin.

- (7) The SCP clock is a gated clock. Duty cycle must be  $50\% \pm 10\%$ . SCP parameter is related to the frequency of DCLK.
- (8) See [图 6-2](#).
- (9) See LVDS timing requirements in [Timing Requirements](#).
- (10) See LVDS waveform requirements in the specifications.
- (11) Simultaneous exposure of the DMD to the maximum [Recommended Operating Conditions](#) for temperature and UV illumination reduces device lifetime.
- (12) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1) shown in [图 7-1](#) and the package thermal resistance ([Thermal Information](#)) using the [Micromirror Array Temperature Calculation](#).
- (13) Long-term is defined as the usable life of the device.
- (14) CP internal oscillator is specified to operate all SCP registers. For all SCP operations, DCLK is required.
- (15) Array temperatures beyond those specified as long-term are recommended for short-term conditions only (power-up). Short-term is defined as the cumulative time over the usable life of the device and is less than 500 hours.
- (16) The locations of thermal test points TP2, TP3, TP4, and TP5 in [Figure 10](#) are intended to measure the highest window edge temperature. For most applications, the locations shown are representative of the highest window edge temperature. If a particular application causes additional points on the window edge to be at a higher temperature, use that location.
- (17) The maximum marginal ray angle of the incoming illumination light at any point in the micromirror array, including the pond of micromirrors (POM), cannot exceed 55 degrees from the normal to the device array plane. The device window aperture has not necessarily been designed to allow incoming light at higher maximum angles to pass to the micromirrors, and the device performance has not been tested nor qualified at angles exceeding this. Illumination light exceeding this angle outside the micromirror array (including POM) will contribute to thermal limitations described in this document, and may negatively affect lifetime.
- (18) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in [图 7-1](#). The window test points TP2, TP3, TP4, and TP5 shown in [图 7-1](#) are intended to result in the worst case delta temperature. If a particular application causes another point on the window edge to result in a larger delta in temperature, that point needs to be used.
- (19) DMD is qualified at the combination of the maximum temperature and maximum lumens specified. Operation of the DMD outside of these limits has not been tested.
- (20) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
- (21) Limit exposure to dew point temperatures in the elevated range during storage and operation to less than a total cumulative time of  $CT_{ELR}$ .
- (22) Supported for video applications only
- (23) Per the [Maximum Recommended Array Temperature - Derating Curve](#), the maximum operational array temperature is derated based on the micromirror landed duty cycle that the DMD experiences in the end application. See [Micromirror Landed-On/Landed-Off Duty Cycle](#) for a definition of micromirror landed duty cycle.

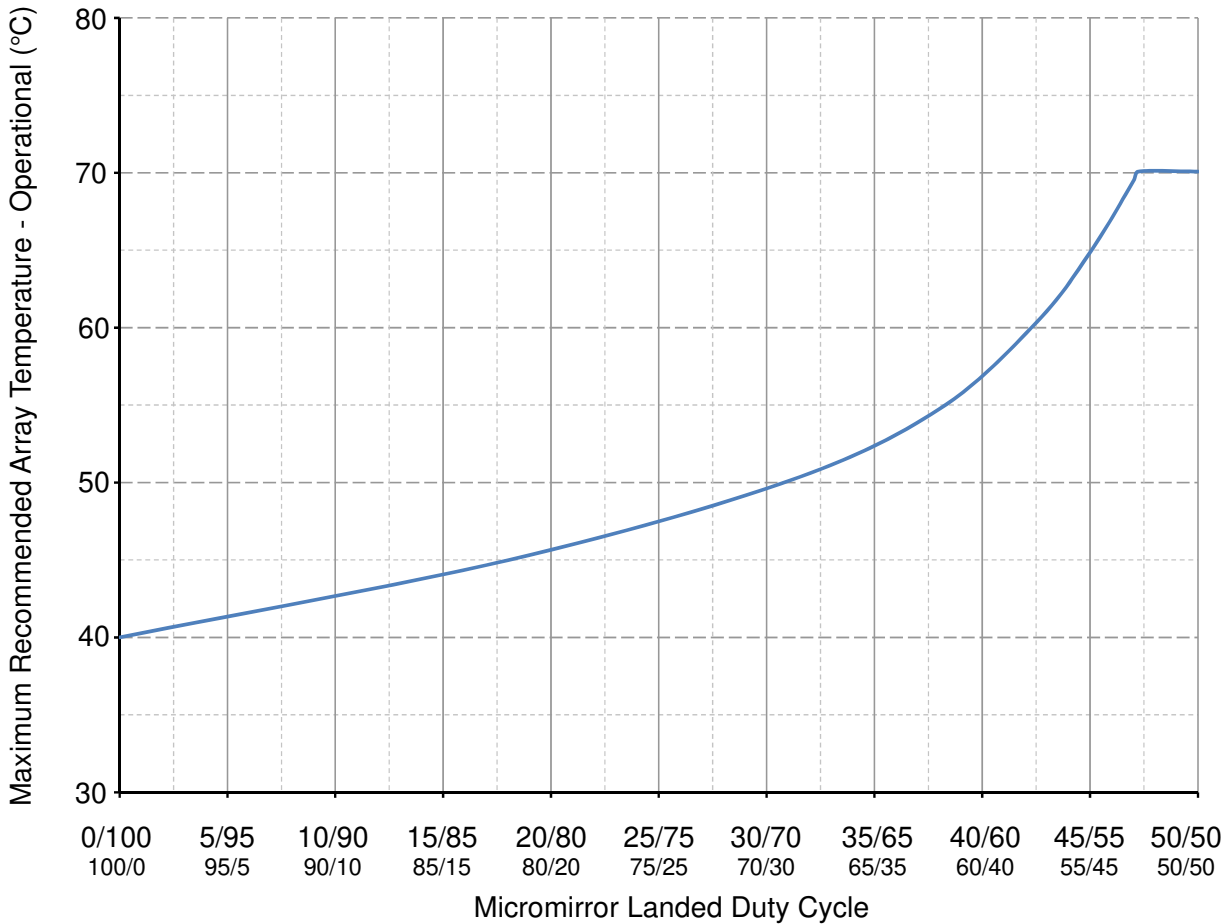


图 6-1. Maximum Recommended Array Temperature - Derating Curve

## 6.5 Thermal Information

THERMAL METRIC	DLP470TE	UNIT
	FXJ Package	
	257 PINS	
Thermal resistance, active area to test point 1 (TP1) <sup>(1)</sup>	0.90	°C/W

- (1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package where it can be removed by an appropriate heat sink. The heat sink and cooling system must be capable of maintaining the package within the temperature range specified in the [Recommended Operating Conditions](#).  
The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array.  
Optical systems need to be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

Over operating free-air temperature range (unless otherwise noted).

## 6.6 Electrical Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>OH</sub>	High level output voltage V <sub>CC</sub> = 1.8 V, I <sub>OH</sub> = - 2 mA	0.8 × V <sub>CC</sub>			V
V <sub>OL</sub>	Low level output voltage V <sub>CC</sub> = 1.95 V, I <sub>OL</sub> = 2 mA			0.2 × V <sub>CC</sub>	V
I <sub>OZ</sub>	High impedance output current V <sub>CC</sub> = 1.95 V	- 40		25	μA
I <sub>IL</sub>	Low level input current V <sub>CC</sub> = 1.95 V, V <sub>I</sub> = 0	- 1			μA

## 6.6 Electrical Characteristics (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{IH}$	High level input current <sup>(1)</sup>	$V_{CC} = 1.95\text{ V}$ , $V_I = V_{CC}$			110	$\mu\text{A}$
$I_{CC}$	Supply current $V_{CC}$ <sup>(2)</sup>	$V_{CC} = 1.95\text{ V}$			1500	mA
$I_{OFFSET}$	Supply current $V_{OFFSET}$ <sup>(3)</sup>	$V_{OFFSET} = 10.5\text{ V}$			13.2	mA
$I_{BIAS}$	Supply current $V_{BIAS}$ <sup>(3) (4)</sup>	$V_{BIAS} = 18.5\text{ V}$			3.6	mA
$I_{RESET}$	Supply current $V_{RESET}$ <sup>(4)</sup>	$V_{RESET} = -14.5\text{ V}$			-9	mA
$P_{CC}$	Supply power dissipation $V_{CC}$	$V_{CC} = 1.95\text{ V}$			2925.0	mW
$P_{OFFSET}$	Supply power dissipation $V_{OFFSET}$ <sup>(3)</sup>	$V_{OFFSET} = 10.5\text{ V}$			138.6	mW
$P_{BIAS}$	Supply power dissipation $V_{BIAS}$ <sup>(3) (4)</sup>	$V_{BIAS} = 18.5\text{ V}$			66.6	mW
$P_{RESET}$	Supply power dissipation $V_{RESET}$ <sup>(4)</sup>	$V_{RESET} = -14.5\text{ V}$			130.5	mW
$P_{TOTAL}$	Supply power dissipation $V_{TOTAL}$				3260.7	mW

(1) Applies to LVCMOS pins only. Excludes LVDS pins and MBRST (15:0) pins.

(2) See the Pin Functions table for pull - up and pull - down configuration per device pin.

(3) To prevent excess current, the supply voltage difference  $|V_{BIAS} - V_{OFFSET}|$  must be less than the specified limits listed in the [Recommended Operating Conditions](#) table.

(4) To prevent excess current, the supply voltage difference  $|V_{BIAS} - V_{RESET}|$  must be less than specified limit in [Recommended Operating Conditions](#).

## 6.7 Capacitance at Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{I_{lvds}}$	LVDS input capacitance 2xLVDS	$f = 1\text{ MHz}$			20	pF
$C_{I_{nonlvds}}$	Non-LVDS input capacitance 2xLVDS	$f = 1\text{ MHz}$			20	pF
$C_{I_{tdiode}}$	Temperature diode input capacitance 2xLVDS	$f = 1\text{ MHz}$			30	pF
$C_O$	Output capacitance	$f = 1\text{ MHz}$			20	pF

## 6.8 Timing Requirements

			MIN	NOM	MAX	UNIT
<b>SCP<sup>(1)</sup></b>						
$t_r$	Rise time	20% to 80% reference points			30	ns
$t_f$	Fall time	80% to 20% reference points			30	ns
<b>LVDS<sup>(2)</sup></b>						
$t_r$	Rise slew rate	20% to 80% reference points	0.7	1		V/ns
$t_f$	Fall slew rate	80% to 20% reference points	0.7	1		V/ns
$t_c$	Clock cycle	DCLK_A, LVDS pair	2.5			ns
		DCLK_B, LVDS pair	2.5			ns
		DCLK_C, LVDS pair	2.5			ns
		DCLK_D, LVDS pair	2.5			ns
$t_w$	Pulse duration	DCLK_A, LVDS pair	1.19	1.25		ns
		DCLK_B, LVDS pair	1.19	1.25		ns
		DCLK_C, LVDS pair	1.19	1.25		ns
		DCLK_D, LVDS pair	1.19	1.25		ns

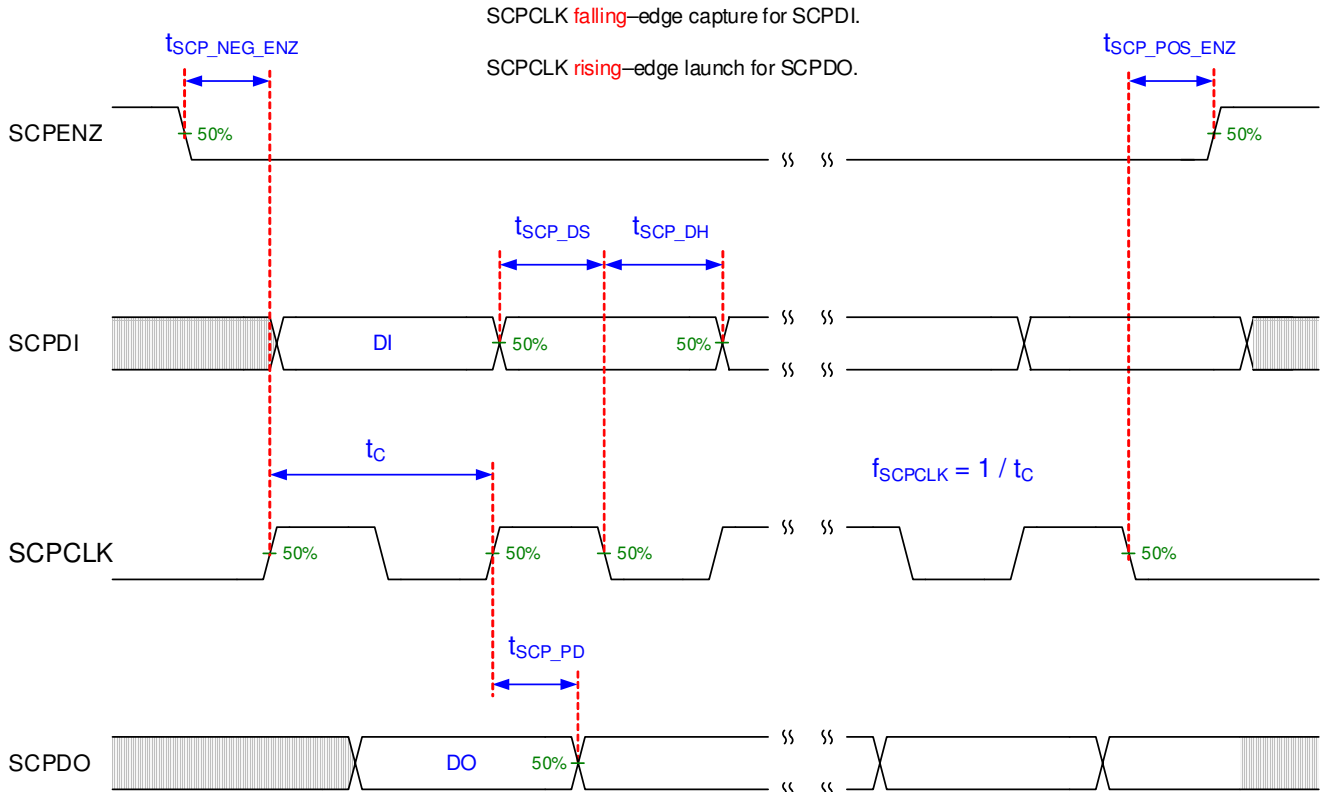


## 6.8 Timing Requirements (continued)

		MIN	NOM	MAX	UNIT	
t <sub>Su</sub>	Setup time	D_A(15:0) before DCLK_A, LVDS pair	0.275		ns	
		D_B(15:0) before DCLK_B, LVDS pair	0.275		ns	
		D_C(15:0) before DCLK_C, LVDS pair	0.275		ns	
		D_D(15:0) before DCLK_D, LVDS pair	0.275		ns	
		SCTRL_A before DCLK_A, LVDS pair	0.275		ns	
		SCTRL_B before DCLK_B, LVDS pair	0.275		ns	
		SCTRL_C before DCLK_C, LVDS pair	0.275		ns	
		SCTRL_D before DCLK_D, LVDS pair	0.275		ns	
t <sub>h</sub>	Hold time	D_A(15:0) after DCLK_A, LVDS pair	0.195		ns	
		D_B(15:0) after DCLK_B, LVDS pair	0.195		ns	
		D_C(15:0) after DCLK_C, LVDS pair	0.195		ns	
		D_D(15:0) after DCLK_D, LVDS pair	0.195		ns	
		SCTRL_A after DCLK_A, LVDS pair	0.195		ns	
		SCTRL_B after DCLK_B, LVDS pair	0.195		ns	
		SCTRL_C after DCLK_C, LVDS pair	0.195		ns	
		SCTRL_D after DCLK_D, LVDS pair	0.195		ns	
t <sub>SKEW</sub>	Skew time	Channel B relative to channel A <sup>(3)</sup> <sup>(4)</sup>		- 1.25	1.25	ns
t <sub>SKEW</sub>	Skew time	Channel D relative to channel C <sup>(5)</sup> <sup>(6)</sup> , LVDS pair		- 1.25	1.25	ns

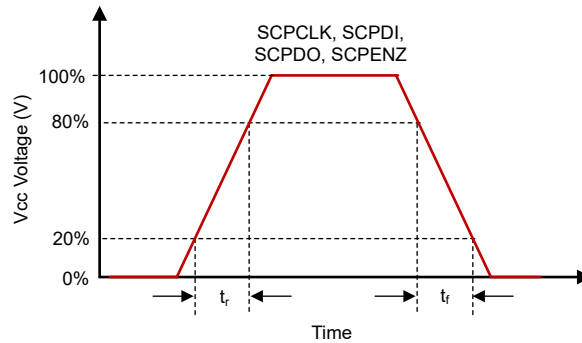
- (1) See the specifications for rise time and fall time for SCP.
- (2) See the specifications the for timing requirements for LVDS.
- (3) Channel A (Bus A) includes the following LVDS pairs: DCLK\_AN and DCLK\_AP, SCTRL\_AN and SCTRL\_AP, D\_AN(15:0) and D\_AP(15:0).
- (4) Channel B (Bus B) includes the following LVDS pairs: DCLK\_BN and DCLK\_BP, SCTRL\_BN and SCTRL\_BP, D\_BN(15:0) and D\_BP(15:0).
- (5) Channel C (Bus C) includes the following LVDS pairs: DCLK\_CN and DCLK\_CP, SCTRL\_CN and SCTRL\_CP, D\_CN(15:0) and D\_CP(15:0).
- (6) Channel D (Bus D) includes the following LVDS pairs: DCLK\_DN and DCLK\_DP, SCTRL\_DN and SCTRL\_DP, D\_DN(15:0) and D\_DP(15:0).

### 6.8.1 Timing Diagrams



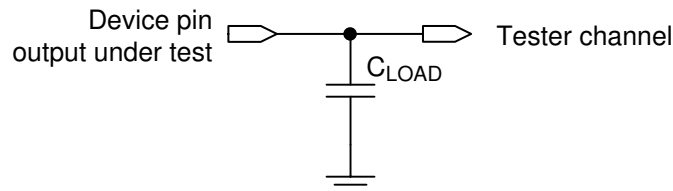
See *Recommended Operating Conditions* for  $f_{SCPCLK}$ ,  $t_{SCP\_DS}$ ,  $t_{SCP\_DH}$  and  $t_{SCP\_PD}$  specifications.

图 6-2. SCP Timing Requirements



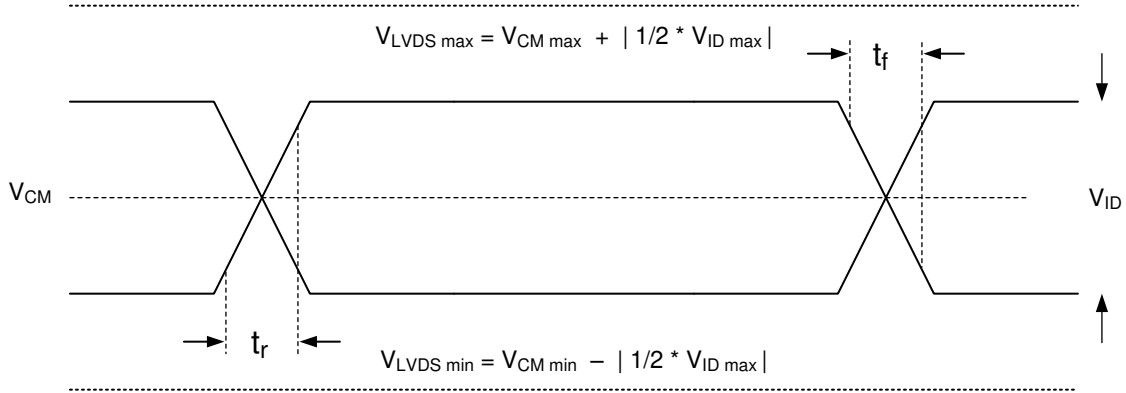
See *Timing Diagrams* for  $t_r$  and  $t_f$  specifications and conditions.

图 6-3. SCP Requirements for Rise and Fall



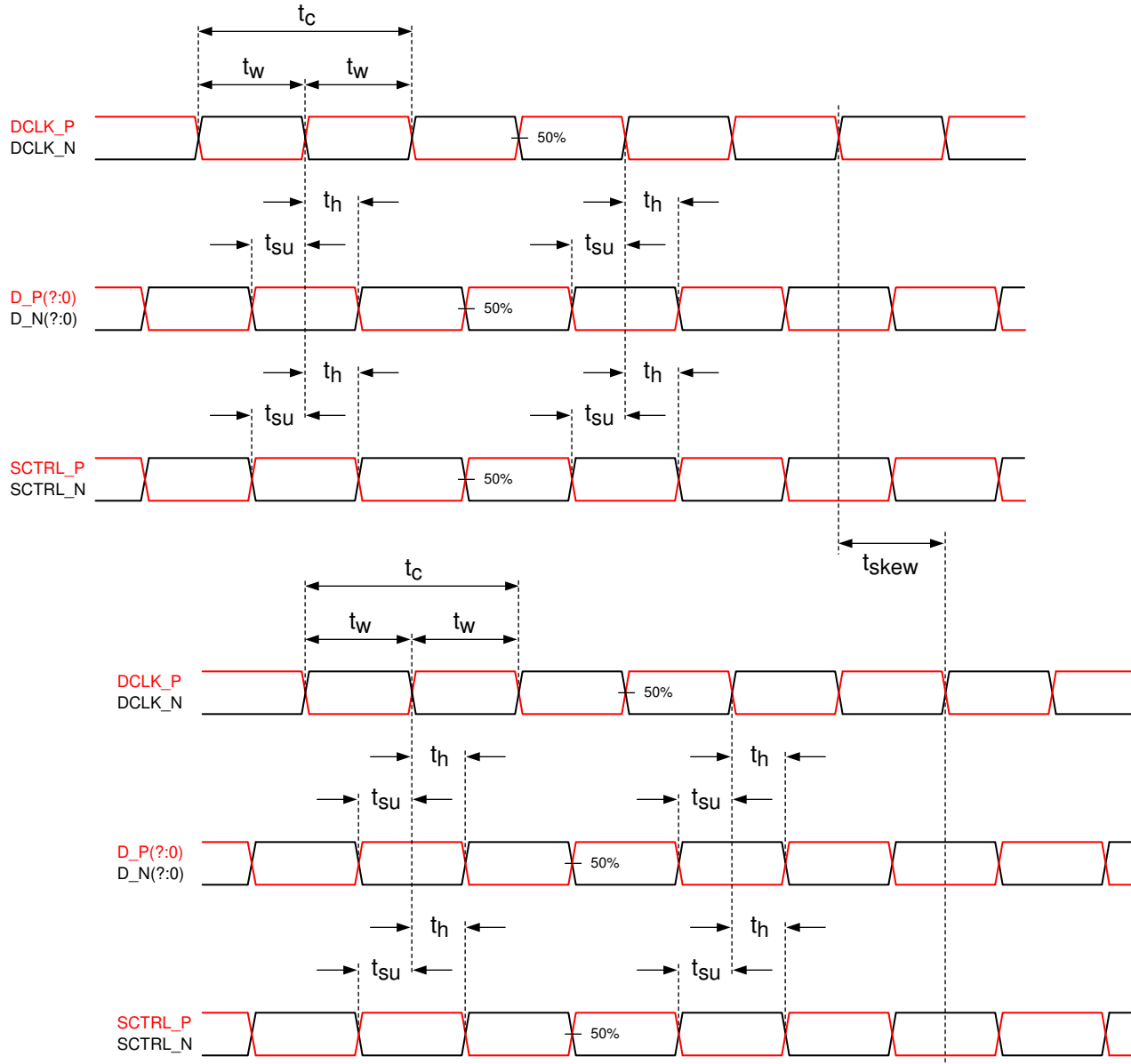
For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. System designers use IBIS or other simulation tools to correlate the timing reference load to a system environment.

图 6-4. Test Load Circuit for Output Propagation Measurement



See [Recommended Operating Conditions](#) for  $V_{CM}$ ,  $V_{ID}$ , and  $V_{LVDS}$  specifications and conditions.

**图 6-5. LVDS Waveform Requirements**



See [Timing Diagrams](#) for timing requirements and LVDS pairs per channel (bus) defining D\_P(?:0) and D\_N(?:0).

图 6-6. Timing Requirements

## 6.9 System Mounting Interface Loads

表 6-1. System Mounting Interface Loads

PARAMETER	MIN	NOM	MAX	UNIT
Thermal interface area <sup>(1)</sup>			12	kg
Electrical interface area <sup>(1)</sup>			25	kg

(1) Uniformly distributed within area shown in [图 6-7](#).

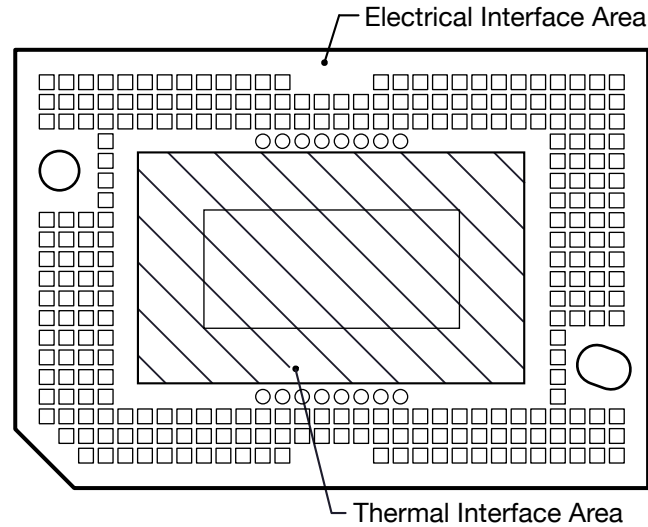


图 6-7. System Mounting Interface Loads

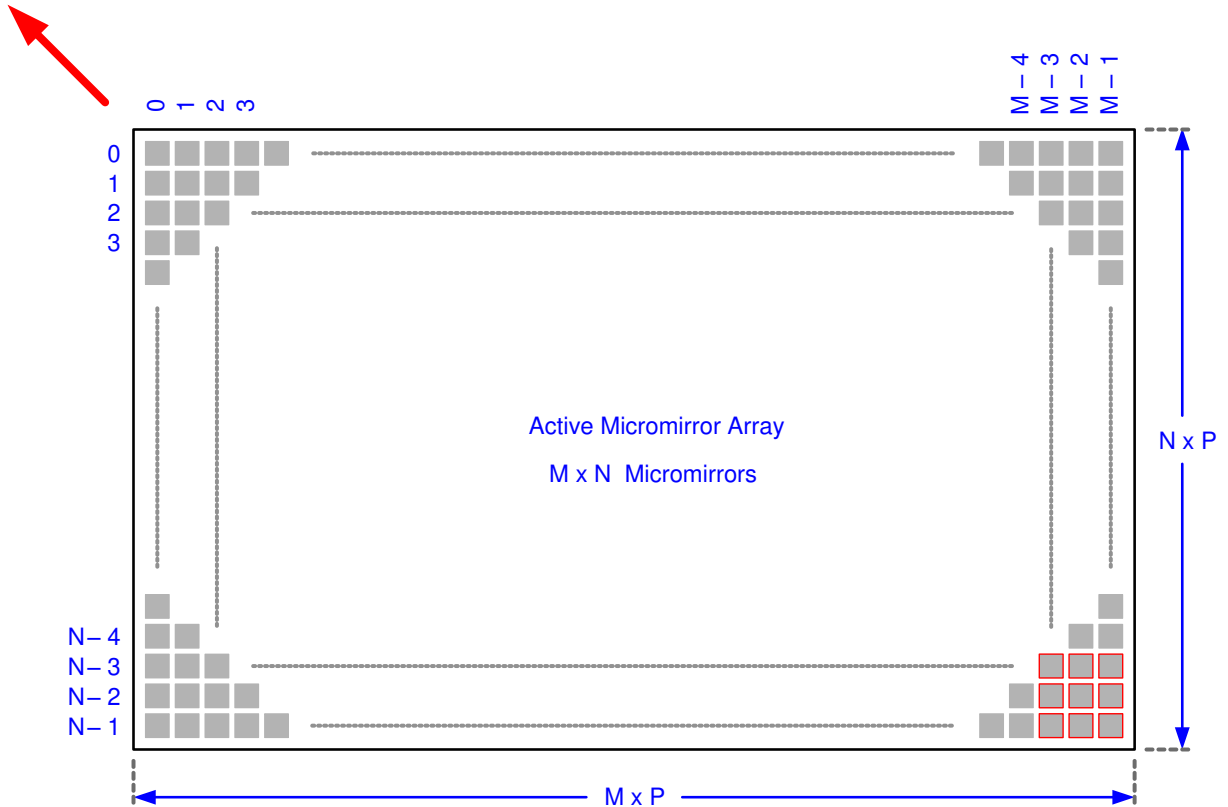
## 6.10 Micromirror Array Physical Characteristics

表 6-2. Micromirror Array Physical Characteristics

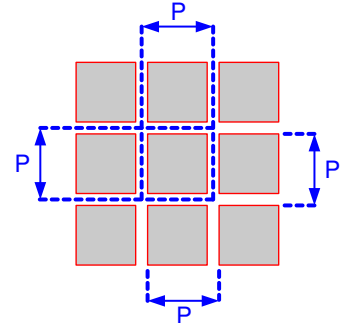
PARAMETER DESCRIPTION		VALUE	UNIT
Number of active columns <sup>(1)</sup>	M	1920	micromirrors
Number of active rows <sup>(1)</sup>	N	1080	micromirrors
Micromirror (pixel) pitch <sup>(1)</sup>	P	5.4	μm
Micromirror active array width <sup>(1)</sup>	Micromirror pitch × number of active columns	10.368	mm
Micromirror active array height <sup>(1)</sup>	Micromirror pitch × number of active rows	5.832	mm
Micromirror active border (top / bottom) <sup>(2)</sup>	Pond of micromirrors (POM)	80	micromirrors/side
Micromirror active border (right / left) <sup>(2)</sup>	Pond of micromirrors (POM)	84	micromirrors/side

- (1) See 图 6-8.
- (2) The structure and qualities of the border around the active array includes a band of partially functional micromirrors referred to as the pond of micromirrors (POM). These micromirrors are prevented from tilting toward the bright or “on” state but still require an electrical bias to tilt toward “off.”

Off-State Light Path



Incident Illumination Light Path



Pond Of Micromirrors (POM) omitted for clarity.

Details omitted for clarity. Not to scale.

图 6-8. Micromirror Array Physical Characteristics

Refer to section [Micromirror Array Physical Characteristics](#) table for M, N, and P specifications.

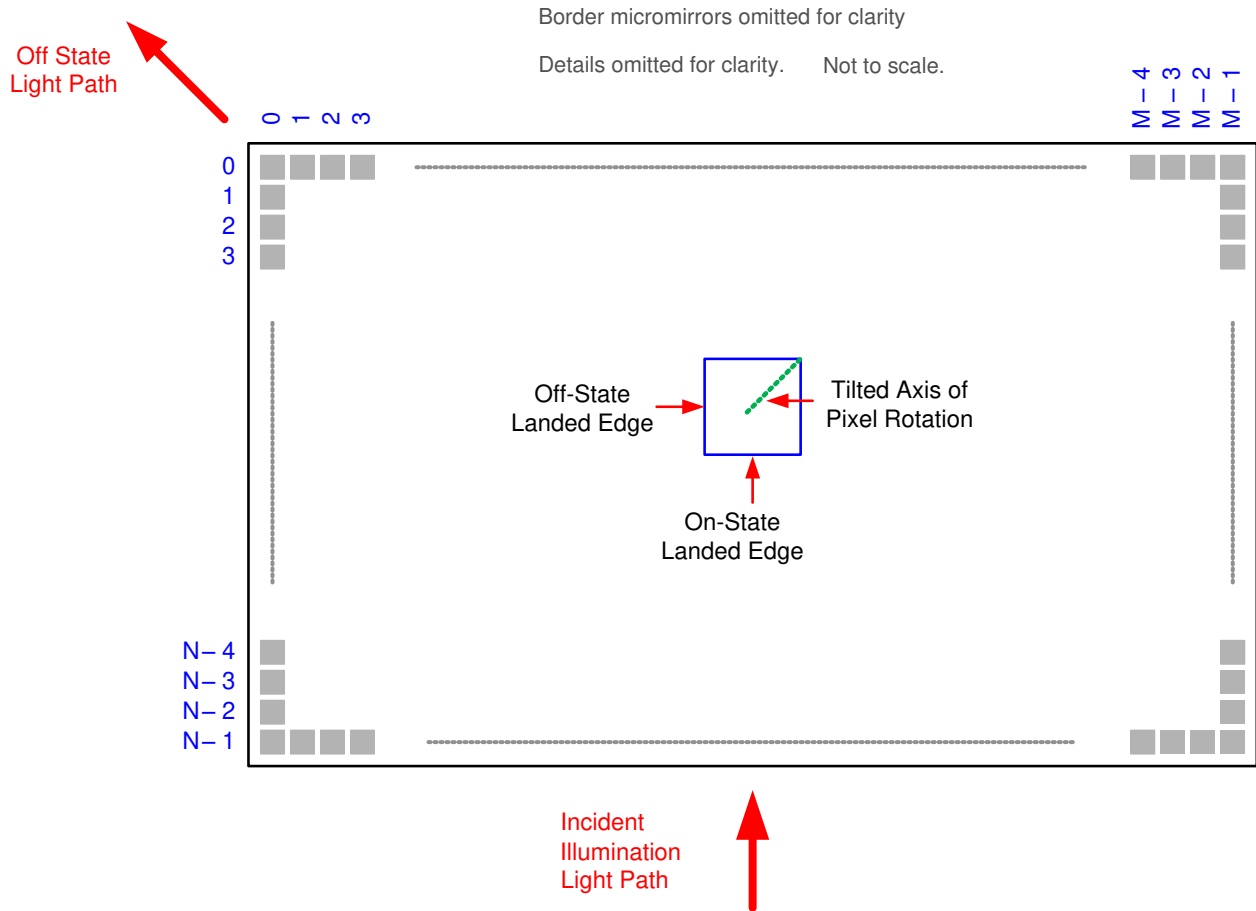
### 6.11 Micromirror Array Optical Characteristics

表 6-3. Micromirror Array Optical Characteristics

PARAMETER		MIN	NOM	MAX	UNIT
Mirror tilt angle, variation device to device <sup>(1) (2) (3) (4)</sup>		15.6	17.0	18.4	degrees
Number of out-of-specification micromirrors <sup>(5)</sup>	Adjacent micromirrors			0	micromirrors
	Non-Adjacent micromirrors			10	
DMD Efficiency (420 nm - 680 nm)			68		%

- (1) Measured relative to the plane formed by the overall micromirror array
- (2) Variation can occur between any two individual micromirrors located on the same device or located on different devices.
- (3) Additional variation exists between the micromirror array and the package datums. See package drawing.
- (4) See 图 6-9.

(5) An out-of-specification micromirror is defined as a micromirror that is unable to transition between the two landed states.



- A. Pond of micromirrors (POM) omitted for clarity.
- B. Refer to section [Micromirror Array Physical Characteristics](#) table for M, N, and P specifications.

图 6-9. Micromirror Landed Orientation and Tilt

## 6.12 Window Characteristics

表 6-4. DMD Window Characteristics

DESCRIPTION	MIN	NOM
Window material		Corning Eagle XG
Window refractive index at 546.1 nm		1.5119
Window transmittance, minimum within the wavelength range 420-680 nm. Applies to all angles 0°-30° AOI. (1) (2)	97%	
Window transmittance, average over the wavelength range 420-680 nm. Applies to all angles 30°-45° AOI. (1) (2)	97%	

- (1) Single-pass through both surfaces and glass.
- (2) Angle of incidence (AOI) is the angle between an incident ray and the normal to a reflecting or refracting surface.

## 6.13 Chipset Component Usage Specification

Reliable function and operation of the DLP470TE DMD requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology consists of the TI technology and devices used for operating or controlling a DLP DMD.

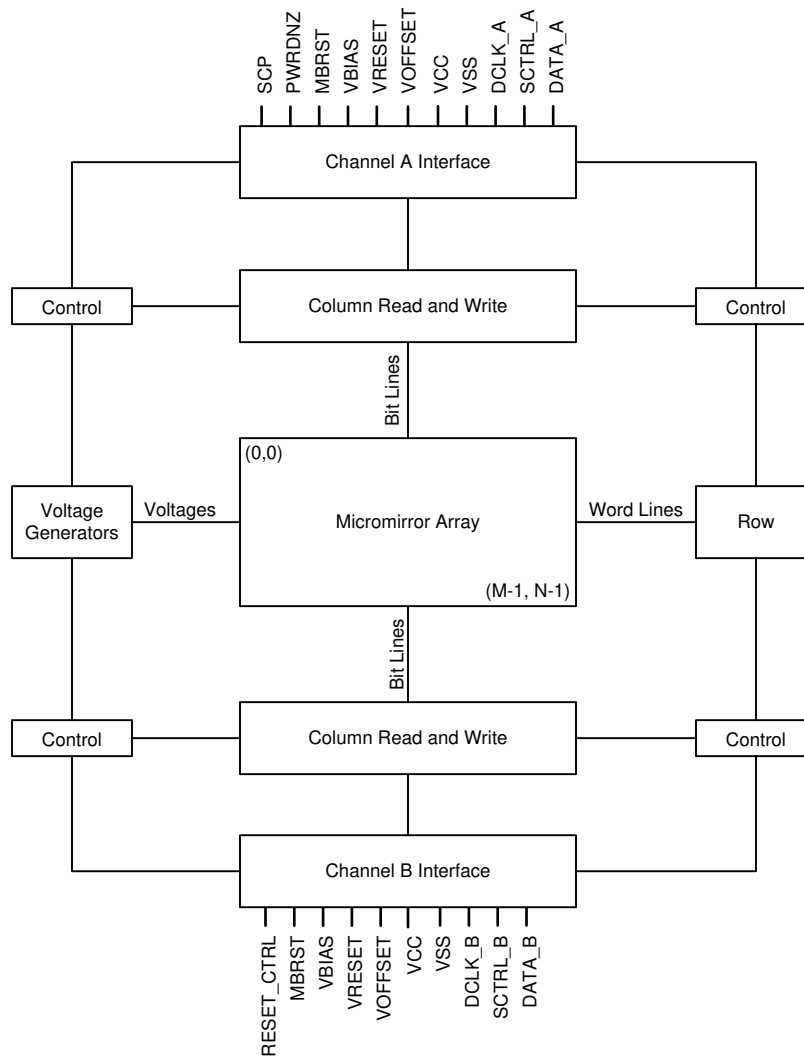
## 7 Detailed Description

### 7.1 Overview

The DMD is a 0.47-inch diagonal spatial light modulator which consists of an array of highly reflective aluminum micromirrors. The DMD is an electrical input, optical output micro-electrical-mechanical system (MEMS). The electrical interface is low voltage differential signaling (LVDS). The DMD consists of a two-dimensional array of 1-bit CMOS memory cells. The array is organized in a grid of M memory cell columns by N memory cell rows. Refer to the [Functional Block Diagram](#). The positive or negative deflection angle of the micromirrors can be individually controlled by changing the address voltage of underlying CMOS addressing circuitry and micromirror reset signals (MBRST).

The DLP470TE DMD is part of the chipset that comprises the DLP470TE DMD, the DLPC4420 display controller, and the DLPA100 power and motor driver. To ensure reliable operation, the DLP470TE DMD must always be used with the DLPC4420 display controller and the DLPA100 power and motor driver.

### 7.2 Functional Block Diagram





### 备注

Channels C and D not shown. For pin details on channels A, B, C, and D, refer to the *Pin Configurations and Functions* table and the LVDS interface section of [Timing Diagrams](#). RESET\_CTRL is utilized in applications when an external reset signal is required.

## 7.3 Feature Description

### 7.3.1 Power Interface

The DMD requires five DC voltages: DMD\_P3P3V, DMD\_P1P8V,  $V_{\text{OFFSET}}$ ,  $V_{\text{RESET}}$ , and  $V_{\text{BIAS}}$ . DMD\_P3P3V is created by the DLPA100 power and motor driver and is used on the DMD board to create the other 4 DMD voltages, as well as powering various peripherals (TMP411, I<sup>2</sup>C, and TI level translators). DMD\_P1P8V is created by the TI PMIC LP38513S and provides the  $V_{\text{CC}}$  voltage required by the DMD.  $V_{\text{OFFSET}}$  (10 V),  $V_{\text{RESET}}$  (-14 V), and  $V_{\text{BIAS}}$  (18 V) are made by the TI PMIC TPS65145 and are supplied to the DMD to control the micromirrors.

### 7.3.2 Timing

The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. The specifications show an equivalent test load circuit for the output under test. Timing reference loads are not intended as a precise representation of any particular system environment or depiction of the actual load presented by a production test. System designers use IBIS or other simulation tools to correlate the timing reference load to a system environment. The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

## 7.4 Device Functional Modes

DMD functional modes are controlled by the DLPC4420 display controller. For more information, see the [DLPC4420 Display Controller Data Sheet](#) or contact a TI applications engineer.

## 7.5 Optical Interface and System Image Quality Considerations

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. System optical performance and image quality strongly relate to optical system design parameter trade offs. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

### 7.5.1 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area needs to be the same. This angle cannot exceed the nominal device micromirror tilt angle unless appropriate apertures are added in the illumination and projection pupils to block out flat-state and stray light from the projection lens. The micromirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the micromirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle, contrast degradation, and objectionable artifacts in the display border or active area could occur.

### 7.5.2 Pupil Match

TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display border or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

### 7.5.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view, and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. Design the illumination optical system to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system optical architecture, overfill light may have to be further reduced below the suggested 10% level in order to be acceptable.

### 7.6 Micromirror Array Temperature Calculation

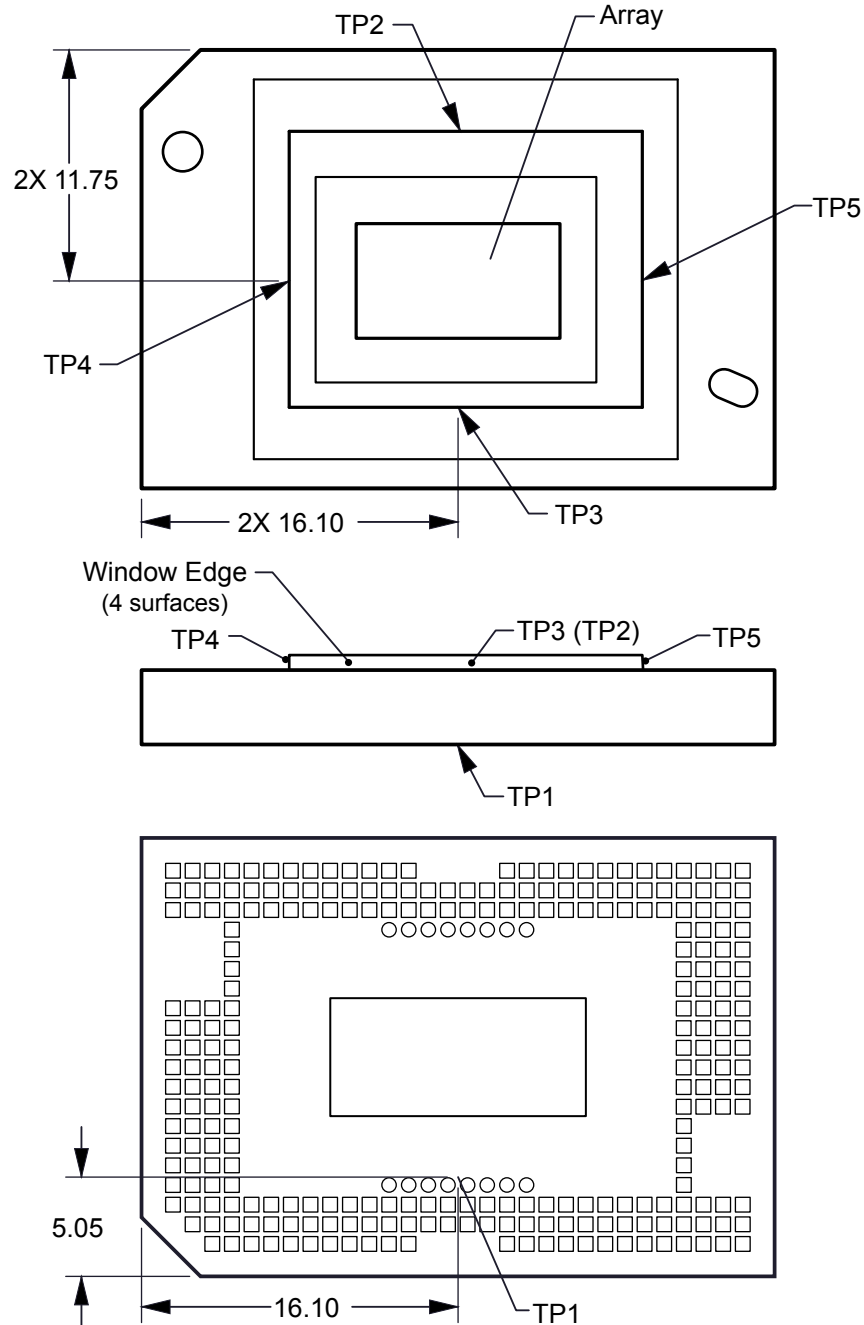


图 7-1. DMD Thermal Test Points

Micromirror array temperature can be computed analytically from measurement points on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load. The relationship between micromirror array temperature and the reference ceramic temperature is provided by the following equations:

$$T_{\text{ARRAY}} = T_{\text{CERAMIC}} + (Q_{\text{ARRAY}} \times R_{\text{ARRAY-TO-CERAMIC}}) \quad (1)$$

$$Q_{\text{ARRAY}} = Q_{\text{ELECTRICAL}} + Q_{\text{ILLUMINATION}} \quad (2)$$

where

- $T_{\text{ARRAY}}$  = computed array temperature (°C)
- $T_{\text{CERAMIC}}$  = measured ceramic temperature (°C) (TP1 location)
- $R_{\text{ARRAY-TO-CERAMIC}}$  = thermal resistance of package from array to ceramic TP1 (°C/Watt)
- $Q_{\text{ARRAY}}$  = Total DMD power on the array (Watts) (electrical + absorbed)
- $Q_{\text{ELECTRICAL}}$  = nominal electrical power
- $Q_{\text{ILLUMINATION}} = (C_{\text{L2W}} \times \text{SL})$
- $C_{\text{L2W}}$  = Conversion constant for screen lumens to power on DMD (Watts/Lumen)
- $\text{SL}$  = measured screen lumens

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates and operating frequencies. A nominal electrical power dissipation to use when calculating array temperature is 0.9 Watts. The absorbed power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. The equations shown above are valid for a 1-Chip DMD system with projection efficiency from the DMD to the screen of 87%.

The conversion constant  $C_{\text{L2W}}$  is based on array characteristics. It assumes a spectral efficiency of 300 lumens/Watt for the projected light and illumination distribution of 83.7% on the active array, and 16.3% on the array border.

Sample calculations for typical projection application:

$$Q_{\text{ELECTRICAL}} = 0.9 \text{ W} \quad (3)$$

$$C_{\text{L2W}} = 0.00266 \quad (4)$$

$$\text{SL} = 4000 \text{ lm} \quad (5)$$

$$T_{\text{CERAMIC}} = 55.0^\circ\text{C} \quad (6)$$

$$Q_{\text{ARRAY}} = 0.9 \text{ W} + (0.00266 \times 4000 \text{ lm}) = 11.54 \text{ W} \quad (7)$$

$$T_{\text{ARRAY}} = 55.0^\circ\text{C} + (11.54 \text{ W} \times 0.90^\circ\text{C/W}) = 65.39^\circ\text{C} \quad (8)$$

## 7.7 Micromirror Landed-On/Landed-Off Duty Cycle

### 7.7.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the ON state versus the amount of time the same micromirror is landed in the OFF state.

As an example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the ON state 100% of the time (and in the OFF state 0% of the time), whereas 0/100 indicate that the pixel is in the OFF state 100% of the time. Likewise, 50/50 indicates that the pixel is ON for 50% of the time (and OFF for 50% of the time).

Note that when assessing the landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) always add to 100.

### 7.7.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD usable life.

Note that it is the symmetry or asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

### 7.7.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD temperature and landed duty cycle interact to affect DMD usable life, and this interaction can be exploited to reduce the impact that an asymmetrical landed duty cycle has on the DMD usable life. This is quantified in the de-rating curve shown in [Figure 6-1](#). The importance of this curve is that:

- All points along this curve represent the same usable life.
- All points above this curve represent lower usable life (and the further away from the curve, the lower the usable life).
- All points below this curve represent higher usable life (and the further away from the curve, the higher the usable life).

In practice, this curve specifies the maximum operating DMD temperature at a given long-term average landed duty cycle.

### 7.7.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the landed duty cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel operates under a 100/0 landed duty cycle during that time period. Likewise, when displaying pure-black, the pixel operates under a 0/100 landed duty cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the landed duty cycle tracks one-to-one with the gray scale value, as shown in [Table 7-1](#).

**表 7-1. Grayscale Value and Landed Duty Cycle**

GRAYSCALE VALUE	LANDED DUTY CYCLE
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, or blue) for the given pixel as well as the color cycle

time for each primary color, where “color cycle time” is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

Use the following equation to calculate the landed duty cycle of a given pixel during a specified time period

$$\text{Landed Duty Cycle} = (\text{Red\_Cycle\_}\% \times \text{Red\_Scale\_Value}) + (\text{Green\_Cycle\_}\% \times \text{Green\_Scale\_Value}) + (\text{Blue\_Cycle\_}\% \times \text{Blue\_Scale\_Value})$$

where

- Red\_Cycle\_% represents the percentage of the frame time that red is displayed to achieve the desired white point
- Green\_Cycle\_% represents the percentage of the frame time that green is displayed to achieve the desired white point
- Blue\_Cycle\_% represents the percentage of the frame time that blue is displayed to achieve the desired white point

For example, assume that the red, green, and blue color cycle times are 50%, 20%, and 30% respectively (in order to achieve the desired white point), then the landed duty cycle for various combinations of red, green, and blue color intensities are as shown in [表 7-2](#) and [表 7-3](#).

**表 7-2. Example Landed Duty Cycle for Full-Color,  
Color Percentage**

CYCLE PERCENTAGE		
RED	GREEN	BLUE
50%	20%	30%

**表 7-3. Example Landed Duty Cycle for Full-Color**

SCALE VALUE			LANDED DUTY CYCLE
RED	GREEN	BLUE	
0%	0%	0%	0/100
100%	0%	0%	50/50
0%	100%	0%	20/80
0%	0%	100%	30/70
12%	0%	0%	6/94
0%	35%	0%	7/93
0%	0%	60%	18/82
100%	100%	0%	70/30
0%	100%	100%	50/50
100%	0%	100%	80/20
12%	35%	0%	13/87
0%	35%	60%	25/75
12%	0%	60%	24/76
100%	100%	100%	100/0

## 8 Application and Implementation

### 备注

Information in the following application section is not part of the TI component specifications, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

Texas Instruments DLP® technology is a micro-electro-mechanical systems (MEMS) technology that modulates light using a digital micromirror device (DMD). The DMD is a spatial light modulator, which reflects incoming light from an illumination source to one of two directions, towards the projection optics or collection optics. The new TRP pixel with a higher tilt angle increases brightness performance and enables smaller system electronics for size constrained applications. Typical applications using the DLP470NE include home theater, digital signage, interactive displays, low-latency gaming displays, and portable smart displays.

The most recent class of chipsets from Texas Instruments is based on a breakthrough micromirror technology called TRP. With a smaller pixel pitch of 5.4  $\mu\text{m}$  and increased tilt angle of 17 degrees, TRP chipsets enable higher resolution in a smaller form factor and enhanced image processing features while maintaining high optical efficiency. DLP® chipsets are a great fit for any system that requires high resolution and high brightness displays. The following orderables have been replaced by the DLP470TE.

#### Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)	Mechanical ICD
1910-5532B	FXJ (257)	32.2 mm × 22.3 mm	2516207
1910-5537B	FXJ (257)	32.2 mm × 22.3 mm	2516207
1910-553AB	FXJ (257)	32.2 mm × 22.3 mm	2516207

### 8.2 Typical Application

The DLP470TE DMD combined with two DLPC4420 display controllers, an FPGA, a power management device DLPA100, and other electrical, optical, and mechanical components, enables bright, affordable, full 4K UHD display solutions. [图 8-1](#) shows a typical 4K UHD system application using the DLP470TE DMD.

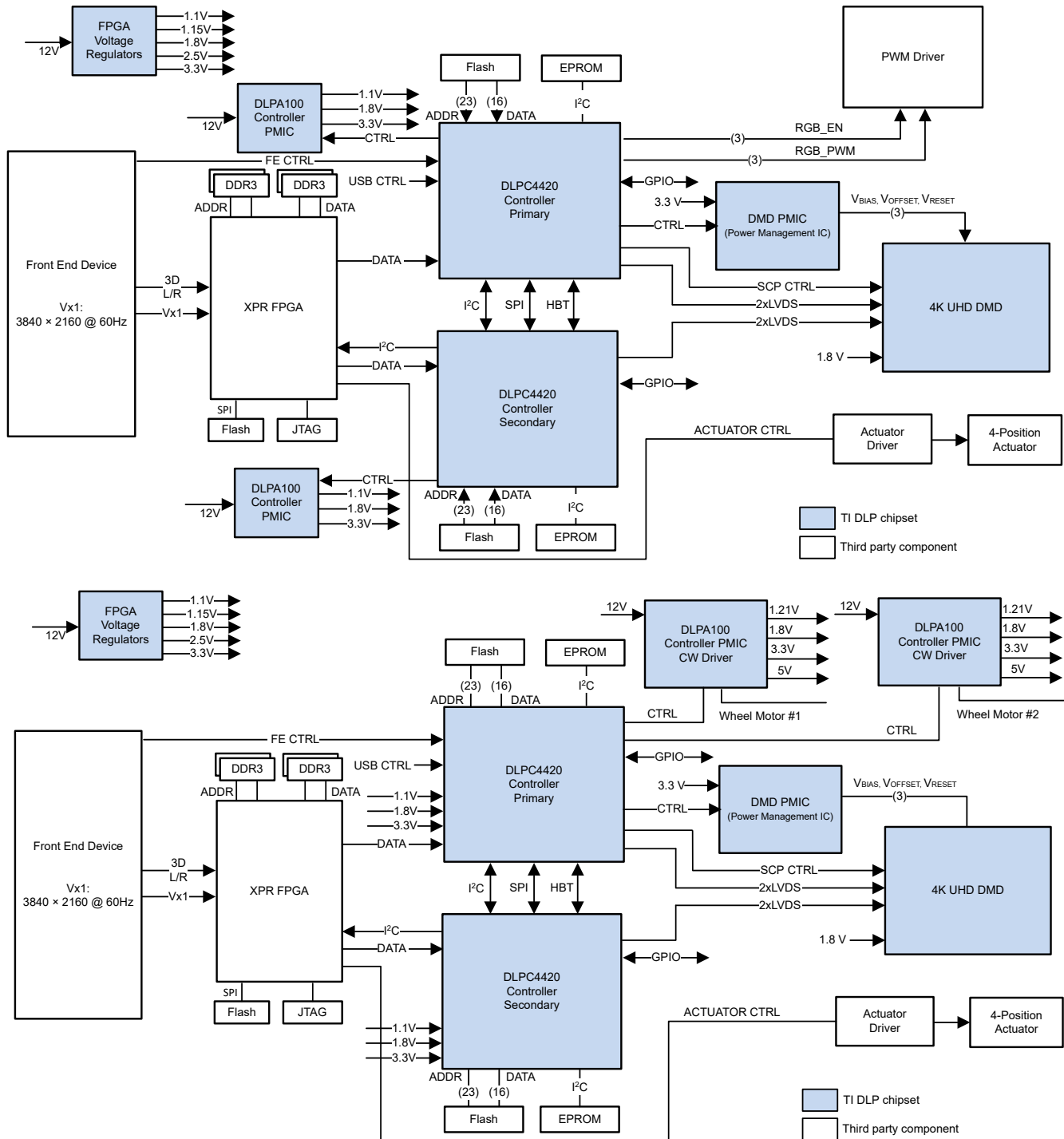


图 8-1. Typical DLPC4420 4K UHD Application (LED, Top; LPCW, Bottom)

### 8.2.1 Design Requirements

A DLP470TE projection system is created by using the DMD chipset, including the DLP470TE digital micromirror device (DMD), the DLPC4420 controller, and the DLPA100 power management and motor driver. The DLP470TE is used as the core imaging device in the display system and contains a 0.47-inch array of micromirrors. The DLPC4420 controller is the digital interface between the DMD and the rest of the system,

taking digital input from a front-end receiver and driving the DMD over a high-speed interface. The DLPA100 power management device provides voltage regulators for the DMD, controller, and illumination functionality.

Other core components of the display system include an FPGA, illumination source, an optical engine for the illumination and projection optics, other electrical and mechanical components, and software. The illumination source options include lamp, LED, laser, or laser phosphor. The type of illumination used and desired brightness will have a major effect on the overall system design and size.

### 8.2.2 Detailed Design Procedure

For a complete DLP® system, an optical module or light engine is required that contains the DLP470TE DMD, associated illumination sources, optical elements, and necessary mechanical components.

To ensure reliable operation, the DLP470TE DMD must always be used with the DLPC4420 display controller and the DLPA100 PMIC driver. Refer to the PCB design requirements to see DLP standard TRP digital micromirror devices for the DMD board design and manufacturer handling of the DMD sub-assemblies.

### 8.2.3 Application Curves

When LED illumination is utilized, the typical LED-current-to-luminance relationship is shown in [图 8-2](#).

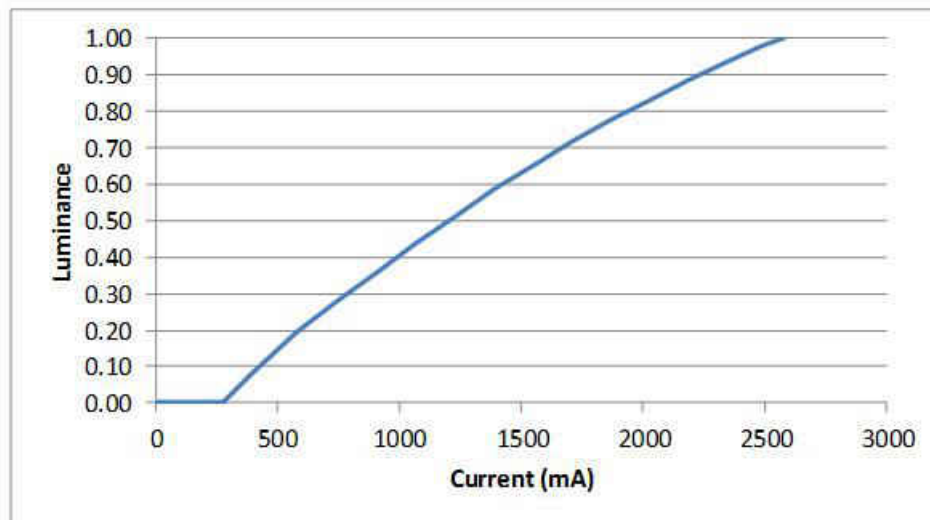


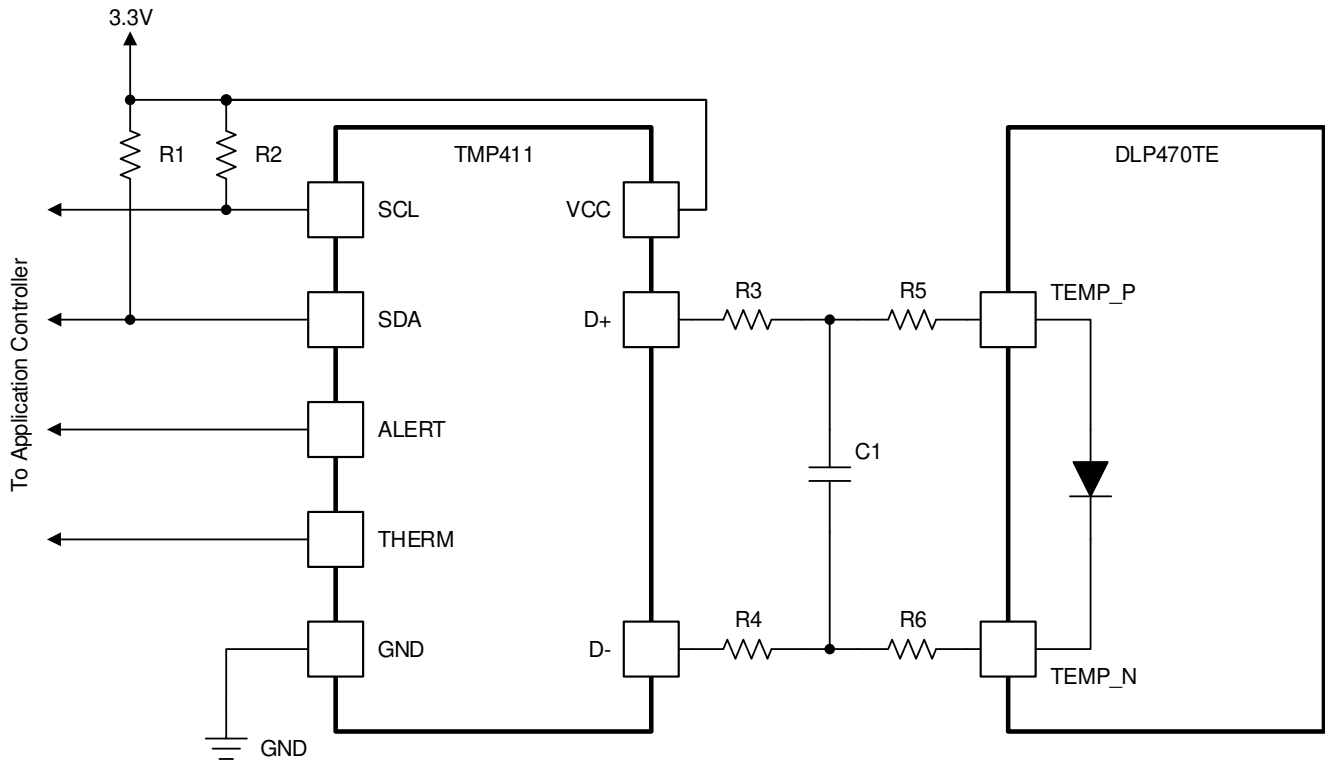
图 8-2. Luminance vs. Current

## 8.3 DMD Die Temperature Sensing

The DMD features a built-in thermal diode that measures the temperature at one corner of the die outside the micromirror array. The thermal diode can be interfaced with the TMP411 temperature sensor as shown in [图 8-3](#). The serial bus from the TMP411 can be connected to the DLPC4420 display controller to enable its temperature sensing features. See the DLPC4420 Programmers' Guide for instructions on installing the DLPC4420 controller support firmware bundle and obtaining the temperature readings.

The software application contains functions to configure the TMP411 to read the DMD temperature sensor diode. This data can be leveraged to incorporate additional functionality in the overall system design such as adjusting illumination, fan speeds, and so forth. All communication between the TMP411 and the DLPC4420 controller will be completed using the I<sup>2</sup>C interface. The TMP411 connects to the DMD via pins B17 and B18 as outlined in [Pin Configuration and Functions](#).





- A. Details omitted for clarity, see the [TI Reference Design](#) for connections to the DLPC4420 controller.
- B. See the [TMP411](#) data sheet for system board layout recommendation.
- C. See the [TMP411](#) data sheet and the TI reference design for suggested component values for R1, R2, R3, R4, and C1.
- D.  $R5 = 0 \Omega$ .  $R6 = 0 \Omega$ . Zero ohm resistors need to be located close to the DMD package pins.

**图 8-3. TMP411 Sample Schematic**

## 9 Power Supply Recommendations

The following power supplies are all required to operate the DMD:

- $V_{SS}$
- $V_{BIAS}$
- $V_{CC}$
- $V_{OFFSET}$
- $V_{RESET}$

DMD power-up and power-down sequencing is strictly controlled by the  $\text{DLP}^{\text{TM}}$  display controller.

### CAUTION

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to any of the prescribed power-up and power-down requirements may affect device reliability. See [Figure 9-1](#).

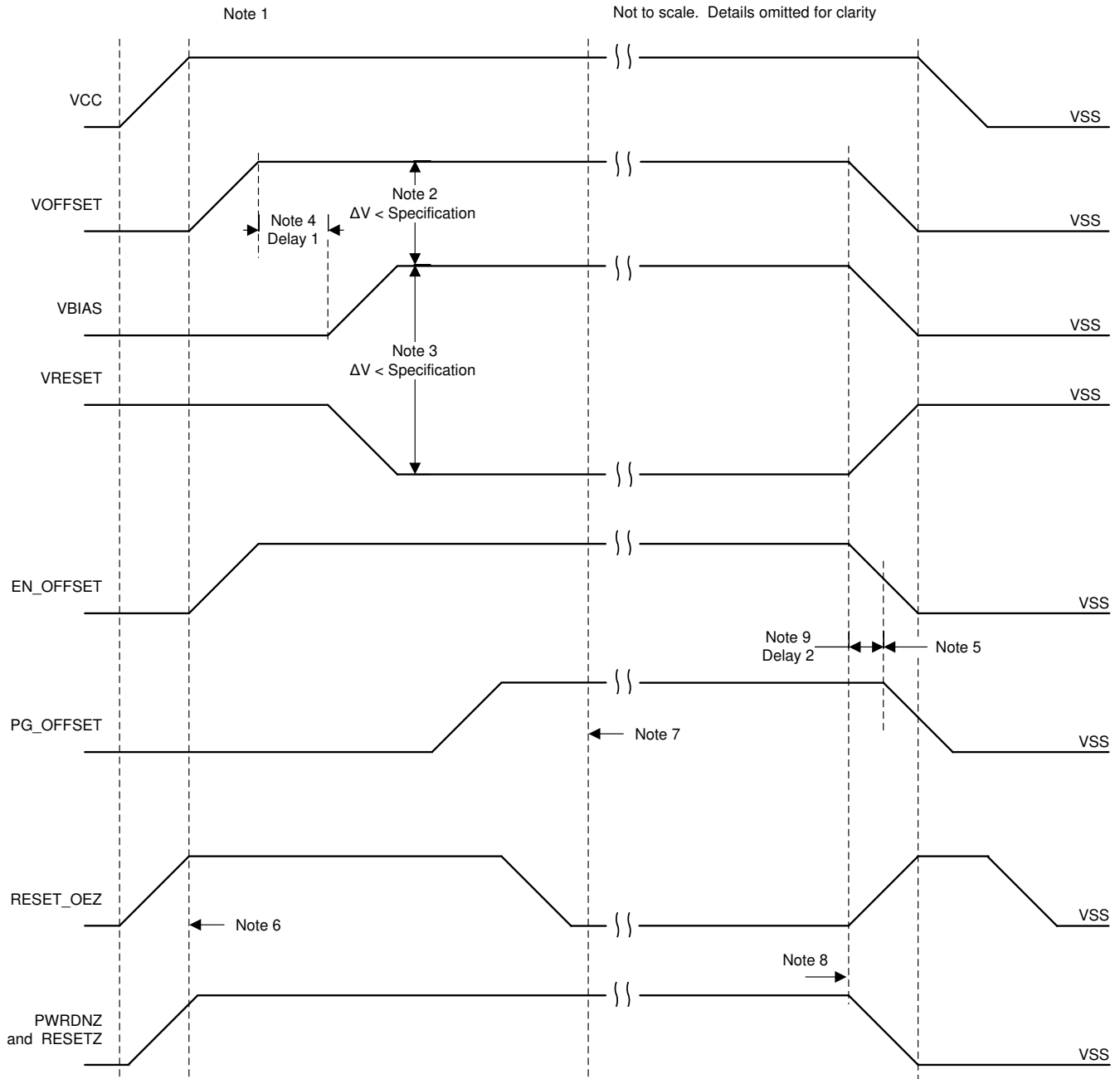
$V_{BIAS}$ ,  $V_{CC}$ ,  $V_{OFFSET}$ , and  $V_{RESET}$  power supplies must be coordinated during power-up and power-down operations. Failure to meet any of the below requirements will result in a significant reduction in the DMD reliability and lifetime. Common ground  $V_{SS}$  must also be connected.

### 9.1 DMD Power Supply Power-Up Procedure

- During power-up,  $V_{CC}$  must always start and settle before  $V_{OFFSET}$  plus Delay1 specified in [Table 9-1](#),  $V_{BIAS}$ , and  $V_{RESET}$  voltages are applied to the DMD.
- During power-up, it is a strict requirement that the voltage difference between  $V_{BIAS}$  and  $V_{OFFSET}$  must be within the specified limit shown in [Recommended Operating Conditions](#).
- During power-up, there is no requirement for the relative timing of  $V_{RESET}$  with respect to  $V_{BIAS}$ .
- Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements specified in the [Absolute Maximum Ratings](#), in the [Recommended Operating Conditions](#), and in [Figure 9-1](#).
- During power-up, LVCMOS input pins must not be driven high until after  $V_{CC}$  have settled at operating voltages listed in the [Recommended Operating Conditions](#).

### 9.2 DMD Power Supply Power-Down Procedure

- During power-down,  $V_{CC}$  must be supplied until after  $V_{BIAS}$ ,  $V_{RESET}$ , and  $V_{OFFSET}$  are discharged to within the specified limit of ground. See [Table 9-1](#).
- During power-down, it is a strict requirement that the voltage difference between  $V_{BIAS}$  and  $V_{OFFSET}$  must be within the specified limit shown in the [Recommended Operating Conditions](#).
- During power-down, there is no requirement for the relative timing of  $V_{RESET}$  with respect to  $V_{BIAS}$ .
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements specified in the [Absolute Maximum Ratings](#), in the [Recommended Operating Conditions](#), and in [Figure 9-1](#).
- During power-down, LVCMOS input pins must be less than specified in the [Recommended Operating Conditions](#).



- A. See [Recommended Operating Conditions](#), and the Pin Functions table.
- B. To prevent excess current, the supply voltage difference  $|V_{\text{OFFSET}} - V_{\text{BIAS}}|$  must be less than the specified limit in the [Recommended Operating Conditions](#)
- C. To prevent excess current, the supply difference  $|V_{\text{BIAS}} - V_{\text{RESET}}|$  must be less than the specified limit in the [Recommended Operating Conditions](#).
- D.  $V_{\text{BIAS}}$  must power up after  $V_{\text{OFFSET}}$  has powered up, per the Delay1 specification in [表 9-1](#)
- E.  $\text{PG\_OFFSET}$  must turn off after  $\text{EN\_OFFSET}$  has turned off, per the Delay2 specification in [表 9-1](#).
- F. ®DLP controller software enables the DMD power supplies  $V_{\text{BIAS}}$ ,  $V_{\text{RESET}}$ ,  $V_{\text{OFFSET}}$  with  $V_{\text{CC}}$  active after  $\text{RESET\_OEZ}$  is at logic high.
- G. ®DLP controller software initiates the global  $V_{\text{BIAS}}$  command.
- H. After the DMD micromirror park sequence is complete, the ®DLP controller software initiates a hardware power-down that activates  $\text{PWRDNZ}$  and disables  $V_{\text{BIAS}}$ ,  $V_{\text{RESET}}$ , and  $V_{\text{OFFSET}}$ .

- I. Under power-loss conditions where emergency DMD micromirror park procedures are being enacted by the <sup>®</sup>DLP controller hardware, EN\_OFFSET may turn off after PG\_OFFSET has turned off. The OEZ signal goes high prior to PG\_OFFSET turning off to indicate the DMD micromirror has completed the emergency park procedures.

### 图 9-1. DMD Power Supply Requirements

表 9-1. DMD Power-Supply Requirements

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNIT
Delay1	Delay from $V_{\text{OFFSET}}$ settled at recommended operating voltage to $V_{\text{BIAS}}$ and $V_{\text{RESET}}$ power up	1	2		ms
Delay2	PG_OFFSET hold time after EN_OFFSET goes low	100			ns

## 10 Layout

### 10.1 Layout Guidelines

The DLP470TE DMD is part of a chipset that is controlled by the DLPC4420 display controller in conjunction with the DLPA100 power and motor driver. These guidelines are targeted to help design a PCB board with the DLP470TE DMD. The DLP470TE DMD board is a high-speed multilayer PCB, with primarily high-speed digital logic using dual-edge clock rates up to 400 MHz for DMD LVDS signals. The remaining traces are comprised of low speed digital LVTTTL signals. TI recommends that mini power planes are used for VOFFSET, VRESET, and VBIAS. Solid planes are required for DMD\_P3P3V(3.3 V), DMD\_P1P8V and Ground. The target impedance for the PCB is  $50 \Omega \pm 10\%$  with the LVDS traces being  $100 \Omega \pm 10\%$  differential. TI recommends using an 8-layer stack-up, as described in [表 10-1](#).

### 10.2 Layout Example

#### 10.2.1 Layers

The layer stack-up and copper weight for each layer is shown in [表 10-1](#). Small sub-planes are allowed on signal routing layers to connect components to major sub-planes on top/bottom layers if necessary.

**表 10-1. Layer Stack-Up**

LAYER NO.	LAYER NAME	COPPER WT. (oz.)	COMMENTS
1	Side A - DMD only	1.5	DMD, escapes, low frequency signals, power sub-planes.
2	Ground	1	Solid ground plane (net GND).
3	Signal	0.5	50 $\Omega$ and 100 $\Omega$ differential signals
4	Ground	1	Solid ground plane (net GND)
5	DMD_P3P3V	1	+3.3-V power plane (net DMD_P3P3V)
6	Signal	0.5	50 $\Omega$ and 100 $\Omega$ differential signals
7	Ground	1	Solid ground plane (net GND).
8	Side B - All other Components	1.5	Discrete components, low frequency signals, power sub-planes

#### 10.2.2 Impedance Requirements

TI recommends that the board has matched impedance of  $50 \Omega \pm 10\%$  for all signals. The exceptions are listed in [表 10-2](#).

**表 10-2. Special Impedance Requirements**

Signal Type	Signal Name	Impedance (ohms)
A channel LVDS differential pairs	D_AP(0:15), D_AN(0:15)	100 $\pm 10\%$ differential across each pair
	DCLKA_P, DCLKA_N	
	SCTRL_AP, SCTRL_AN	
B channel LVDS differential pairs	D_BP(0:15), D_BN(0:15)	100 $\pm 10\%$ differential across each pair
	DCLKB_P, DCLKB_N	
	SCTRL_BP, SCTRL_BN	
C channel LVDS differential pairs	D_CP(0:15), D_CN(0:15)	100 $\pm 10\%$ differential across each pair
	DCLKC_P, DCLKC_N	
	SCTRL_CP, SCTRL_CN	
D channel LVDS differential pairs	D_DP(0:15), D_DN(0:15)	100 $\pm 10\%$ differential across each pair
	DCLKD_P, DCLKD_N	
	SCTRL_DP, SCTRL_DN	

### 10.2.3 Trace Width, Spacing

Unless otherwise specified, TI recommends that all signals follow the 0.005-inch/0.005-inch design rule. Minimum trace clearance from the ground ring around the PWB has a 0.1-inch minimum. An analysis of impedance and stack-up requirements determine the actual trace widths and clearances.

#### 10.2.3.1 Voltage Signals

表 10-3. Special Trace Widths, Spacing Requirements

SIGNAL NAME	MINIMUM TRACE WIDTH TO PINS (MIL)	LAYOUT REQUIREMENT
GND	15	Maximize trace width to connecting pin
DMD_P3P3V	15	Maximize trace width to connecting pin
DMD_P1P8V	15	Maximize trace width to connecting pin
VOFFSET	15	Create mini plane from U2 to U3
VRESET	15	Create mini plane from U2 to U3
VBIAS	15	Create mini plane from U2 to U3
All U3 control connections	10	Use 10 mil etch to connect all signals/voltages to DMD pads

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Device Nomenclature

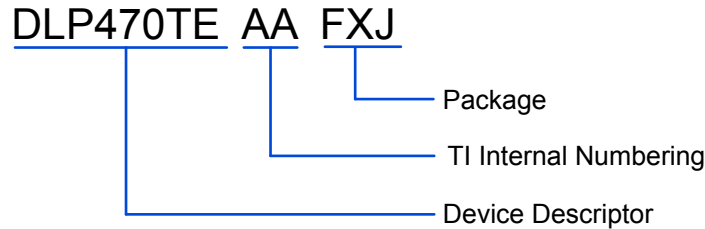


图 11-1. Part Number Description

#### 11.1.2 Device Markings

The device marking includes both human-readable information and a 2-dimensional matrix code. The human-readable information is described in 图 11-2. The 2-dimensional matrix code is an alpha-numeric character string that contains the DMD part number, part 1 of the serial number, and part 2 of the serial number. The first character of the DMD serial number (part 1) is the manufacturing year. The second character of the DMD serial number (part 1) is the manufacturing month. The last character of the DMD Serial Number (part 2) is the bias voltage bin letter.

Example: \*1910-553AB GHXXXXX LLLLLLM

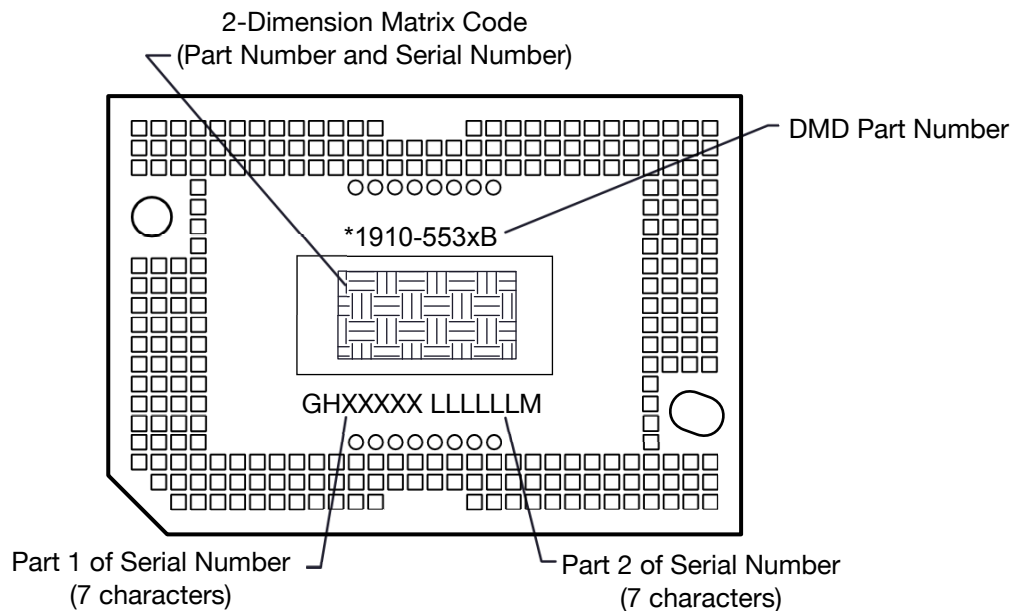


图 11-2. DMD Marking Locations

### 11.2 第三方产品免责声明

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## 11.3 Documentation Support

### 11.3.1 Related Documentation

The following documents contain additional information related to the chipset components used with the DLP470TE.

- [DLPC4420 Display Controller Data Sheet](#)
- [DLPA100 Power Management and Motor Driver Data Sheet](#)

### 11.3.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

### 11.3.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.4 Trademarks

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## 11.5 静电放电警告



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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 11.6 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。



## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLP470TEAAFJ	ACTIVE	CLGA	FXJ	257	33	RoHS & Green	Call TI	N / A for Pkg Type	0 to 70		Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

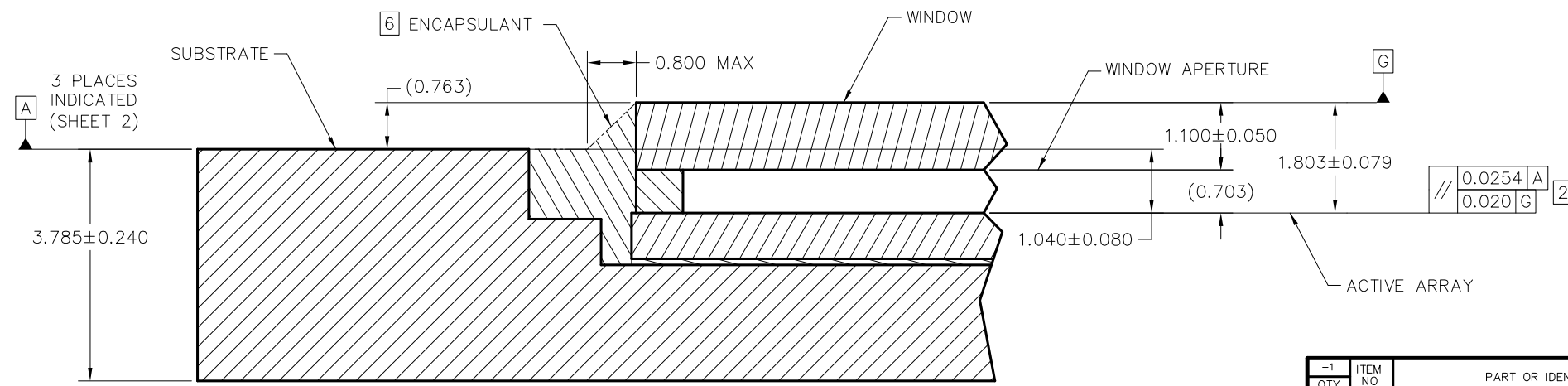
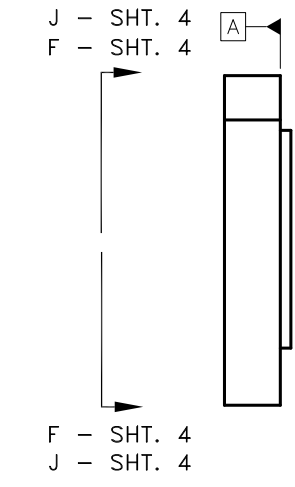
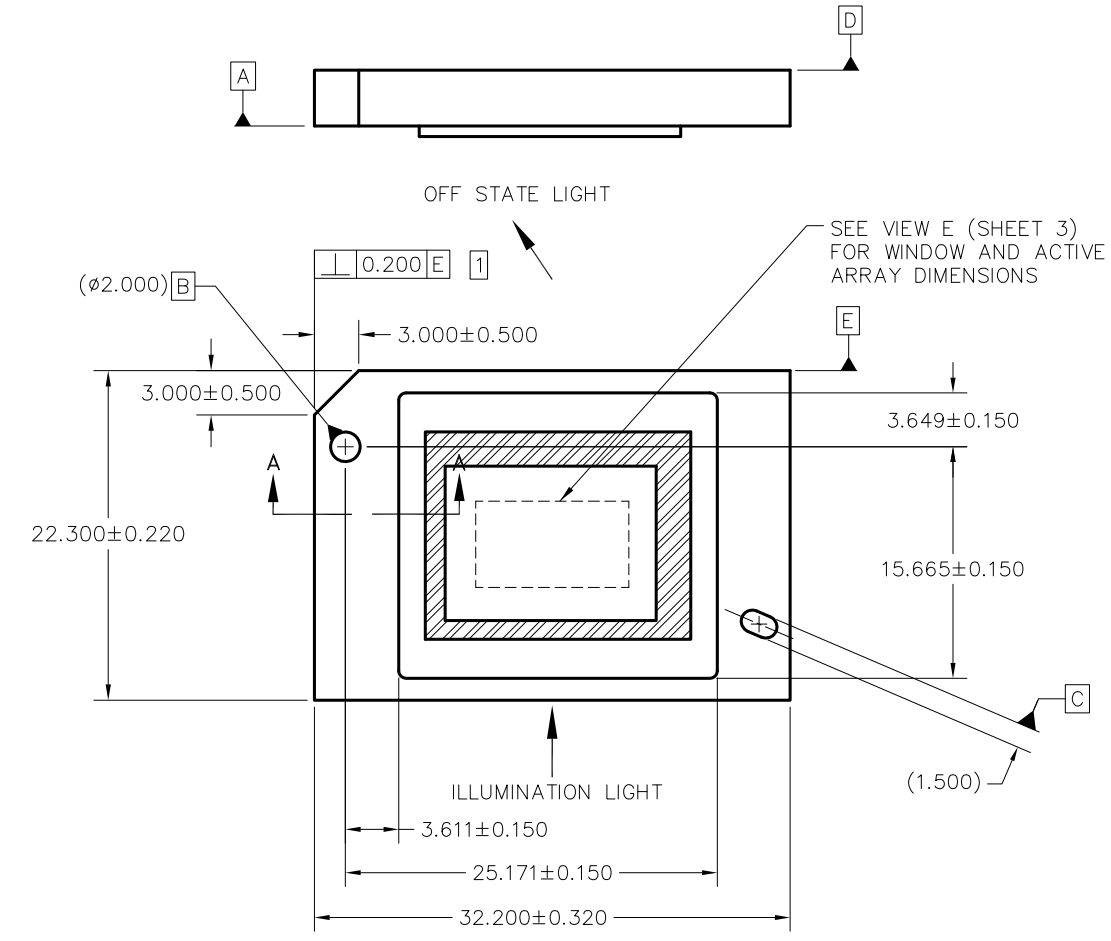
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REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	ECO 2174192, INITIAL RELEASE	05/11/2018	F. ARMSTRONG

NOTES: UNLESS OTHERWISE SPECIFIED:

- 1 SUBSTRATE EDGE PERPENDICULARITY TOLERANCE APPLIES TO ENTIRE SURFACE
- 2 DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY
- 3 ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.8 DEGREES
- 4 SUBSTRATE SYMBOLIZATION PAD, AND PLATING AT BOTTOM OF DATUMS B AND C HOLES TO BE ELECTRICALLY CONNECTED TO VSS PLANE WITHIN THE SUBSTRATE
- 5 BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE AREA
- 6 MAXIMUM ENCAPSULANT PROFILE SHOWN
- 7 ENCAPSULANT ALLOWED ON THE SURFACE OF THE CERAMIC IN THE AREA SHOWN IN VIEW B (SHEET 2). ENCAPSULANT SHALL NOT EXCEED 0.200 THICKNESS MAXIMUM.
- 8 SUBSTRATES PLATED WITH Ni/Au SHALL HAVE THE THREE-DIGIT NUMERICAL MARKING IN THE AREA TO THE LEFT OF THE SYMBOLIZATION PAD. SUBSTRATES PLATED WITH Ni/Pd/Au SHALL HAVE THE MARKING IN THE AREA TO THE RIGHT OF THE SYMBOLIZATION PAD.



SECTION A-A  
SCALE 20/1

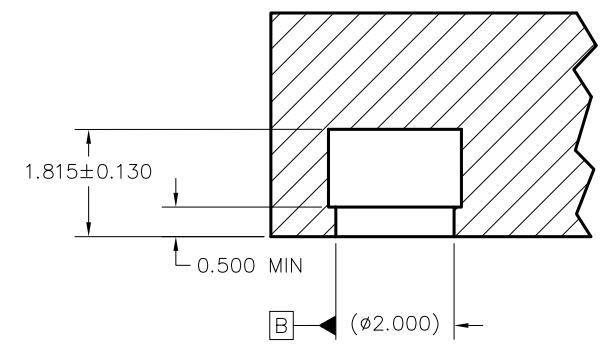
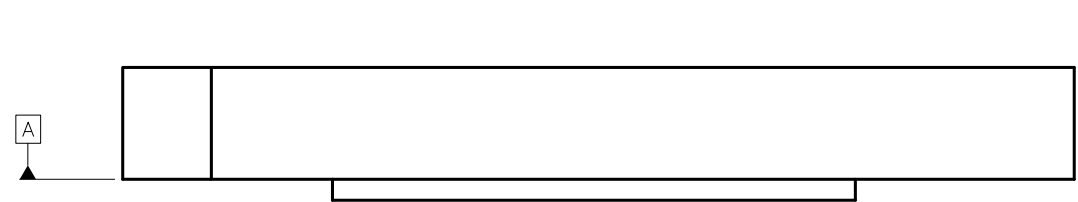
QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES
-1				

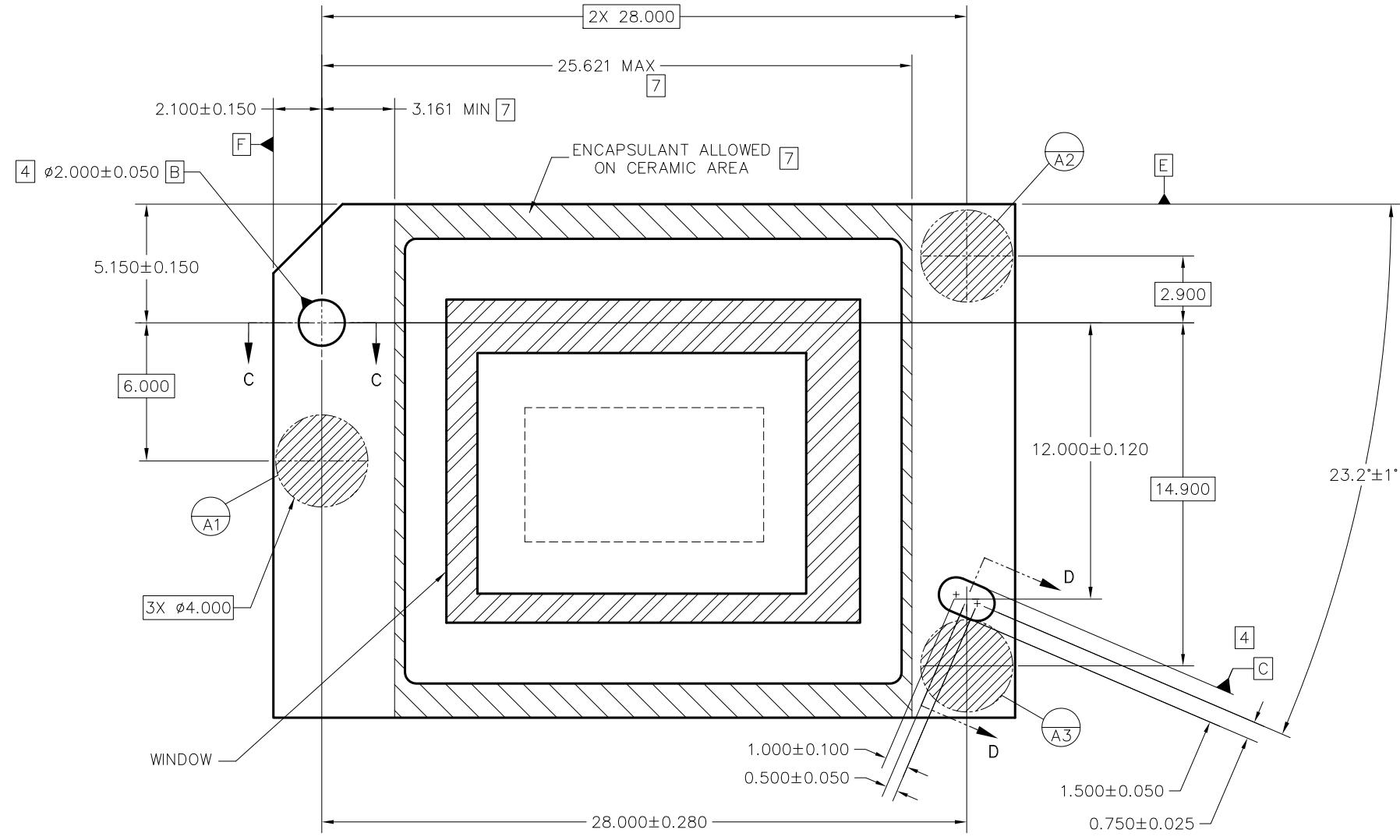
PARTS LIST		DATE		DRAWN	
		05/11/2018		F. ARMSTRONG	
		05/11/2018		F. ARMSTRONG	
		05/11/2018		P. KONRAD	
		05/11/2018		M. DORAK	

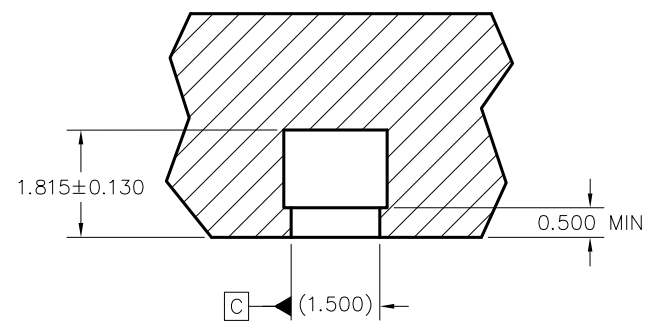
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS TOLERANCES: ANGLES ± 1° 2 PLACE DECIMALS ±0.25 3 PLACE DECIMALS ±0.50		TEXAS INSTRUMENTS Dallas, Texas	
REMOVE ALL BURRS AND SHARP EDGES INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5-1994 DIMENSIONAL LIMITS APPLY BEFORE PROCESSES PARENTHEICAL INFO FOR REF ONLY		ICD, MECHANICAL, DMD .47" UHD MTRP 2xLVDS HB C SERIES 410 (FXJ PACKAGE)	
THIRD ANGLE PROJECTION	NONE	0314DA	SIZE B
NEXT ASSY	USED ON	APPLICATION	DRAWING NO 2516207
			REV A
			SCALE 4/1
			SHEET 1 OF 4



SECTION C-C  
DATUM B  
SCALE 16/1



VIEW B  
DATUMS AND ENCAPSULANT ALLOWABLE AREA  
SCALE 8/1



SECTION D-D  
DATUM C  
SCALE 16/1

8

7

6

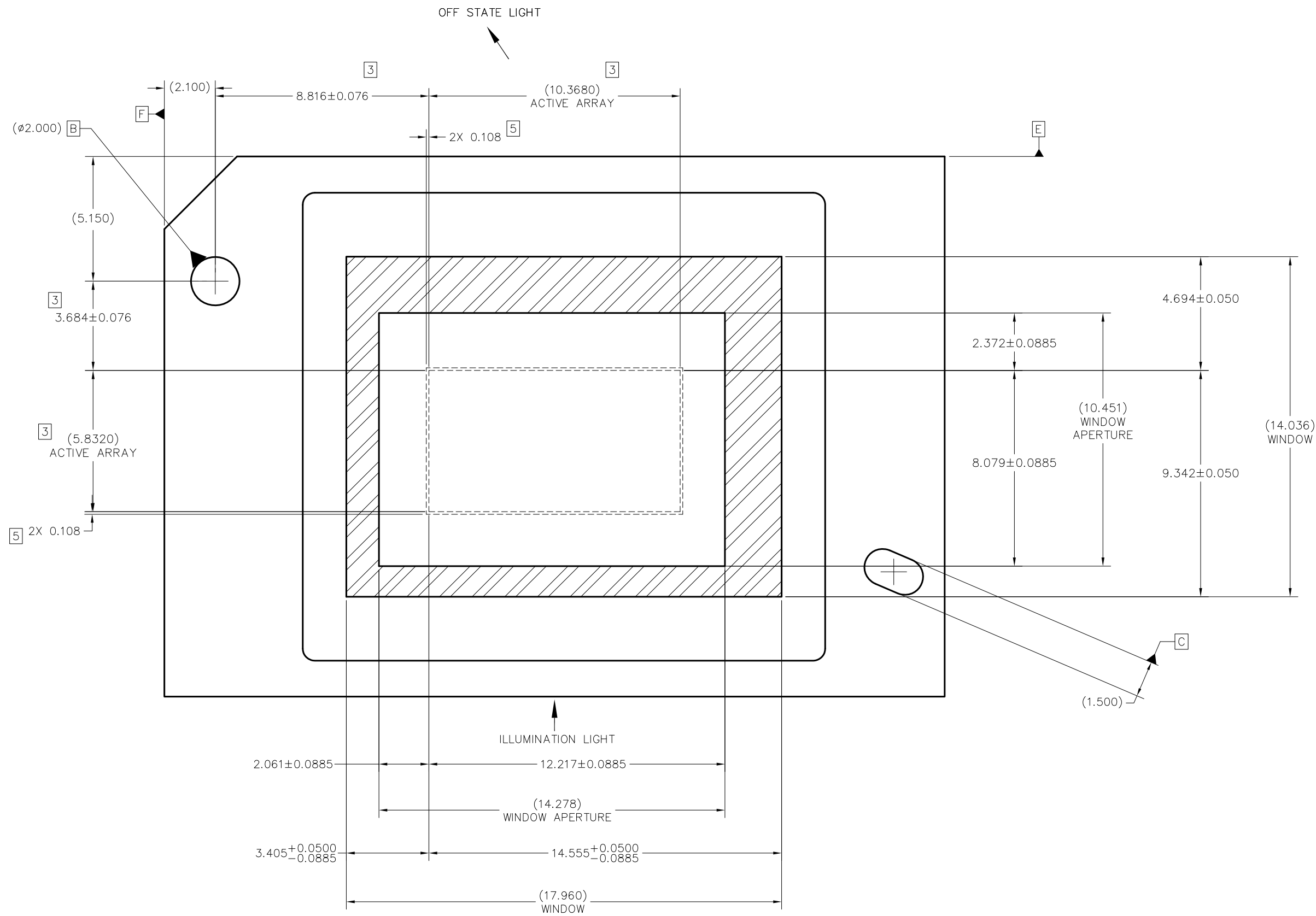
5

4

3

DWG NO 2516207 SH 3

1



VIEW E (SHEET 1)  
 DMD WINDOW AND ACTIVE ARRAY  
 SCALE 12:1

 TEXAS INSTRUMENTS Dallas, Texas	DWN	DATE	SIZE	DRAWING NO	REV
	ISSUE DATE	SCALE	4/1	2516207	A
				SHEET	3

8

7

6

5

4

3

2

1

8

7

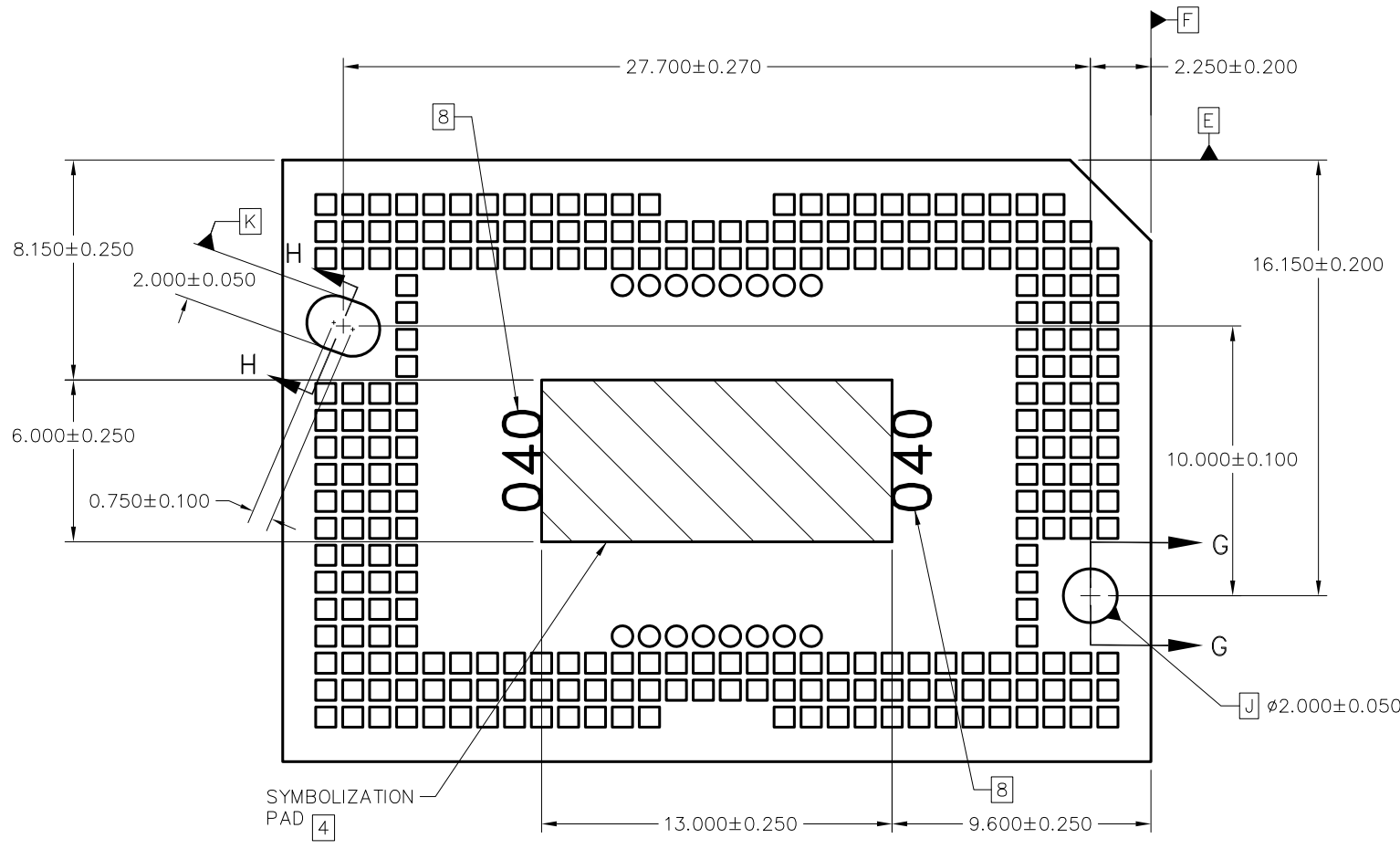
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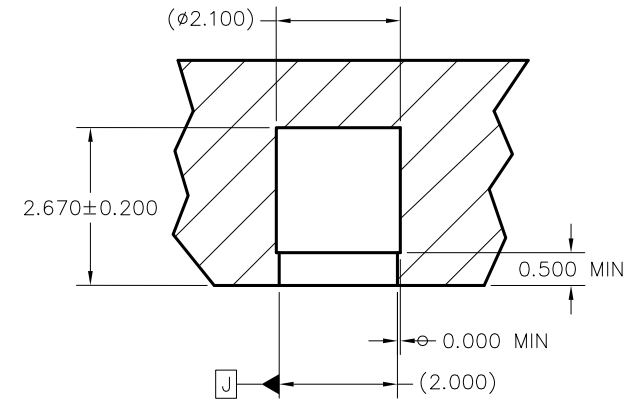
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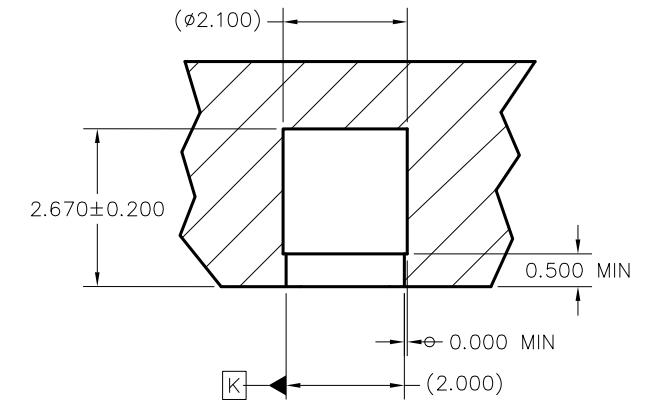
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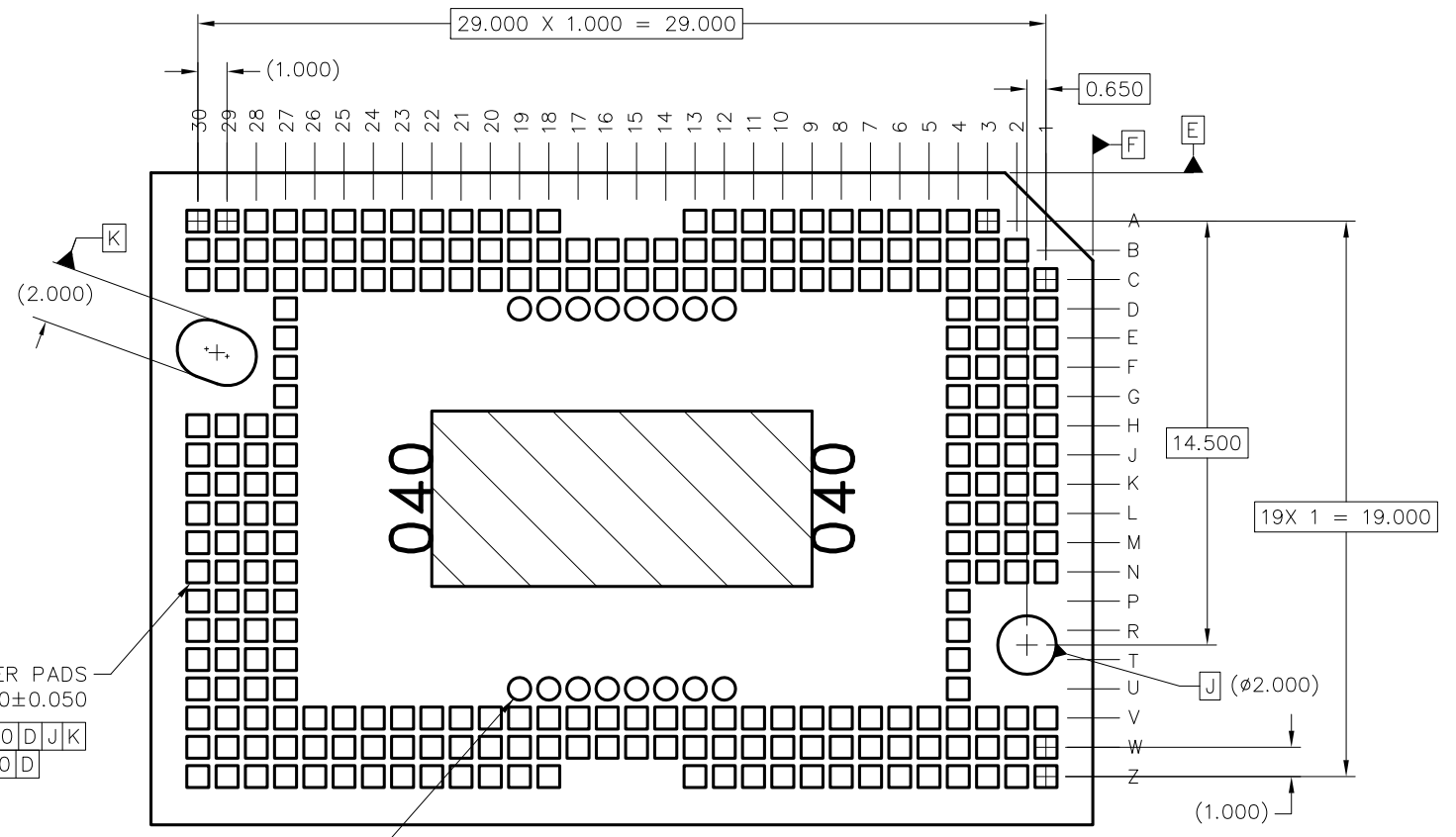
VIEW F-F (SHEET 1)  
DATUMS J AND K, SYMBOLIZATION PAD  
SCALE 8/1



SECTION G-G  
DATUM J  
SCALE 16/1

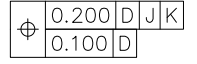


SECTION H-H  
DATUM K  
SCALE 16/1



VIEW J-J (SHEET 1)  
LGA PADS  
SCALE 8/1

257X LGA CUSTOMER PADS  
0.750±0.050 X 0.750±0.050



16X LGA TEST PADS  
DO NOT CONNECT

8

7

6

5

4

3

2

1

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