

## 7 位集成电机和中继驱动器

查询样品: [DRV777](#)

### 特性

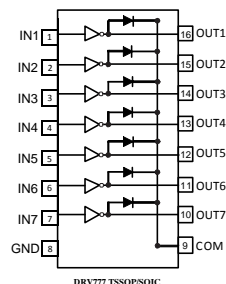
- 支持高达 **20V** 输出上拉电压
- 40°C 至 125°C** 工作温度范围
- 支持宽范围的步进电机, **DC** 电机, 继电器和感应线圈
- 0.4V** (典型值) 的低输出 **VOL**, 此时
  - 在 **5.0V** 的逻辑输入上, 每通道 **140mA** 的电流吸收能力<sup>(1)</sup>
  - 当全部 **7** 个通道并联时, **1A** 电流输出能力<sup>(1)</sup>
- 与 **1.8V**, **3.3V** 和 **5.0V** 微控制器和逻辑接口兼容
- 用于感应反冲保护的内部自振荡二极管
- 输入下拉电阻器可实现三态输入驱动器
- 用来消除嘈杂环境中寄生运行的输入电阻电容 (**RC**) 缓冲器
- 低输入和输出泄漏电流
- 易于使用的并行接口
- 静电放电 (**ESD**) 保护性能超过 **JESD 22** 规范要求
  - 2kV** 人体模型 (**HBM**), **500V** 充电器件模型 (**CDM**)
- 采用 **16** 引脚小外形尺寸集成电路 (**SOIC**) 和薄型小外形尺寸 (**TSSOP**) 封装

<sup>(1)</sup> 总电流吸收有可能受到内部结温、绝对最大电流水平等的限制-详细情况请参考电气规范部分。

### 应用范围

- 单极步进电机驱动器
- 继电器和感应负载驱动器
- 螺线管驱动器
- 照明灯和 **LED** 显示
- 逻辑电平转换器
- 常见低侧开关应用

### 功能图



### 说明

DRV777 电机驱动器特有 7 个低输出阻抗驱动器, 此驱动器能够大大降低片上功率耗散。DRV777 支持 1.8V 至 5V CMOS 逻辑输入接口, 从而使得此器件与大范围的微控制器和其它逻辑接口兼容。DRV777 特有一个经改进的输入接口, 此接口可以大大降低汲取自外部驱动器的输入 DC 电流。此器件特有一个输入 RC 缓冲器, 此缓冲器能够极大地改进此器件在嘈杂运行条件下的性能。所有通道输入特有一个内部输入下拉电阻器, 从而可实现三态输入逻辑。DRV777 还支持其它逻辑输入电平, 例如 TTL 和 1.8V; 详细信息请见典型特性部分。

如功能图中所示, 在共阴极配置中, DRV777 的每一个输出都特有一个连接在 COM 引脚上的内部自振荡二极管。

此器件通过将几条相邻的并联通道组合在一起提供增加电流吸收能力的灵活性。在通常情况下, 当所有 7 个通道并联时, DRV777 能够支持高达 1.0A 的负载电流。DRV777 采用 16 引脚 SOIC 和 16 引脚 TSSOP 封装。

表 1. DRV777 功能表<sup>(1)</sup>

输入 (IN1-IN7)	输出 (OUT1-OUT7)
L	H <sup>+(2)</sup>
H	L
Z	H <sup>+(2)</sup>

(1) L = 低电平 (接地); H = 高电平; Z = 高阻抗;  
(2) H<sup>+</sup> = 上拉电平



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### ORDERING INFORMATION<sup>(1)</sup>

T <sub>J</sub>	PART NUMBER	PACKAGE		TOP-SIDE MARKING
–40°C to 125°C	DRV777DR	16-Pin SOIC	Reel of 2500	DRV777
	DRV777PWR	16-Pin TSSOP	Reel of 2000	DRV777

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

### DEVICE INFORMATION

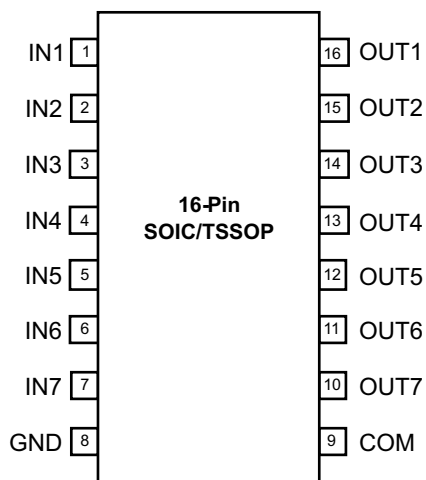


Figure 1. DRV777 PINOUT

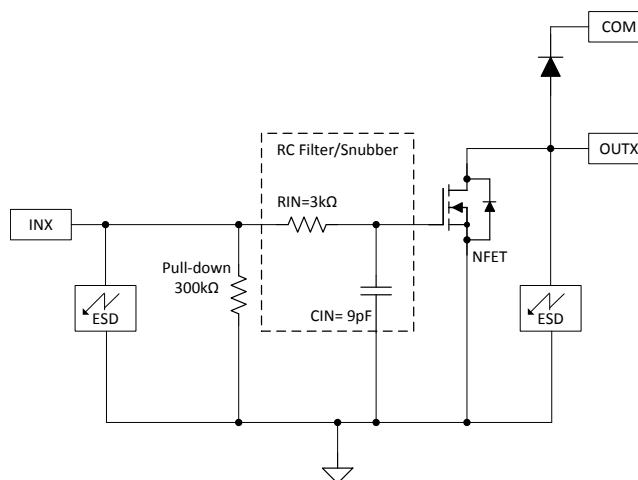


Figure 2. Channel Block Diagram

### DRV777 PIN DESCRIPTION

NAME	PIN NUMBER		DESCRIPTION
	16-SOIC	16-TSSOP	
IN1 – IN7	1–7	1–7	Logic Input Pins IN1 through IN7
GND	8	8	Ground Reference Pin
COM	9	9	Internal Free-Wheeling Diode Common Cathode Pin
OUT7 – OUT1	10–16	10–16	Channel Output Pins OUT7 through OUT1

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Specified at  $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  unless otherwise noted.

		VALUE		UNIT
		MIN	MAX	
$V_{IN}$	Pins IN1- IN7 to GND voltage	-0.3	5.5	V
$V_{OUT}$	Pins OUT1 – OUT7 to GND voltage		20	V
$V_{COM}$	Pin COM to GND voltage		20	V
$I_{GND}$	Max GND-pin continuous current ( $100^{\circ}\text{C} < T_J < +125^{\circ}\text{C}$ )		700	mA
	Max GND-pin continuous current ( $T_J < +100^{\circ}\text{C}$ )		1.0	A
$P_D$	Total device power dissipation at $T_A = 85^{\circ}\text{C}$	16 Pin - SOIC	0.86	W
		16 Pin - TSSOP	0.68	W
ESD	ESD Rating – HBM		2	kV
	ESD Rating – CDM		500	V
$T_J$	Operating virtual junction temperature	-55	150	$^{\circ}\text{C}$
$T_{stg}$	Storage temperature range	-55	150	$^{\circ}\text{C}$

- (1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## DISSIPATION RATINGS<sup>(1)(2)</sup>

BOARD	PACKAGE	$\theta_{JC}$	$\theta_{JA}$ <sup>(3)</sup>	DERATING FACTOR ABOVE $T_A = 25^{\circ}\text{C}$	$T_A < 25^{\circ}\text{C}$	$T_A = 70^{\circ}\text{C}$	$T_A = 85^{\circ}\text{C}$	$T_A = 105^{\circ}\text{C}$
High-K	16-Pin SOIC	46 $^{\circ}\text{C}/\text{W}$	75 $^{\circ}\text{C}/\text{W}$	13.33 mW/ $^{\circ}\text{C}$	1.66 W	1.06 W	0.86 W	0.59 W
High-K	16-Pin TSSOP	49 $^{\circ}\text{C}/\text{W}$	95 $^{\circ}\text{C}/\text{W}$	10.44 mW/ $^{\circ}\text{C}$	1.31 W	0.84 W	0.68 W	0.47 W

- (1) Maximum dissipation values for retaining device junction temperature of  $150^{\circ}\text{C}$   
(2) Refer to TI's design support web page at [www.ti.com/thermal](http://www.ti.com/thermal) for improving device thermal performance  
(3) Operating at the absolute  $T_{J-max}$  of  $150^{\circ}\text{C}$  can affect reliability– for higher reliability it is recommended to ensure  $T_J < 125^{\circ}\text{C}$

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OUT}$	Channel off-state output pull-up voltage			16	V
$V_{COM}$	COM pin voltage			16	V
$I_{OUT(ON)}$	Per channel continuous sink current	$V_{INx} = 3.3\text{V}$		100 <sup>(1)</sup>	mA
		$V_{INx} = 5.0\text{V}$		140 <sup>(1)</sup>	
$T_J$	Operating junction temperature	-40		125	$^{\circ}\text{C}$

- (1) 1) Refer to [ABSOLUTE MAXIMUM RATINGS](#) for  $T_J$  dependent absolute maximum GND-pin current

## ELECTRICAL CHARACTERISTICS

Specified over the recommended junction temperature range  $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  and over recommended operating conditions unless otherwise noted. Typical values are at  $T_J = 25^{\circ}\text{C}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>INPUTS IN1 THROUGH IN7 PARAMETERS</b>						
$V_{I(ON)}$	IN1–IN7 logic high input voltage	$V_{pull-up} = 3.3\text{ V}$ , $R_{pull-up} = 1\text{ k}\Omega$ , $I_{OUTX} = 3.2\text{ mA}$	1.65			V
$V_{I(OFF)}$	IN1–IN7 logic low input voltage	$V_{pull-up} = 3.3\text{ V}$ , $R_{pull-up} = 1\text{ k}\Omega$ , ( $I_{OUTX} < 20\text{ }\mu\text{A}$ )		0.4	0.6	V
$I_{I(ON)}$	IN1–IN7 ON state input current	$V_{pull-up} = 3.3\text{ V}$ , $V_{INx} = 3.3\text{ V}$		12	25	$\mu\text{A}$
$I_{I(OFF)}$	IN1–IN7 OFF state input leakage	$V_{pull-up} = 3.3\text{ V}$ , $V_{INx} = 0\text{ V}$			250	nA
<b>OUTPUTS OUT1 THROUGH OUT7 PARAMETERS</b>						
$V_{OL}$	OUT1–OUT7 low-level output voltage	$V_{INX} = 3.3\text{ V}$ , $I_{OUTX} = 100\text{ mA}$		0.36	0.49	V
		$V_{INX} = 5.0\text{ V}$ , $I_{OUTX} = 140\text{ mA}$		0.40		
$I_{OUT(ON)}$	OUT1–OUT7 ON-state continuous current <sup>(1) (2)</sup> at $V_{OUTX} = 0.4\text{ V}$	$V_{INX} = 3.3\text{ V}$ , $V_{OUTX} = 0.4\text{ V}$	80	100		mA
		$V_{INX} = 5.0\text{ V}$ , $V_{OUTX} = 0.4\text{ V}$	95	140		
$I_{OUT(OFF)(ICEX)}$	OUT1–OUT7 OFF-state leakage current	$V_{INX} = 0\text{ V}$ , $V_{OUTX} = V_{COM} = 16\text{ V}$		0.5		$\mu\text{A}$
<b>SWITCHING PARAMETERS<sup>(3)(4)</sup></b>						
$t_{PHL}$	OUT1–OUT7 logic high propagation delay	$V_{INX} = 3.3\text{ V}$ , $V_{pull-up} = 12\text{ V}$ , $R_{pull-up} = 1\text{ k}\Omega$		50	70	ns
$t_{PLH}$	OUT1–OUT7 logic low propagation delay	$V_{INX} = 3.3\text{ V}$ , $V_{pull-up} = 12\text{ V}$ , $R_{pull-up} = 1\text{ k}\Omega$		121	140	ns
$t_{CHANNEL}$	Channel to Channel delay	Over recommended operating conditions and with same test conditions on channels.		15	50	ns
$R_{PD}$	IN1–IN7 input pull-down Resistance		210k	300k	390k	$\Omega$
$\zeta$	IN1–IN7 Input filter time constant			9		ns
$C_{OUT}$	OUT1–OUT7 output capacitance	$V_{INX} = 3.3\text{ V}$ , $V_{OUTX} = 0.4\text{ V}$		15		pF
<b>FREE-WHEELING DIODE PARAMETERS<sup>(5)(4)</sup></b>						
$V_F$	Forward voltage drop	$I_{F-peak} = 140\text{ mA}$ , $V_F = V_{OUTX} - V_{COM}$		1.2		V
$I_{F-peak}$	Diode peak forward current			140		mA

- (1) The typical continuous current rating is limited by  $V_{OL} = 0.4\text{ V}$ . Whereas, absolute maximum operating continuous current may be limited by the Thermal Performance parameters listed in the Dissipation Rating Table and other Reliability parameters listed in the Recommended Operating Conditions Table.
- (2) Refer to the Absolute Maximum Ratings Table for  $T_J$  dependent absolute maximum GND-pin current.
- (3) Rise and Fall propagation delays,  $t_{PHL}$  and  $t_{PLH}$ , are measured between 50% values of the input and the corresponding output signal amplitude transition.
- (4) Guaranteed by design only. Validated during qualification. Not measured in production testing.
- (5) Not rated for continuous current operation – for higher reliability use an external freewheeling diode for inductive loads resulting in more than specified maximum free-wheeling. diode peak current across various temperature conditions

## APPLICATION INFORMATION

### TTL and other Logic Inputs

DRV777 input interface is specified for standard 1.8V, 3V and 5V CMOS logic interface. Refer to [Figure 8](#) and [Figure 9](#) to establish VOL and the corresponding typical load current levels for various input voltage ranges. Application Information section shows an implementation to drive 1.8V relays using DRV777.

### Input RC Snubber

DRV777 features an input RC snubber that helps prevent spurious switching in noisy environment. Connect an external 1kΩ to 5kΩ resistor in series with the input to further enhance DRV777's noise tolerance.

### High-impedance Input Drivers

DRV777 features a 300kΩ input pull-down resistor. The presence of this resistor allows the input drivers to be tri-stated. When a high-impedance driver is connected to a channel input the DRV777 detects the channel input as a low level input and remains in the OFF position. The input RC snubber helps improve noise tolerance when input drivers are in the high-impedance state.

### On-chip Power Dissipation

Use the below equation to calculate DRV777 on-chip power dissipation  $P_D$ :

$$P_D = \sum_{i=1}^N V_{OLi} \times I_{Li}$$

Where:

N is the number of channels active together.

$V_{OLi}$  is the  $OUT_i$  pin voltage for the load current  $I_{Li}$ .

(1)

### Thermal Reliability

It is recommended to limit DRV777 IC's die junction temperature to less than 125°C. The IC junction temperature is directly proportional to the on-chip power dissipation. Use the following equation to calculate the maximum allowable on-chip power dissipation for a target IC junction temperature:

$$PD_{(MAX)} = \frac{(T_{J(MAX)} - T_A)}{\theta_{JA}}$$

Where:

$T_{J(MAX)}$  is the target maximum junction temperature.

$T_A$  is the operating ambient temperature.

$\theta_{JA}$  is the package junction to ambient thermal resistance.

(2)

### Improving Package Thermal Performance

The package  $\theta_{JA}$  value under standard conditions on a High-K board is listed in the [DISSIPATION RATINGS](#).  $\theta_{JA}$  value depends on the PC board layout. An external heat sink and/or a cooling mechanism, like a cold air fan, can help reduce  $\theta_{JA}$  and thus improve device thermal capabilities. Refer to TI's design support web page at [www.ti.com/thermal](http://www.ti.com/thermal) for a general guidance on improving device thermal performance.

## Application Examples

### One Amp Unipolar DC Motor Driver

An implementation of DRV777 for driving a unipolar DC motor is shown in Figure 3. With all of the channels tied together and the input being driven at 5V, the driver can sink 1A of current. With a VOL of 0.4V this creates a driver with 400mΩ. The input snubber circuitry is great for PWM applications that need high noise immunity. These two features make DRV777 an ideal choice for power efficient high duty cycle motor driving applications.

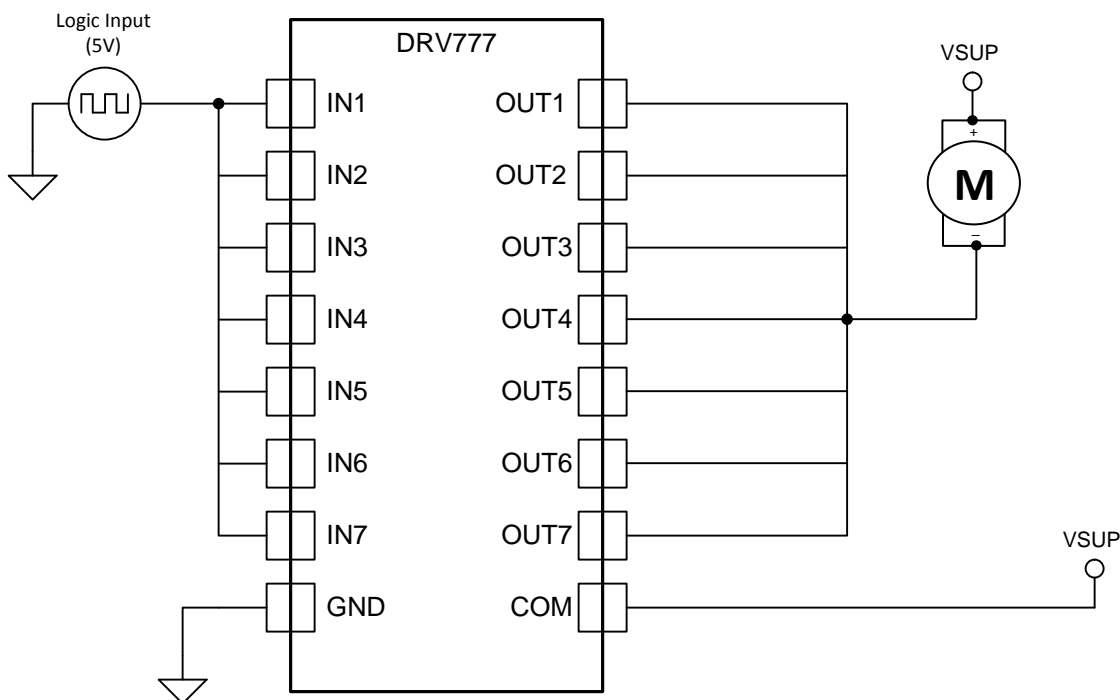
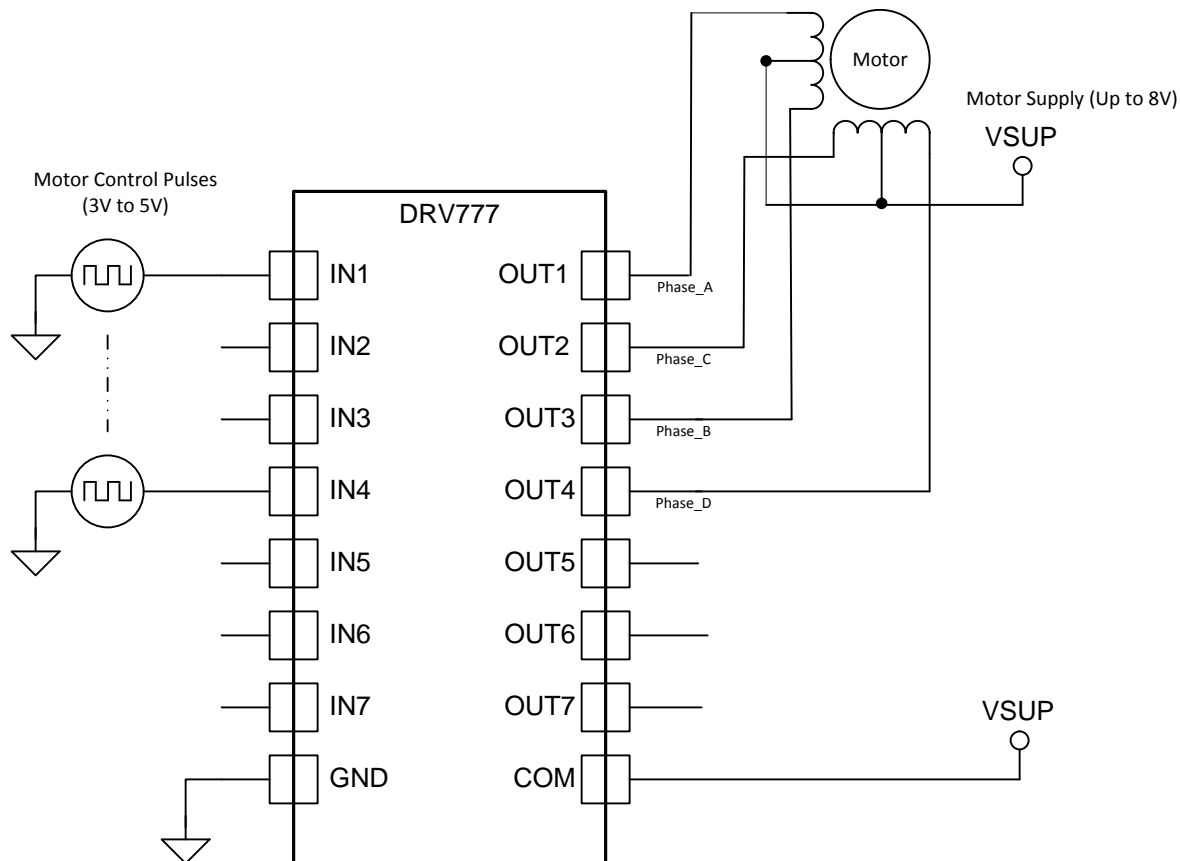


Figure 3. DRV777 as a DC Motor Driver

## Unipolar Stepper Motor Driver

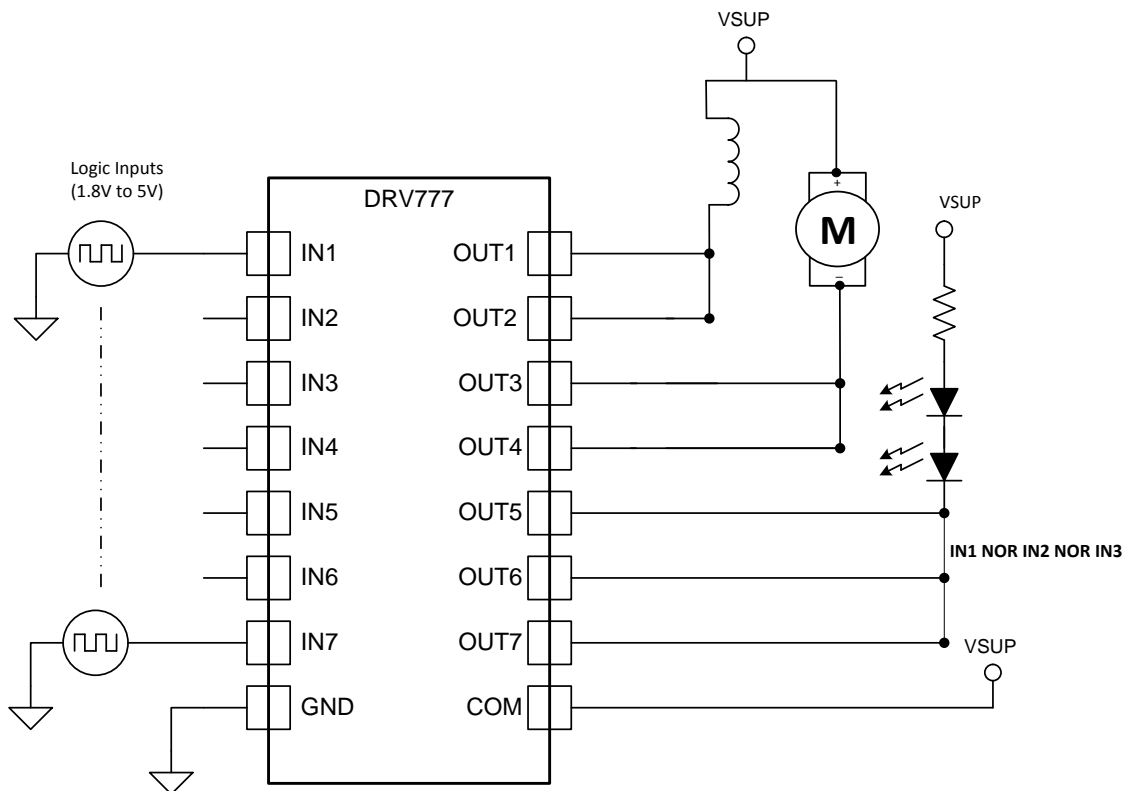
Figure 4 shows an implementation of DRV777 for driving a unipolar stepper motor. The unconnected input channels can be used for other functions. When an input pin is left open the internal 300kΩ pull down resistor pulls the respective input pin to GND potential. For higher noise immunity use an external short across an unconnected input and GND pins.



**Figure 4. DRV777 as a Stepper Motor Driver**

## Multi-Purpose Sink Driver

When configured as per [Figure 5](#) DRV777 can be used as a multi-purpose driver. The output channels can be tied together to sink more current. DRV777 can easily drive motors, relays & LEDs with little power dissipation. The COM pin must be tied to the supply of whichever inductive load is to be protected by the free-wheeling diode.

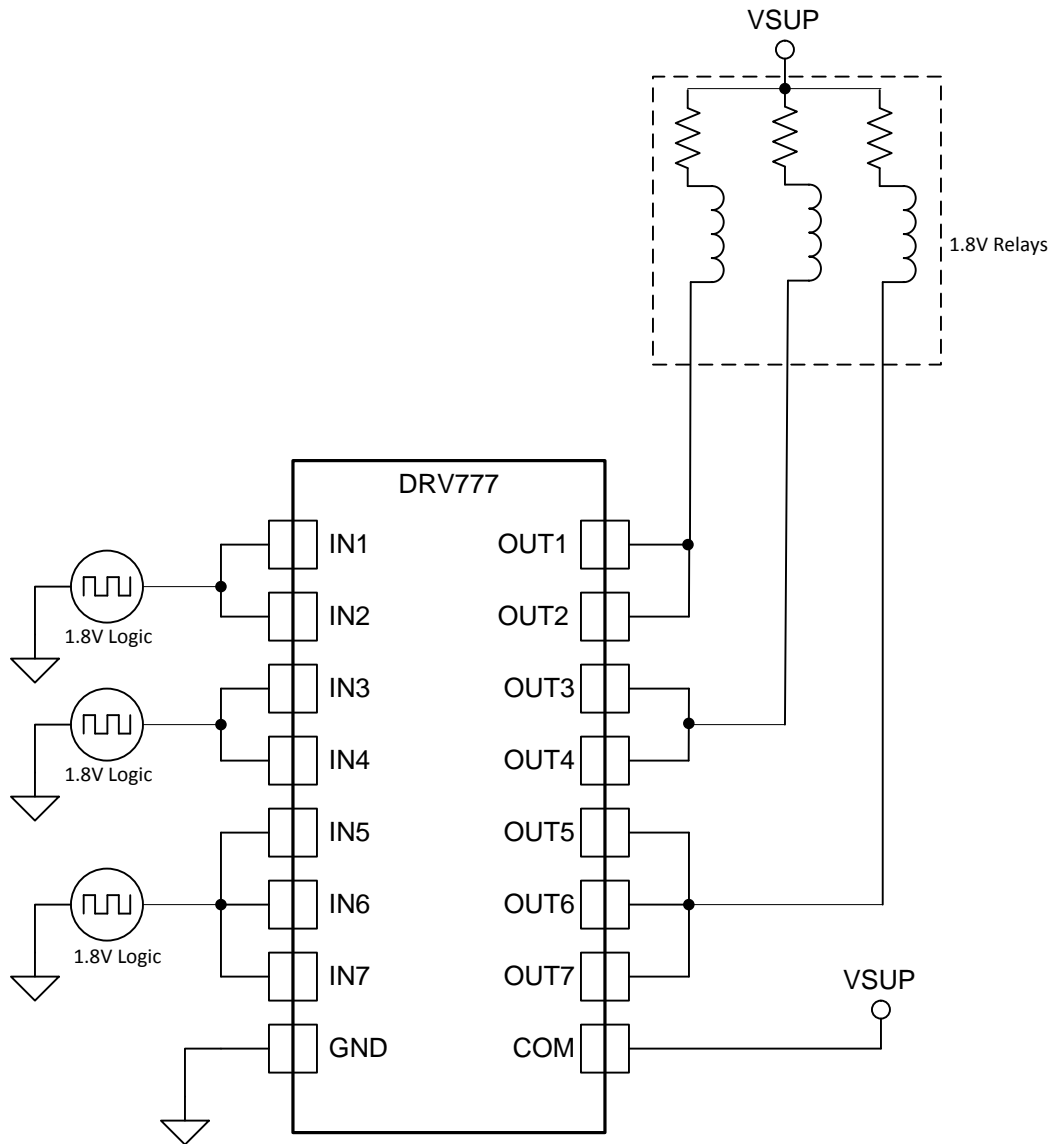


**Figure 5. DRV777 Multi-Purpose Sink Driver Application**



## 1.8V Relay Driver

To drive lower voltage relays, like 1.8V, connect two or more adjacent channels in parallel as shown in [Figure 6](#). Connecting several channels in parallel lowers the channel output resistance and thus minimizes VOL for a fixed current. DRV777 can be used for driving 3V, 5V and 12V relays with similar implementation.



**Figure 6. DRV777 Driving 1.8V Relays**

## TYPICAL CHARACTERISTICS

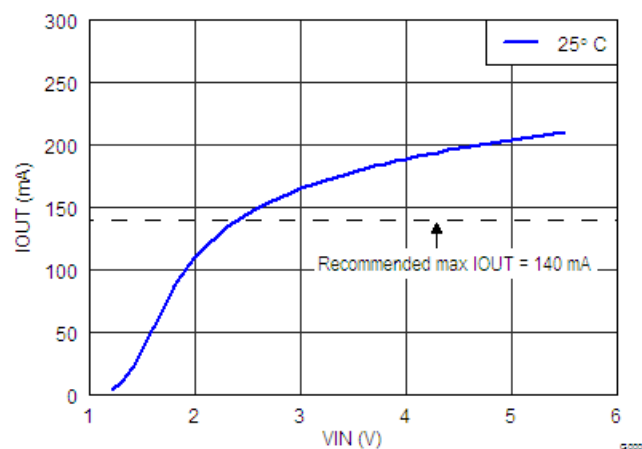
 $T_A = +25^\circ\text{C}$ 

Figure 7. Load Current 1-Channel; VOL=0.4V

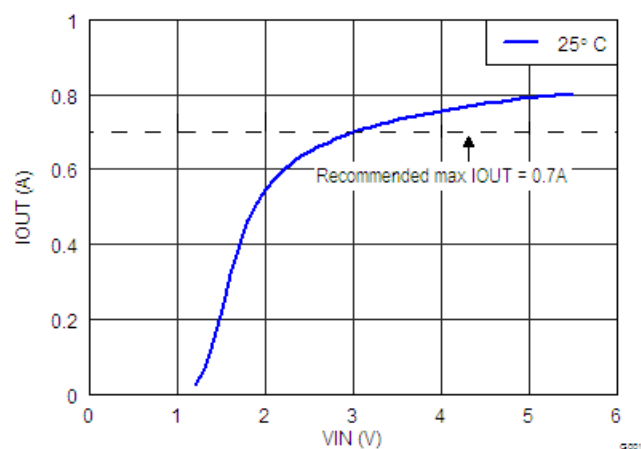


Figure 8. Load Current 7-Channels in parallel; VOL=0.4V

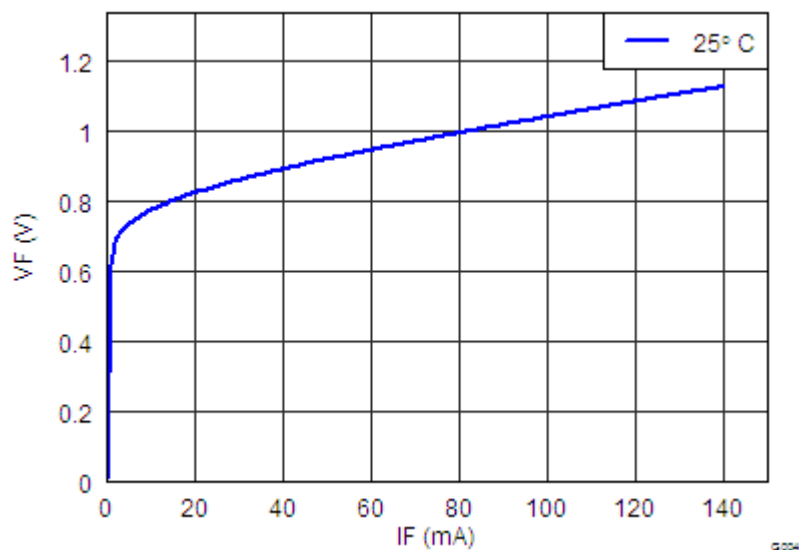


Figure 9. Freewheeling Diode VF versus IF

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">DRV777DR</a>	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	DRV777
DRV777DR.B	Active	Production	SOIC (D)   16	2500   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	DRV777
<a href="#">DRV777PWR</a>	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	DRV777
DRV777PWR.B	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	DRV777

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

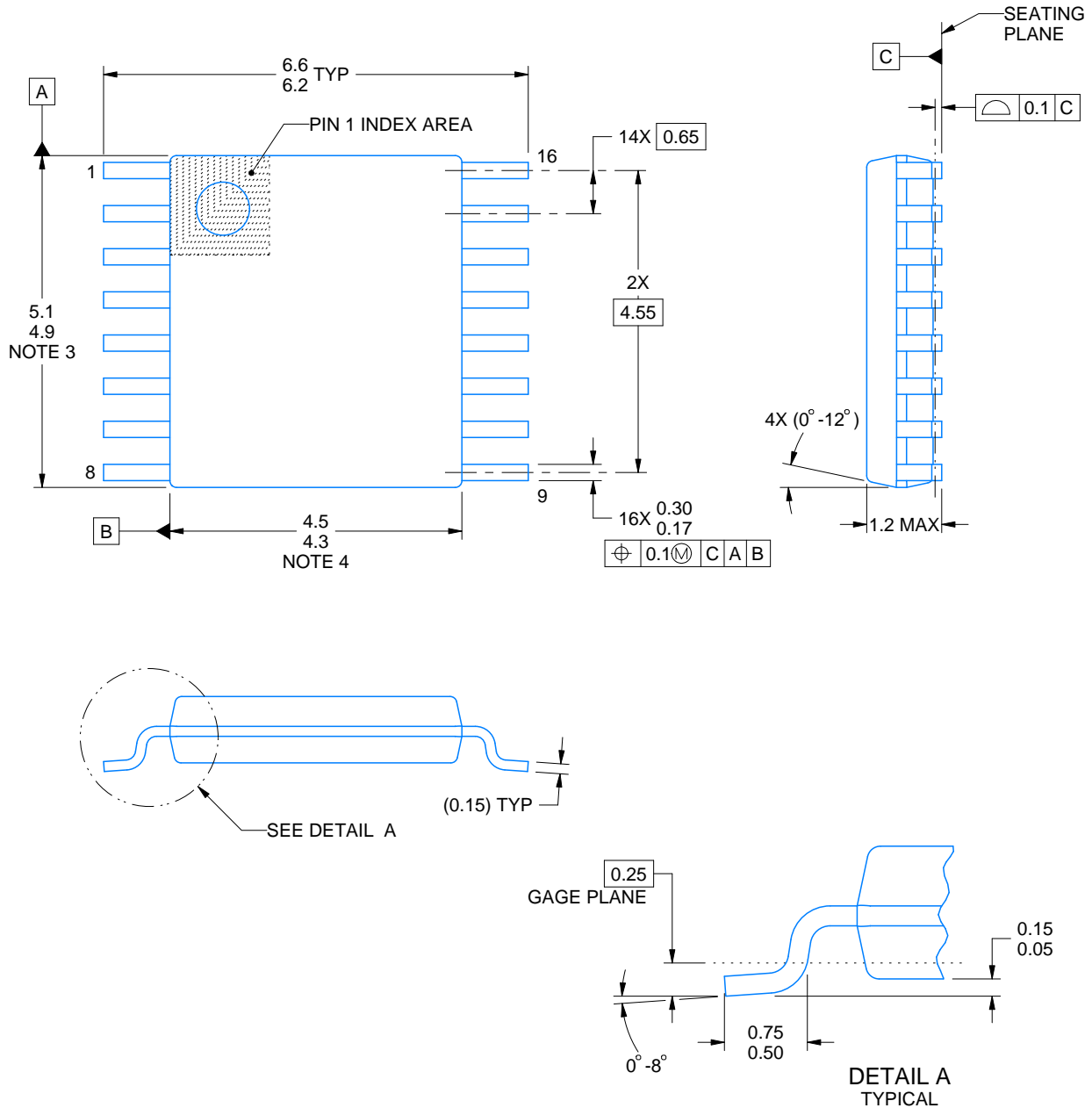
<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

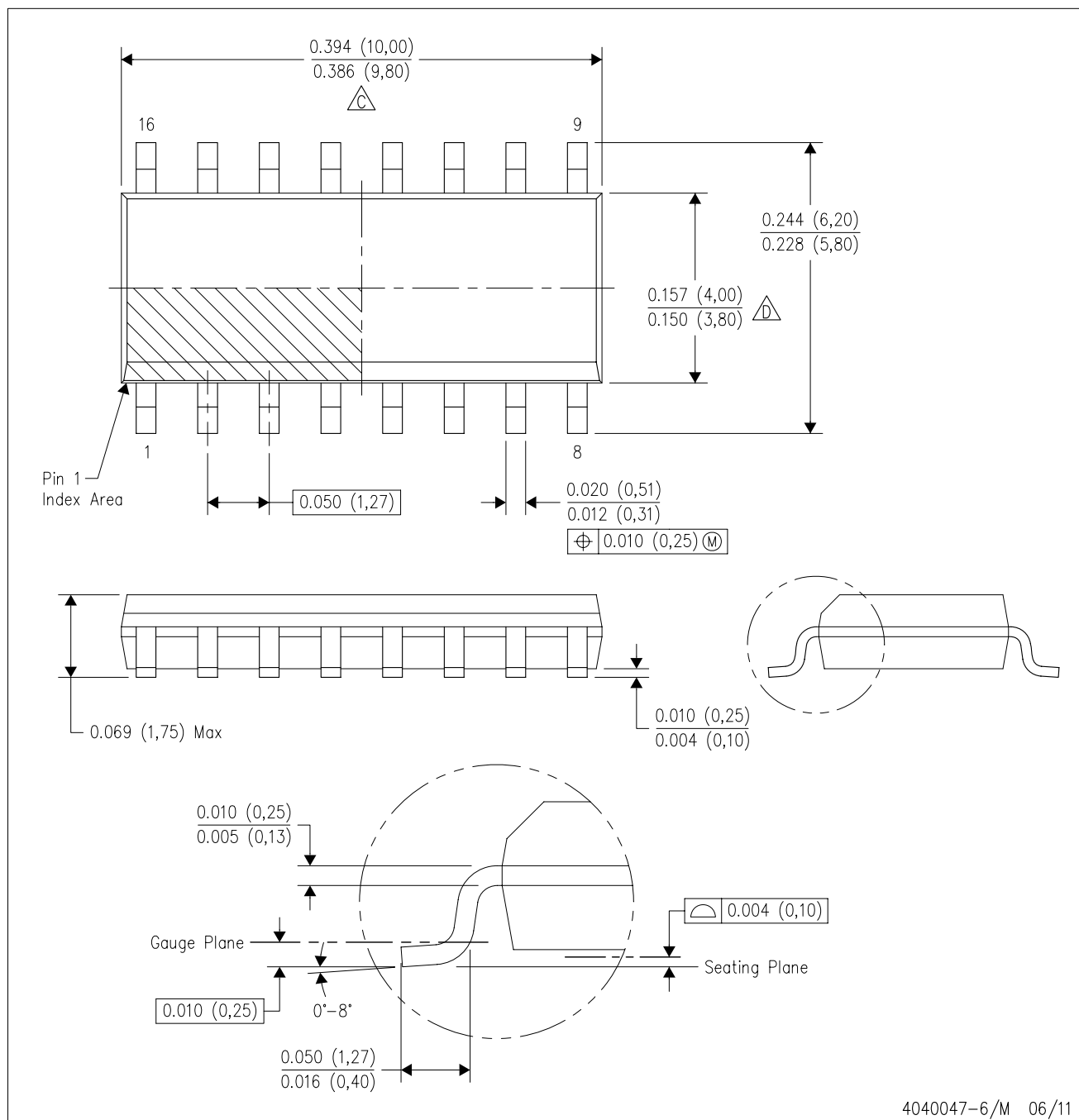
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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

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