DS90C032B LVDS Quad CMOS Differential Line Receiver

Check for Samples: DS90C032B

FEATURES

- **>155.5 Mbps (77.7 MHz) Switching Rates**
- **Accepts Small Swing (350 mV) Differential Signal Levels**
- **High Impedance LVDS Inputs with Power Down**
- **Ultra Low Power Dissipation**
- **600 ps Maximum Differential Skew (5V, 25°C)**
- **6.0 ns Maximum Propagation Delay**
- **Industrial Operating Temperature Range**
- **Available in Surface Mount Packaging (SOIC)**
- **Pin Compatible with DS26C32A, MB570 (PECL) and 41LF (PECL)**
- **Supports OPEN and Terminated Input Failsafe**
- **Conforms to ANSI/TIA/EIA-644 LVDS Standard**

DESCRIPTION

The DS90C032B is a quad CMOS differential line receiver designed for applications requiring ultra low power dissipation and high data rates. The device supports data rates in excess of 155.5 Mbps (77.7 MHz) and uses Low Voltage Differential Signaling (LVDS) technology.

The DS90C032B accepts low voltage (350 mV) differential input signals and translates them to CMOS (TTL compatible) output levels. The receiver supports a TRI-STATE function that may be used to multiplex outputs. The receiver also supports OPEN Failsafe and terminated (100Ω) input Failsafe with the addition of external failsafe biasing. Receiver output will be HIGH for both Failsafe conditions.

The DS90C032B provides power-off high impedance LVDS inputs. This feature assures minimal loading effect on the LVDS bus lines when V_{CC} is not present.

The DS90C032B and companion line driver (DS90C031B) provide a new alternative to high power pseudo-ECL devices for high-speed point-to-point interface applications.

Connection Diagram

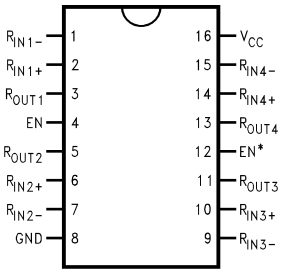


Figure 1. Dual-In-Line Top View
See Package Number D (R-PDSO-G16)

Functional Diagram

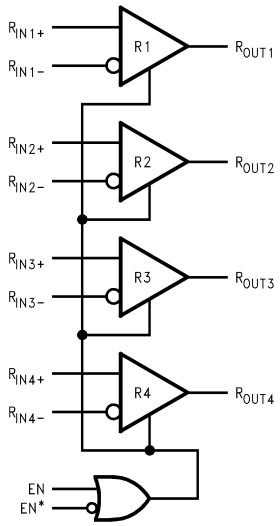


Table 1. Receiver Truth Table

ENABLES		INPUTS	OUTPUT
EN	**EN***	**$R_{IN+} - R_{IN-}$**	**R_{OUT}**
L	H	X	Z
All other combinations of ENABLE inputs		$V_{ID} \geq 0.1V$	H
		$V_{ID} \leq -0.1V$	L
		Failsafe OPEN or Terminated	H

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)

Supply Voltage (V_{CC})		−0.3V to +6V
Input Voltage (R_{IN+}, R_{IN-})		−0.3V to +5.8V
Enable Input Voltage (EN, EN*)		−0.3V to (V_{CC} + 0.3V)
Output Voltage (R_{OUT})		−0.3V to (V_{CC} + 0.3V)
Maximum Package Power Dissipation at +25°C		1025 mW
Derate Power Dissipation		8.2 mW/°C above +25°C
Storage Temperature Range		−65°C to +150°C
Maximum Lead Temperature, Soldering (4 seconds)		+260°C
Maximum Junction Temperature		+150°C
ESD Ratings	HBM, 1.5 kΩ, 100 pF	≥ 2kV
	EIAJ, 0 Ω, 200 pF	≥ 250V

(1) “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the devices should be operated at these limits. “Electrical Characteristics” specifies conditions of device operation.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	+4.5	+5.0	+5.5	V
Receiver Input Voltage	GND		2.4	V
Operating Free Air Temperature (T_A)	−40	+25	+85	°C

Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified[1][2]

Symbol	Parameter	Conditions		Pin	Min	Typ	Max	Units
V_{TH}	Differential Input High Threshold	V_{CM} = +1.2V		R_{IN+}, R_{IN-}			+100	mV
V_{TL}	Differential Input Low Threshold				−100			mV
I_{IN}	Input Current	V_{IN} = +2.4V	V_{CC} = 5.5V or 0V		−10	±1	+10	µA
		V_{IN} = 0V			−10	±1	+10	µA
V_{OH}	Output High Voltage	I_{OH} = −0.4 mA, V_{ID} = +200 mV		R_{OUT}	3.8	4.9		V
		I_{OH} = −0.4 mA, Input terminated			3.8	4.9		V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA, V_{ID} = −200 mV				0.07	0.3	V
I_{OS}	Output Short Circuit Current	Enabled, V_{OUT} = 0V[3]			−15	−60	−100	mA
I_{OZ}	Output TRI-STATE Current	Disabled, V_{OUT} = 0V or V_{CC}			−10	±1	+10	µA
V_{IH}	Input High Voltage			EN, EN*	2.0			V
V_{IL}	Input Low Voltage						0.8	V
I_I	Input Current				−10	±1	+10	µA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−1.5	−0.8		V
I_{CC}	No Load Supply Current, Receivers Enabled	EN, EN* = V_{CC} or GND, Inputs Open		V_{CC}		3.5	10	mA
		EN, EN* = 2.4 or 0.5, Inputs Open				3.7	11	mA
I_{CCZ}	No Load Supply Current, Receivers Disabled	EN = GND, EN* = V_{CC}, Inputs Open				3.5	10	mA

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.
(2) All typicals are given for: V_{CC} = +5.0V, T_A = +25°C.
(3) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only. Only one output should be shorted at a time, do not exceed maximum junction temperature specification.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C[1][2][3]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	C_L = 5 pF, V_{ID} = 200 mV, See Figure 2 and Figure 3	1.5	3.40	5.0	ns
t_{PLHD}	Differential Propagation Delay Low to High		1.5	3.48	5.0	ns
t_{SKD}	Differential Skew $\lvert t_{PHLD} - t_{PLHD} \rvert$		0	80	600	ps
t_{SK1}	Channel-to-Channel Skew[4]		0	0.6	1.0	ns
t_{TLH}	Rise Time			0.5	2.0	ns
t_{THL}	Fall Time			0.5	2.0	ns
t_{PHZ}	Disable Time High to Z	R_L = 2 kΩ, C_L = 10 pF, See Figure 4 and Figure 5		10	15	ns
t_{PLZ}	Disable Time Low to Z			10	15	ns
t_{PZH}	Enable Time Z to High			4	10	ns
t_{PZL}	Enable Time Z to Low			4	10	ns

(1) All typicals are given for: V_{CC} = +5.0V, T_A = +25°C.
(2) Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50Ω, t_r and t_f (0%–100%) ≤ 1 ns for R_{IN} and t_r and t_f ≤ 6 ns for EN or EN*.
(3) C_L includes probe and jig capacitance.
(4) Channel-to-Channel Skew is defined as the difference between the propagation delay of one channel and that of the others on the same chip with an event on the inputs.

Switching Characteristics

V_{CC} = +5.0V ± 10%, T_A = −40°C to +85°C(1)(2)(3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHLD}	Differential Propagation Delay High to Low	C_L = 5 pF, V_{ID} = 200 mV, See Figure 2 and Figure 3	1.0	3.40	6.0	ns
t_{PLHD}	Differential Propagation Delay Low to High		1.0	3.48	6.0	ns
t_{SKD}	Differential Skew $\|t_{PHLD} - t_{PLHD}\|$		0	0.08	1.2	ns
t_{SK1}	Channel-to-Channel Skew(4)		0	0.6	1.5	ns
t_{SK2}	Chip to Chip Skew(5)				5.0	ns
t_{TLH}	Rise Time			0.5	2.5	ns
t_{THL}	Fall Time			0.5	2.5	ns
t_{PHZ}	Disable Time High to Z	R_L = 2 kΩ, C_L = 10 pF, See Figure 4 and Figure 5		10	20	ns
t_{PLZ}	Disable Time Low to Z			10	20	ns
t_{PZH}	Enable Time Z to High			4	15	ns
t_{PZL}	Enable Time Z to Low			4	15	ns

(1) All typicals are given for: V_{CC} = +5.0V, T_A = +25°C.
(2) Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50Ω, t_r and t_f (0%–100%) ≤ 1 ns for R_{IN} and t_r and t_f ≤ 6 ns for EN or EN*.
(3) C_L includes probe and jig capacitance.
(4) Channel-to-Channel Skew is defined as the difference between the propagation delay of one channel and that of the others on the same chip with an event on the inputs.
(5) Chip to Chip Skew is defined as the difference between the minimum and maximum specified differential propagation delays.

Parameter Measurement Information

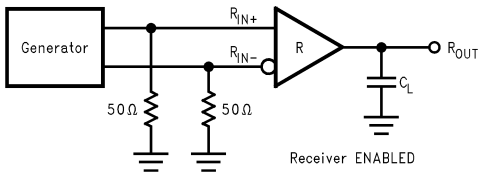


Figure 2. Receiver Propagation Delay and Transition Time Test Circuit

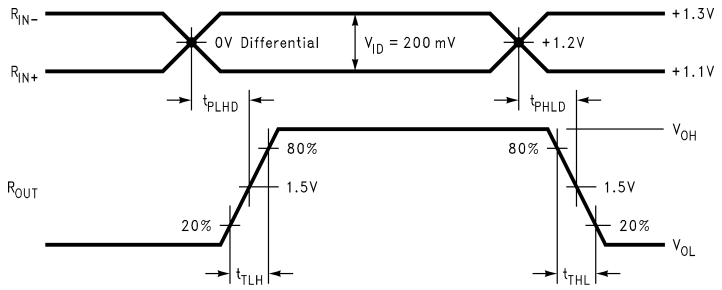
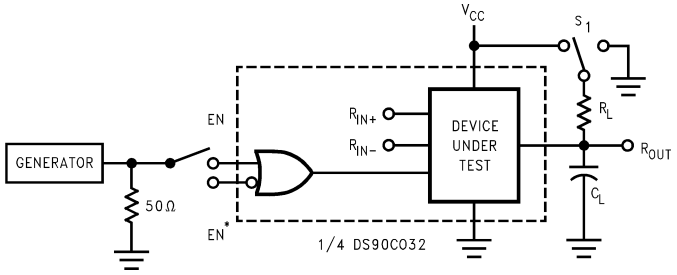


Figure 3. Receiver Propagation Delay and Transition Time Waveforms

Parameter Measurement Information (continued)



C_L includes load and test jig capacitance.
$S_1 = V_{CC}$ for t_{PZL} and t_{PLZ} measurements.
S_1 = GND for t_{PZH} and t_{PHZ} measurements.

Figure 4. Receiver TRI-STATE Delay Test Circuit

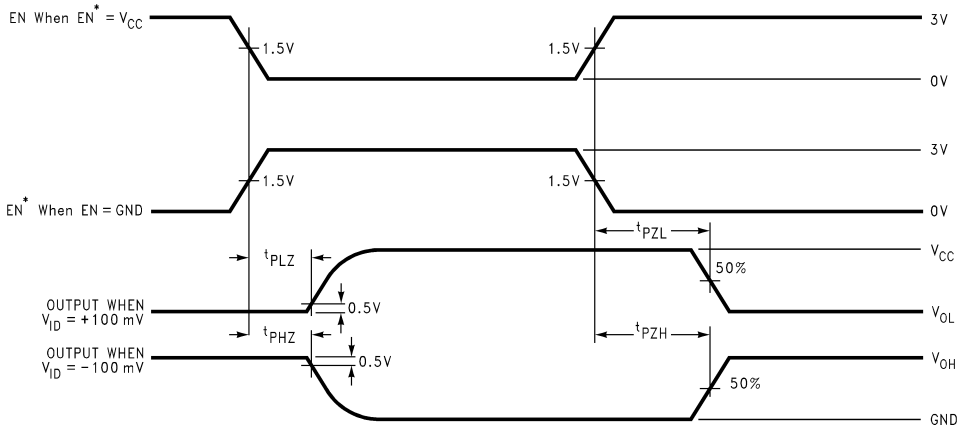


Figure 5. Receiver TRI-STATE Delay Waveforms

Typical Application

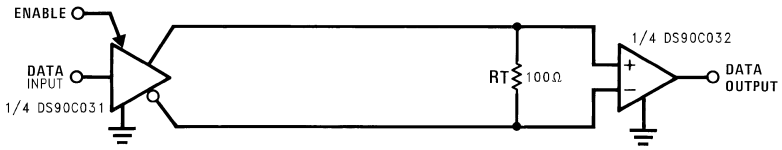


Figure 6. Point-to-Point Application

APPLICATIONS INFORMATION

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in *Figure 6*. This configuration provides a clean signaling environment for the quick edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically the characteristic impedance of the media is in the range of 100Ω. A termination resistor of 100Ω should be selected to match the media, and is located as close to the receiver input pins as possible. The termination resistor converts the current sourced by the driver into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

TheDS90C032B differential line receiver is capable of detecting signals as low as 100 mV, over a ±1V common-mode range centered around +1.2V. This is related to the driver offset voltage which is typically +1.2V. The driven signal is centered around this voltage and may shift ±1V around this center point. The ±1V shifting may be the result of a ground potential difference between the driver's ground reference and the receiver's ground reference, the common-mode effects of coupled noise, or a combination of the two. Both receiver input pins should honor their specified operating input voltage range of 0V to +2.4V (measured from each pin to ground), exceeding these limits may turn on the ESD protection circuitry which will clamp the bus voltages.

RECEIVER FAILSAFE

The LVDS receiver is a high gain, high speed device that amplifies a small differential signal (20mV) to CMOS logic levels. Due to the high gain and tight threshold of the receiver, care should be taken to prevent noise from appearing as a valid signal.

The receiver's internal failsafe circuitry is designed to source/sink a small amount of current, providing failsafe protection (a stable known state of HIGH output voltage) for floating and terminated (100Ω) receiver inputs in low noise environment (differential noise < 10mV).

1. **Open Input Pins.**

   TheDS90C032B is a quad receiver device, and if an application requires only 1, 2, or 3 receivers, the unused channel(s) inputs should be left OPEN. Do not tie unused receiver inputs to ground or any other voltages. The input is biased by internal high value pull up and pull down resistors to set the output to a HIGH state. This internal circuitry will ensure a HIGH, stable output state for open inputs.

2. **Terminated Input.** TheDS90C032B requires external failsafe biasing for terminated input failsafe.

   Terminated input failsafe is the case of a receiver that has a 100Ω termination across its inputs and the driver is in the following situations. Unplugged from the bus, or the driver output is in TRI-STATE or in power-off condition. The use of external biasing resistors provide a small bias to set the differential input voltage while the line is un-driven, and therefore the receiver output will be in HIGH state. If the driver is removed from the bus but the cable is still present and floating, the unplugged cable can become a floating antenna that can pick up noise. The LVDS receiver is designed to detect very small amplitude and width signals and recover them to standard logic levels. Thus, if the cable picks up more than 10mV of differential noise, the receiver may respond. To insure that any noise is seen as common-mode and not differential, a balanced interconnect and twisted pair cables is recommended, as they help to ensure that noise is coupled common to both lines and rejected by the receivers.

3. **Operation in environment with greater than 10mV differential noise.**

   TI recommends external failsafe biasing on its LVDS receivers for a number of system level and signal quality reasons. First, only an application that requires failsafe biasing needs to employ it. Second, the amount of failsafe biasing is now an application design parameter and can be custom tailored for the specific application. In applications in low noise environments, they may choose to use a very small bias if any. For applications with less balanced interconnects and/or in high noise environments they may choose to boost failsafe further. TI's "LVDS Owner's Manual provides detailed calculations for selecting the proper failsafe biasing resistors. Third, the common-mode voltage is biased by the resistors during the un-driven state. This is selected to be close to the nominal driver offset voltage (V_{OS}). Thus when switching between driven and un-driven states, the common-mode modulation on the bus is held to a minimum.

For additional Failsafe Biasing information, please refer to Application Note AN-1194 for more detail.

The footprint of theDS90C032B is the same as the industry standard 26LS32 Quad Differential (RS-422) Receiver.

For additional LVDS application information, please refer to TI's LVDS Owner's Manual available through TI's website http://www.ti.com/lvds

Pin Descriptions

Pin No.	Name	Description
2, 6, 10, 14	R_{IN+}	Non-inverting receiver input pin
1, 7, 9, 15	R_{IN-}	Inverting receiver input pin
3, 5, 11, 13	R_{OUT}	Receiver output pin
4	EN	Active high enable pin, OR-ed with EN*
12	EN*	Active low enable pin, OR-ed with EN
16	V_{CC}	Power supply pin, +5V ± 10%
8	GND	Ground pin

Typical Performance Characteristics

Output High Voltage vs Power Supply Voltage

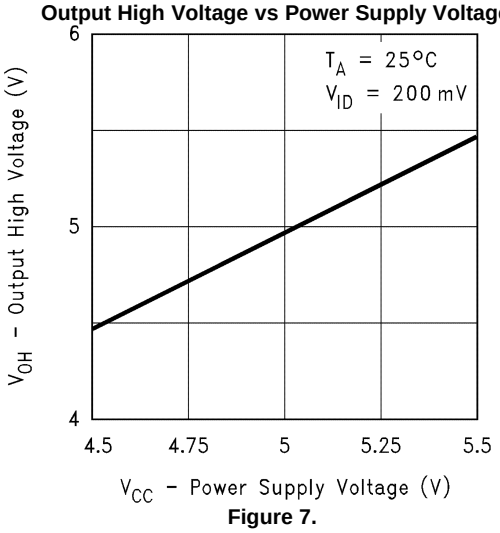


Figure 7.

Output High Voltage vs Ambient Temperature

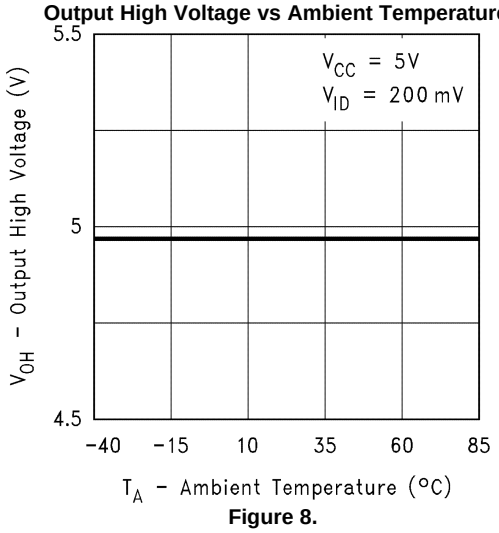


Figure 8.

Output Low Voltage vs Power Supply Voltage

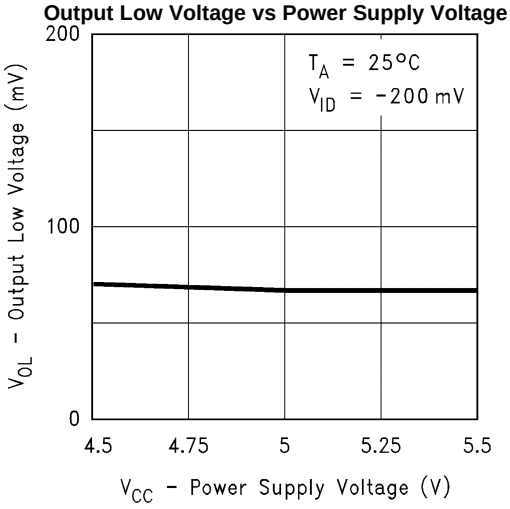


Figure 9.

Output Low Voltage vs Ambient Temperature

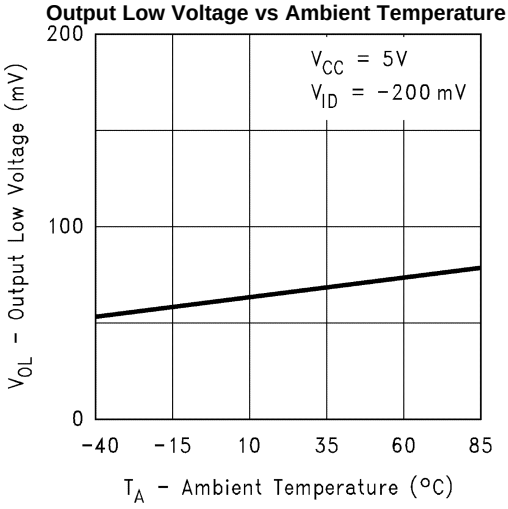


Figure 10.

Output Short Circuit Current vs Power Supply Voltage

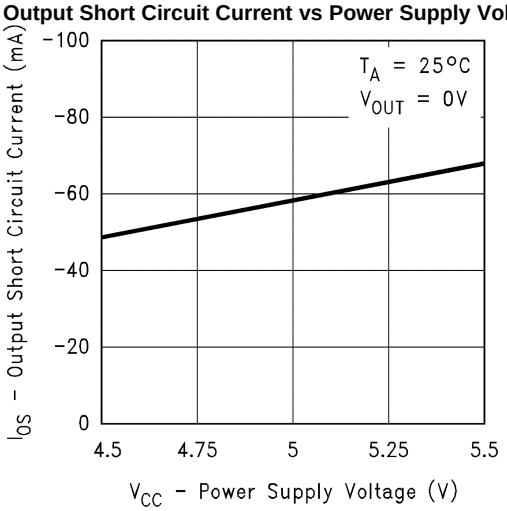


Figure 11.

Output Short Circuit Current vs Ambient Temperature

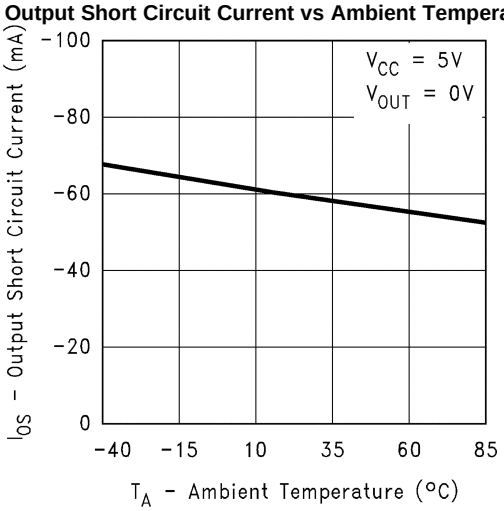


Figure 12.

Typical Performance Characteristics (continued)

Differential Propagation Delay vs Power Supply Voltage

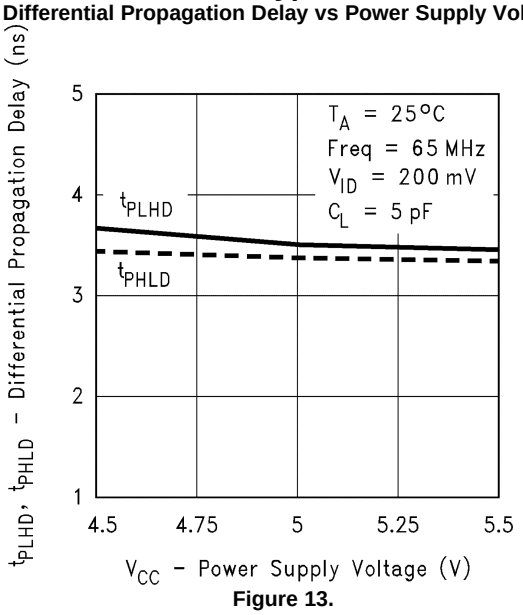


Figure 13.

Differential Propagation Delay vs Ambient Temperature

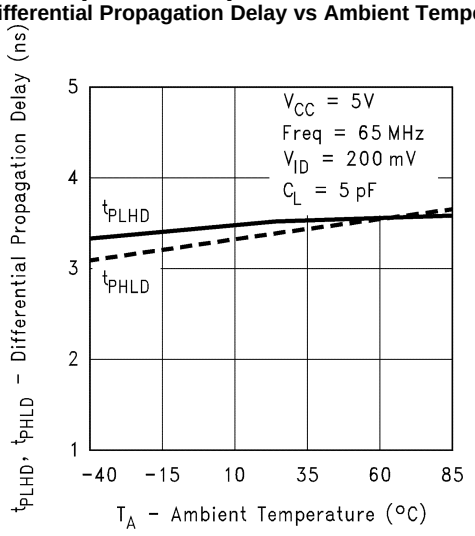


Figure 14.

Differential Skew vs Power Supply Voltage

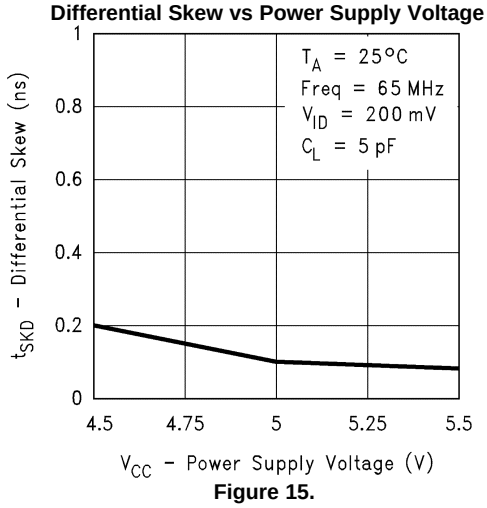


Figure 15.

Differential Skew vs Ambient Temperature

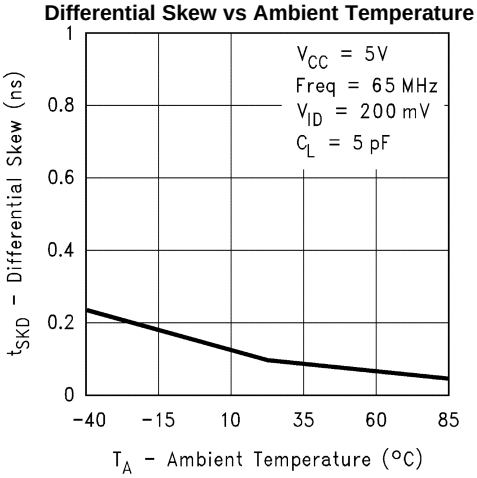


Figure 16.

Transition Time vs Power Supply Voltage

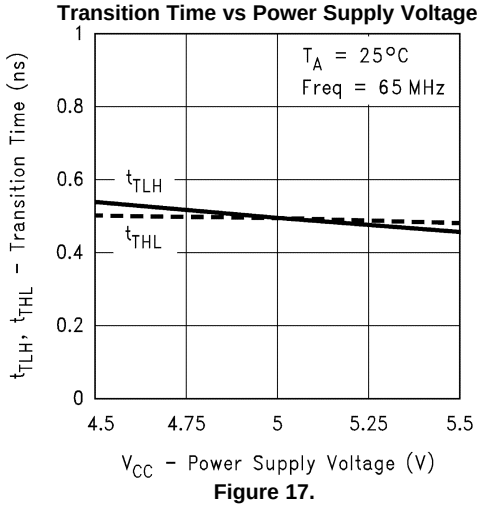


Figure 17.

Transition Time vs Ambient Temperature

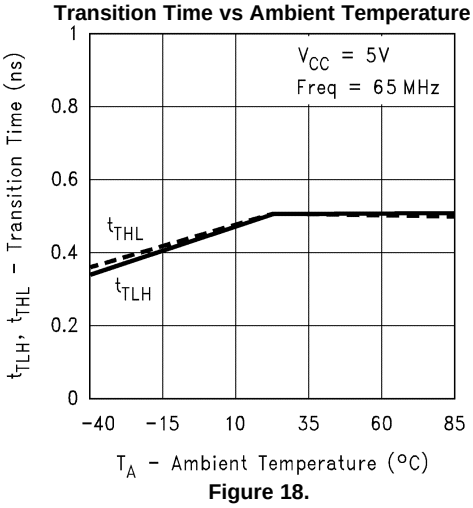


Figure 18.

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	9

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS90C032BTM/NOPB	Active	Production	SOIC (D) | 16	48 | TUBE	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 85	DS90C032BTM
DS90C032BTM/NOPB.A	Active	Production	SOIC (D) | 16	48 | TUBE	Yes	SN	Level-1-260C-UNLIM	-40 to 85	DS90C032BTM
DS90C032BTMX/NOPB	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 85	DS90C032BTM
DS90C032BTMX/NOPB.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	DS90C032BTM
DS90C032BTMX/NOPB.B	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

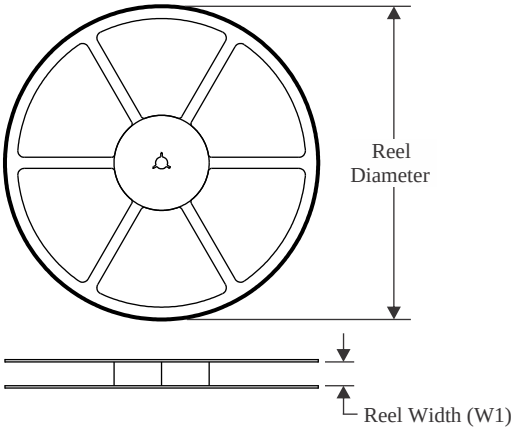
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

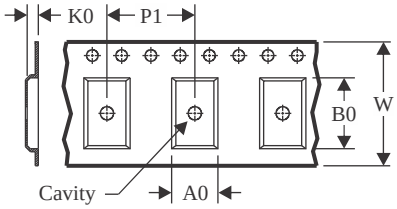
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

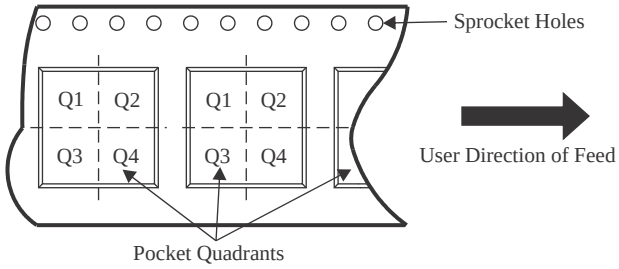


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

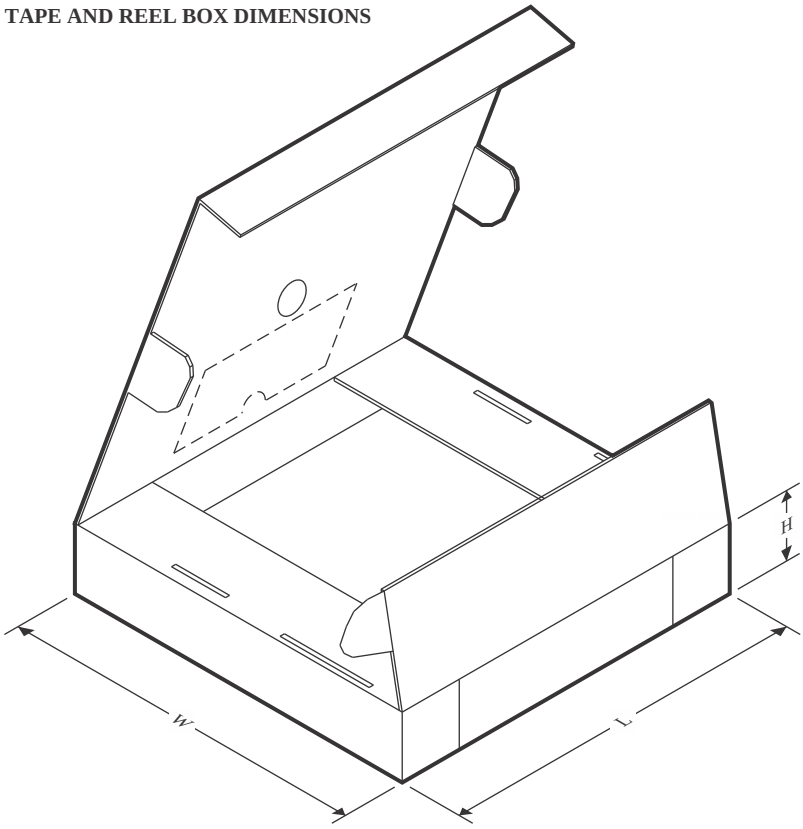
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90C032BTMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

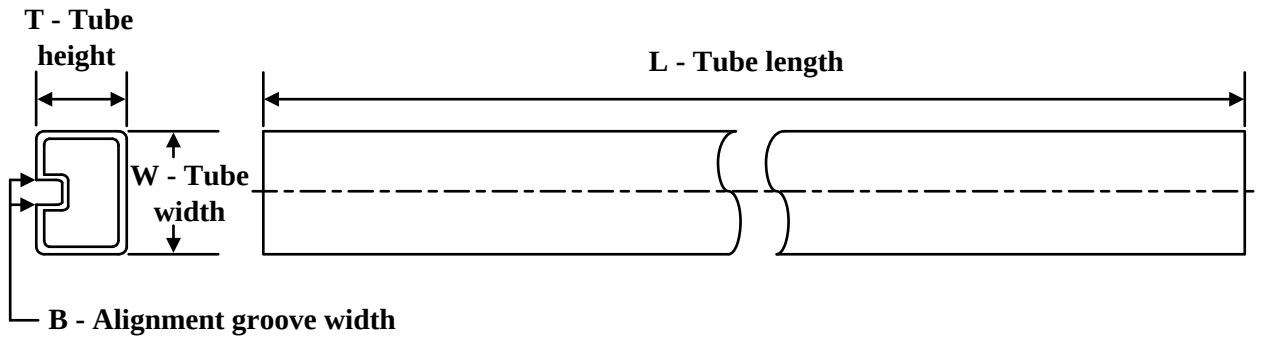
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90C032BTMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0

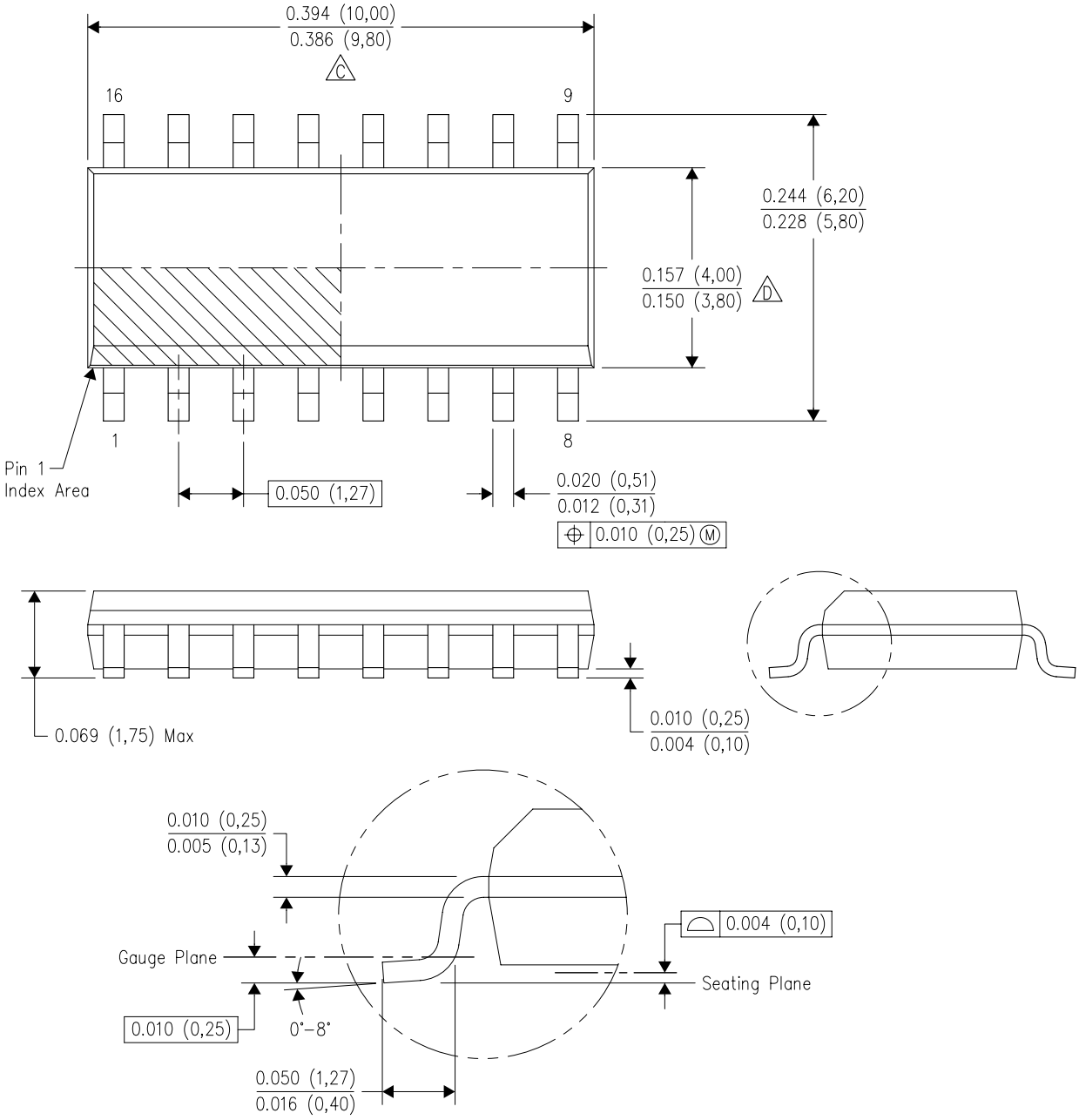
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DS90C032BTM/NOPB	D	SOIC	16	48	495	8	4064	3.05
DS90C032BTM/NOPB.A	D	SOIC	16	48	495	8	4064	3.05

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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