

DS91M040 125 MHz Quad M-LVDS Transceiver

Check for Samples: DS91M040

FEATURES

- DC 125 MHz / 250 Mbps Low Jitter, Low Skew, Low Power Operation
- Wide Input Common Mode Voltage Range Allows up to ±1V of GND Noise
- Conforms to TIA/EIA-899 M-LVDS Standard
- Pin Selectable M-LVDS Receiver Type (1 or 2)
- Controlled Transition Times (2.0 ns typ)
 Minimize Reflections
- 8 kV ESD on M-LVDS I/O pins protects adjoining components
- Flow-Through Pinout Simplifies PCB Layout
- Small 5 mm x 5 mm WQFN-32 Space Saving Package

APPLICATIONS

- Multidrop / Multipoint Clock and Data Distribution
- High-Speed, Low Power, Short-Reach Alternative to TIA/EIA-485/422
- Clock Distribution in AdvancedTCA (ATCA) and MicroTCA (µTCA, uTCA) Backplanes

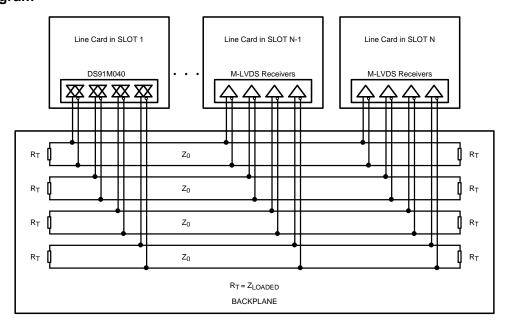
DESCRIPTION

The DS91M040 is a quad M-LVDS transceiver designed for driving / receiving clock or data signals to / from up to four multipoint networks.

M-LVDS (Multipoint LVDS) is a new family of bus interface devices based on LVDS technology specifically designed for multipoint and multidrop cable and backplane applications. It differs from standard LVDS in providing increased drive current to handle double terminations that are required in multipoint applications. Controlled transition times minimize reflections that are common in multipoint configurations due to unterminated stubs. M-LVDS devices also have a very large input common mode voltage range for additional noise margin in heavily loaded and noisy backplane environments.

A single DS91M040 channel is a half-duplex transceiver that accepts LVTTL/LVCMOS signals at the driver inputs and converts them to differential M-LVDS signal levels. The receiver inputs accept low voltage differential signals (LVDS, BLVDS, M-LVDS, LVPECL and CML) and convert them to 3V LVCMOS signals. The DS91M040 supports both M-LVDS type 1 and type 2 receiver inputs.

System Diagram

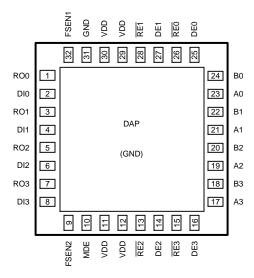


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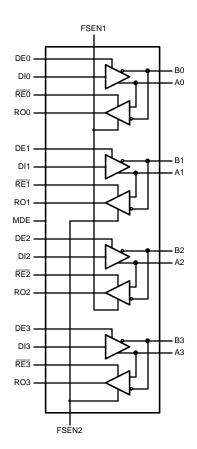
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Connection Diagram



Logic Diagram





PIN DESCRIPTIONS

Number	Name	I/O, Type	Description
1, 3, 5, 7	RO	O, LVCMOS	Receiver output pin.
26, 28, 13, 15	RE	I, LVCMOS	Receiver enable pin: When \overline{RE} is high, the receiver is disabled. When \overline{RE} is low, the receiver is enabled. There is a 300 k Ω pullup resistor on this pin.
25, 27, 14, 16	DE	I, LVCMOS	Driver enable pin: When DE is low, the driver is disabled. When DE is high, the driver is enabled. There is a 300 k Ω pulldown resistor on this pin.
2, 4, 6, 8	DI	I, LVCMOS	Driver input pin.
31, DAP	GND	Power	Ground pin and pad.
17, 19, 21, 23	Α	I/O, M-LVDS	Non-inverting driver output pin/Non-inverting receiver input pin
18, 20, 22, 24	В	I/O, M-LVDS	Inverting driver output pin/Inverting receiver input pin
11, 12, 29, 30	V_{DD}	Power	Power supply pin, +3.3V ± 0.3V
32	FSEN1	I, LVCMOS	Failsafe enable pin with a 300 k Ω pullup resistor. This pin enables Type 2 receiver on inputs 0 and 2. FSEN1 = L> Type 1 receiver inputs FSEN1 = H> Type 2 receiver inputs
9	FSEN2	I, LVCMOS	Failsafe enable pin with a 300 k Ω pullup resistor. This pin enables Type 2 receiver on inputs 1 and 3. FSEN2 = L> Type 1 receiver inputs FSEN2 = H> Type 2 receiver inputs
10	MDE	I, LVCMOS	Master enable pin. When MDE is H, the device is powered up. When MDE is L, the device overrides all other control and powers down.

M-LVDS Receiver Types

The EIA/TIA-899 M-LVDS standard specifies two different types of receiver input stages. A type 1 receiver has a conventional threshold that is centered at the midpoint of the input amplitude, $V_{ID}/2$. A type 2 receiver has a built in offset that is 100mV greater then $V_{ID}/2$. The type 2 receiver offset acts as a failsafe circuit where open or short circuits at the input will always result in the output stage being driven to a low logic state.

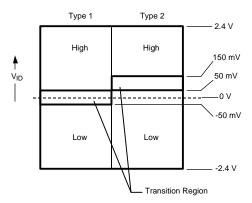


Figure 1. M-LVDS Receiver Input Thresholds



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



Absolute Maximum Ratings (1)(2)

Power Supply Voltage	-0.3V to +4V	
LVCMOS Input Voltage	-0.3V to (V _{DD} + 0.3V)	
LVCMOS Output Voltage		-0.3V to (V _{DD} + 0.3V)
M-LVDS I/O Voltage		−1.9V to +5.5V
M-LVDS Output Short Circuit Current Duration		Continuous
Junction Temperature		+140°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature Range Soldering (4 sec.)		+260°C
Maximum Package Power Dissipation @ +25°C	RTV Package	3.91W
	Derate RTV Package	34 mW/°C above +25°C
Package Thermal Resistance (4-Layer, 2 oz. Cu,	θ_{JA}	+29.4°C/W
JEDEC)	θ_{JC}	+2.8°C/W
ESD Susceptibility	HBM ⁽³⁾	≥8 kV
	MM ⁽⁴⁾	≥250V
	CDM ⁽⁵⁾	≥1250V

[&]quot;Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

- If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
- Human Body Model, applicable std. JESD22-A114C
- Machine Model, applicable std. JESD22-A115-A Field Induced Charge Device Model, applicable std. JESD22-C101-C

Recommended Operating Conditions

	Min	Тур	Max	Units
Supply Voltage, V _{DD}	3.0	3.3	3.6	V
Voltage at Any Bus Terminal (Separate or Common-Mode)	-1.4		+3.8	V
Differential Input Voltage V _{ID}			2.4	V
LVTTL Input Voltage High V _{IH}	2.0		V_{DD}	V
LVTTL Input Voltage Low V _{IL}	0		0.8	V
Operating Free Air Temperature T _A	-40	+25	+85	°C



DC Electrical Characteristics (1)(2)(3)(4)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Min	Тур	Max	Units
M-LVDS D	river	,		1		'	
V _{AB}	Differential output voltage magnitude	$R_L = 50\Omega, C_L = 5 pF$		480		650	mV
ΔV_{AB}	Change in differential output voltage magnitude between logic states	Figure 2 Figure 4		-50	0	+50	mV
V _{OS(SS)}	Steady-state common-mode output voltage	$R_L = 50\Omega, C_L = 5 pF$		0.3	1.6	2.1	V
$ \Delta V_{OS(SS)} $	Change in steady-state common-mode output voltage between logic states	Figure 2 Figure 3		0		+50	mV
V _{A(OC)}	Maximum steady-state open-circuit output voltage	Figure 5		0		2.4	V
V _{B(OC)}	Maximum steady-state open-circuit output voltage			0		2.4	V
V _{P(H)}	Voltage overshoot, low-to-high level output (5)	$R_L = 50\Omega$, $C_L = 5pF$, C_D	o = 0.5 pF			1.2V _{SS}	V
$V_{P(L)}$	Voltage overshoot, high-to-low level output (5)	Figure 7 Figure 8		-0.2V			V
I _{IH}	High-level input current (LVTTL inputs)	V _{IH} = 3.6V		-15		15	μΑ
I _{IL}	Low-level input current (LVTTL inputs)	$V_{IL} = 0.0V$		-15		15	μΑ
V _{CL}	Input Clamp Voltage (LVTTL inputs)	I _{IN} = -18 mA		-1.5			V
Ios	Differential short-circuit output current (6)	Figure 6		-43		43	mA
M-LVDS R	eceiver				•		
V _{IT+}	Positive-going differential input voltage threshold	See Truth Tables	Type 1		16	50	mV
		Type 2			100	150	mV
V _{IT} -	Negative-going differential input voltage threshold	See Truth Tables	Type 1	-50	20		mV
		Type 2		50	94		mV
V _{OH}	High-level output voltage (LVTTL output)	I _{OH} = -8mA		2.4	2.7		V
V _{OL}	Low-level output voltage (LVTTL output)	I _{OL} = 8mA			0.28	0.4	V
I _{OZ}	TRI-STATE output current	V _O = 0V or 3.6V		-10		10	μΑ
I _{OSR}	Short-circuit receiver output current (LVTTL output)	V _O = 0V			-50	-90	mA

⁽¹⁾ The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.

⁽²⁾ Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground

except V_{OD} and ΔV_{OD}.
 (3) Typical values represent most likely parametric norms for V_{DD} = +3.3V and T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not specified.

⁽⁴⁾ C_L includes fixture capacitance and C_D includes probe capacitance.

⁽⁵⁾ Specification is ensured by characterization and is not tested in production.

⁽⁶⁾ Output short circuit current (Ios) is specified as magnitude only, minus sign indicates direction only.



DC Electrical Characteristics⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾ (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Units
M-LVDS B	us (Input and Output) Pins					
I _A	Transceiver input/output current	V _A = 3.8V, V _B = 1.2V			32	μΑ
		V _A = 0V or 2.4V, V _B = 1.2V	-20		+20	μA
		V _A = −1.4V, V _B = 1.2V	-32			μΑ
I _B	Transceiver input/output current	V _B = 3.8V, V _A = 1.2V			32	μΑ
		V _B = 0V or 2.4V, V _A = 1.2V	-20		+20	μΑ
		V _B = −1.4V, V _A = 1.2V	-32			μΑ
I _{AB}	Transceiver input/output differential current (I _A - I _B)	$V_A = V_B$, $-1.4V \le V \le 3.8V$	-4		+4	μΑ
I _{A(OFF)}	Transceiver input/output power-off current	$V_A = 3.8V, V_B = 1.2V,$ DE = 0V $0V \le V_{DD} \le 1.5V$			32	μA
		$V_A = 0V \text{ or } 2.4V, V_B = 1.2V, \\ DE = 0V \\ 0V \le V_{DD} \le 1.5V$	-20		+20	μА
		$V_A = -1.4V, V_B = 1.2V,$ DE = 0V 0V \le V_DD \le 1.5V	-32			μΑ
I _{B(OFF)}	Transceiver input/output power-off current	$V_B = 3.8V, V_A = 1.2V, \\ DE = 0V \\ 0V \le V_{DD} \le 1.5V$			32	μΑ
		$V_B = 0V \text{ or } 2.4V, V_A = 1.2V, \\ DE = 0V \\ 0V \le V_{DD} \le 1.5V$	-20		+20	μА
		$V_B = -1.4V, V_A = 1.2V,$ DE = 0V 0V \le V_{DD} \le 1.5V	-32			μА
I _{AB(OFF)}	Transceiver input/output power-off differential current $(I_{A(OFF)} - I_{B(OFF)})$	$\begin{aligned} & V_A = V_B, \ \neg 1.4V \leq V \leq 3.8V, \\ & DE = 0V \\ & 0V \leq V_{DD} \leq 1.5V \end{aligned}$	-4		+4	μА
C _A	Transceiver input/output capacitance	V _{DD} = OPEN		7.8		pF
Св	Transceiver input/output capacitance			7.8		pF
C _{AB}	Transceiver input/output differential capacitance			3		pF
C _{A/B}	Transceiver input/output capacitance balance (C _A /C _B)			1		
SUPPLY C	URRENT (V _{CC})		•			
I _{CCD}	Driver Supply Current	$R_L = 50\Omega$, $DE = H$, $\overline{RE} = H$		67	75	mA
I _{CCZ}	TRI-STATE Supply Current	DE = L, RE = H		22	26	mA
I _{CCR}	Receiver Supply Current	$DE = L, \overline{RE} = L$		32	38	mA
I _{CCPD}	Power Down Supply Current	MDE = L		3	5	mA



Switching Characteristics (1)(2)(3)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Units
DRIVER AC S	SPECIFICATIONS		"	•		
t _{PLH}	Differential Propagation Delay Low to High	$R_L = 50\Omega, C_L = 5 pF,$	1.5	3.3	5.5	ns
t _{PHL}	Differential Propagation Delay High to Low	$C_D = 0.5 \text{ pF}$	1.5	3.3	5.5	ns
t _{SKD1}	Pulse Skew ⁽⁴⁾⁽⁵⁾	Figure 7 Figure 8		30	125	ps
t _{SKD2}	Channel-to-Channel Skew ⁽⁴⁾⁽⁶⁾			100	200	ps
t _{SKD3}	Part-to-Part Skew ⁽⁴⁾⁽⁷⁾			0.8	1.6	ns
t _{SKD4}	Part-to-Part Skew ⁽⁴⁾⁽⁸⁾				4	ns
t _{TLH}	Rise Time ⁽⁴⁾		1.2	2.0	3.0	ns
t _{THL}	Fall Time ⁽⁴⁾		1.2	2.0	3.0	ns
t _{PZH}	Enable Time (Z to Active High)	$R_L = 50\Omega, C_L = 5 pF,$		7.5	11.5	ns
t _{PZL}	Enable Time (Z to Active Low)	$C_D = 0.5 \text{ pF}$		8.0	11.5	ns
t _{PLZ}	Disable Time (Active Low to Z)	Figure 9 Figure 10		7.0	11.5	ns
t _{PHZ}	Disable Time (Active High to Z)			7.0	11.5	ns
RECEIVER A	C SPECIFICATIONS					
t _{PLH}	Propagation Delay Low to High	C _L = 15 pF	1.5	3.0	4.5	ns
t _{PHL}	Propagation Delay High to Low	Figure 11 Figure 12 Figure 13	1.5	3.1	4.5	ns
t _{SKD1A}	Pulse Skew (Receiver Type 1) ⁽⁴⁾⁽⁵⁾			55	325	ps
t _{SKD1B}	Pulse Skew (Receiver Type 2) ⁽⁴⁾⁽⁵⁾			475	800	ps
t _{SKD2}	Channel-to-Channel Skew ⁽⁴⁾⁽⁶⁾			60	300	ps
t _{SKD3}	Part-to-Part Skew ⁽⁴⁾⁽⁷⁾			0.6	1.2	ns
t _{SKD4}	Part-to-Part Skew ⁽⁸⁾				3	ns
t _{TLH}	Rise Time ⁽⁴⁾		0.3	1.1	1.6	ns
t _{THL}	Fall Time ⁽⁴⁾		0.3	0.65	1.6	ns
t _{PZH}	Enable Time (Z to Active High)	$R_L = 500\Omega, C_L = 15 pF$		3	5.5	ns
t _{PZL}	Enable Time (Z to Active Low)	Figure 14 Figure 15		3	5.5	ns
t _{PLZ}	Disable Time (Active Low to Z)			3.5	5.5	ns
t _{PHZ}	Disable Time (Active High to Z)			3.5	5.5	ns
GENERIC AC	SPECIFICATIONS		•			
t _{WKUP}	Wake Up Time ⁽⁴⁾ (Master Device Enable (MDE) time)				500	ms
f _{MAX}	Maximum Operating Frequency ⁽⁴⁾		125			MHz

- (1) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
- (2) Typical values represent most likely parametric norms for $V_{DD} = +3.3V$ and $T_A = +25^{\circ}C$, and at the Recommended Operation Conditions at the time of product characterization and are not specified.
- (3) C_L includes fixture capacitance and C_D includes probe capacitance.
- (4) Specification is ensured by characterization and is not tested in production.
- (5) t_{SKD1}, |t_{PLHD} t_{PHLD}|, Pulse Skew, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
- (6) t_{SKD2}, Channel-to-Channel Skew, is the difference in propagation delay (t_{PLHD} or t_{PHLD}) among all output channels.
- (7) t_{SKD3}, Part-to-Part Skew, is defined as the difference between the minimum and maximum differential propagation delays. This specification applies to devices at the same V_{DD} and within 5°C of each other within the operating temperature range.
- (8) t_{SKD4}, Part-to-Part Skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as |Max Min| differential propagation delay.



Test Circuits and Waveforms

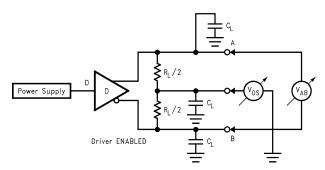


Figure 2. Differential Driver Test Circuit

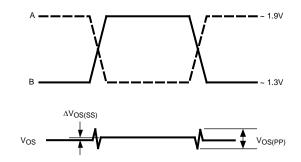


Figure 3. Differential Driver Waveforms

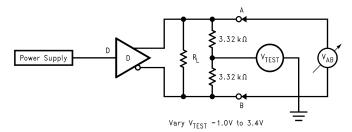


Figure 4. Differential Driver Full Load Test Circuit

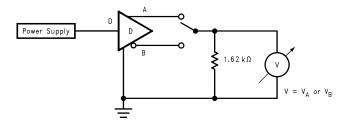


Figure 5. Differential Driver DC Open Test Circuit



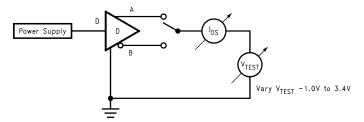


Figure 6. Differential Driver Short-Circuit Test Circuit

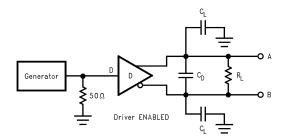


Figure 7. Driver Propagation Delay and Transition Time Test Circuit

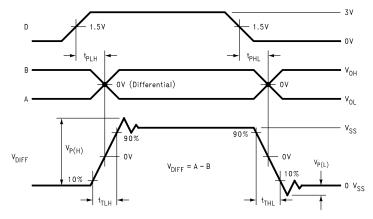


Figure 8. Driver Propagation Delays and Transition Time Waveforms

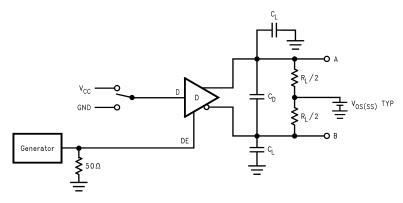


Figure 9. Driver TRI-STATE Delay Test Circuit

Product Folder Links, DC01A

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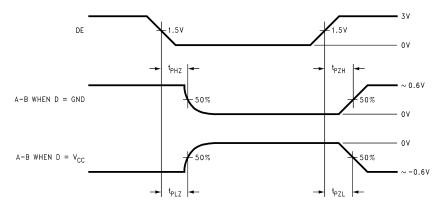


Figure 10. Driver TRI-STATE Delay Waveforms

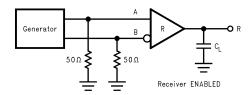


Figure 11. Receiver Propagation Delay and Transition Time Test Circuit

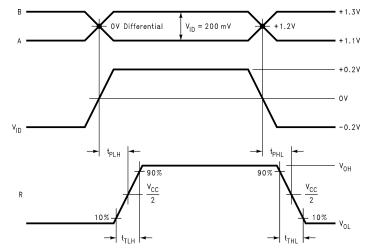


Figure 12. Type 1 Receiver Propagation Delay and Transition Time Waveforms



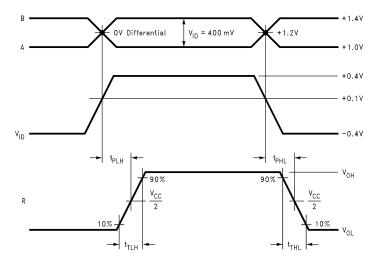


Figure 13. Type 2 Receiver Propagation Delay and Transition Time Waveforms

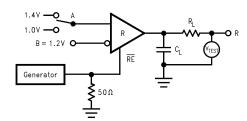


Figure 14. Receiver TRI-STATE Delay Test Circuit

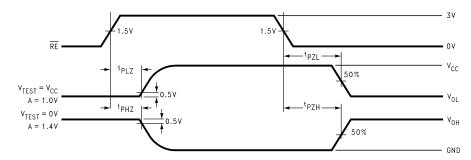


Figure 15. Receiver TRI-STATE Delay Waveforms

TRUTH TABLES

DS91M040 Transmitting⁽¹⁾

Inputs			Out	outs
RE	DE	DI	В	Α
Х	Н	Н	L	Н
X	Н	L	Н	L
X	L	X	Z	Z

⁽¹⁾ X — Don't care condition

Z — High impedance state



DS91M040 as Type 1 Receiving(1)

Inputs			Output	
FSEN	RE	DE	A - B	RO
L	L	X	≥ +0.05V	Н
L	L	Х	≤ -0.05V	L
L	L	Х	-0.05V ≤ A-B ≤ +0.05V	Undefined
L	Н	Х	X	Z

 $\begin{array}{ccc} \text{(1)} & X \longrightarrow \text{Don't care condition} \\ Z \longrightarrow \text{High impedance state} \end{array}$

DS91M040 as Type 2 Receiving(1)

			<u> </u>	
Inputs			Output	
FSEN	RE	DE	A - B	RO
Н	L	X	≥ +0.15V	Н
Н	L	X	≤ +0.05V	L
Н	L	Х	+0.05V ≤ A-B ≤ +0.15V	Undefined
Н	Н	Х	X	Z

(1) X — Don't care condition Z — High impedance state

DS91M040 Type 1 Receiver Input Threshold Test Voltages⁽¹⁾

Applied Voltages		Applied Voltages Resulting Differential Input Voltage		Receiver Output
V _{IA}	V _{IB}	V _{ID}	V _{ICM}	R
2.400V	0.000V	2.400V	1.200V	Н
0.000V	2.400V	-2.400V	1.200V	L
3.800V	3.750V	0.050V	3.775V	Н
3.750V	3.800V	-0.050V	3.775V	L
-1.350V	-1.400V	0.050V	-1.375V	Н
-1.400V	-1.350V	-0.050V	-1.375V	L

(1) H — High Level

L — Low Level

Output state assumes that the receiver is enabled ($\overline{RE} = L$)

DS91M040 Type 2 Receiver Input Threshold Test Voltages⁽¹⁾

Applied Voltages		Resulting Differential Input Voltage	Resulting Common-Mode Input Voltage	Receiver Output
V _{IA}	V _{IB}	V _{ID}	V _{IC}	R
2.400V	0.000V	2.400V	1.200V	Н
0.000V	2.400V	-2.400V	1.200V	L
3.800V	3.650V	0.150V	3.725V	Н
3.800V	3.750V	0.050V	3.775V	L
-1.250V	-1.400V	0.150V	-1.325V	Н
-1.350V	-1.400V	0.050V	-1.375V	L

(1) H — High Level

L — Low Level

Output state assumes that the receiver is enabled ($\overline{RE} = L$)



Typical Performance Characteristics

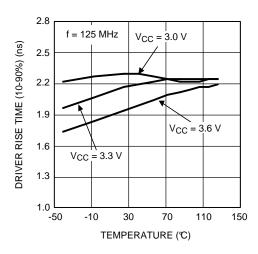


Figure 16. Driver Rise Time as a Function of Temperature

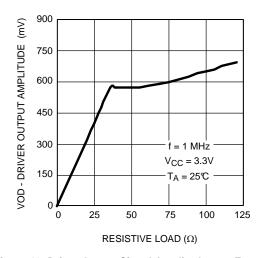


Figure 18. Driver Output Signal Amplitude as a Function of Resistive Load

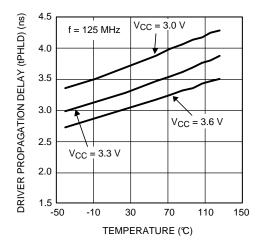


Figure 20. Driver Propagation Delay (tPHLD) as a Function of Temperature

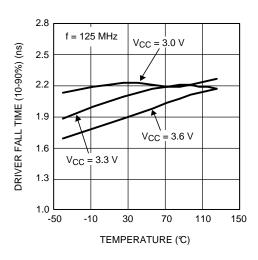


Figure 17. Driver Fall Time as a Function of Temperature

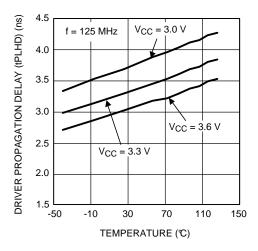


Figure 19. Driver Propagation Delay (tPLHD) as a Function of Temperature

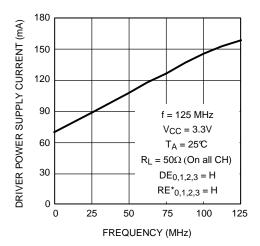
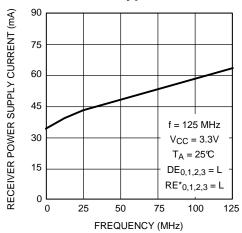


Figure 21. Driver Power Supply Current as a Function of Frequency



Typical Performance Characteristics (continued)



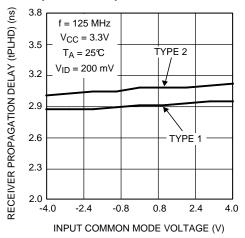


Figure 22. Receiver Power Supply Current as a Function of Frequency

Figure 23. Receiver Propagation Delay (tPLHD) as a Function of Input Common Mode Voltage

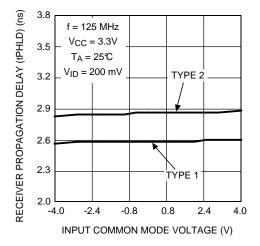


Figure 24. Receiver Propagation Delay (tPHLD) as a Function of Input Common Mode Voltage





REVISION HISTORY

CI	Changes from Revision L (April 2013) to Revision M					
•	Changed layout of National Data Sheet to TI format		14			

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/ Ball material	MSL rating/ Peak reflow	Op temp (°C)	Part marking (6)
	. ,				. , ,	(4)	(5)		, ,
DS91M040TSQ/NOPB	Active	Production	WQFN (RTV) 32	1000 SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	M040TS
DS91M040TSQ/NOPB.A	Active	Production	WQFN (RTV) 32	1000 SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	M040TS
DS91M040TSQE/NOPB	Active	Production	WQFN (RTV) 32	250 SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	M040TS
DS91M040TSQE/NOPB.A	Active	Production	WQFN (RTV) 32	250 SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	M040TS
DS91M040TSQX/NOPB	Active	Production	WQFN (RTV) 32	4500 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	M040TS
DS91M040TSQX/NOPB.A	Active	Production	WQFN (RTV) 32	4500 LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 85	M040TS

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.



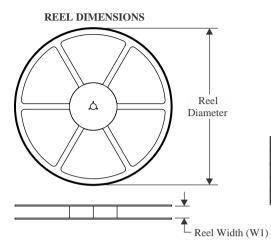
PACKAGE OPTION ADDENDUM

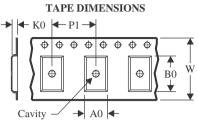
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PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS91M040TSQ/NOPB	WQFN	RTV	32	1000	177.8	12.4	5.3	5.3	1.3	8.0	12.0	Q1
DS91M040TSQE/NOPB	WQFN	RTV	32	250	177.8	12.4	5.3	5.3	1.3	8.0	12.0	Q1
DS91M040TSQX/NOPB	WQFN	RTV	32	4500	330.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1

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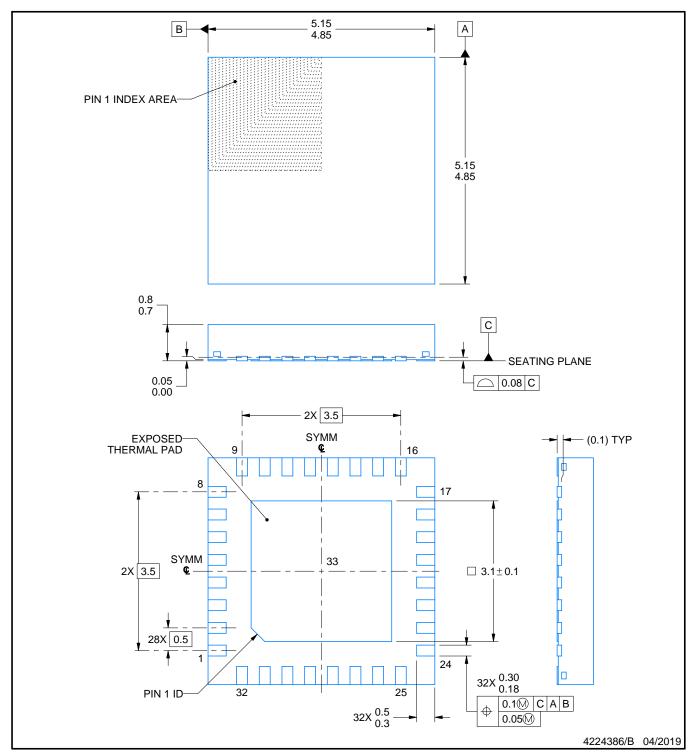


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS91M040TSQ/NOPB	WQFN	RTV	32	1000	208.0	191.0	35.0
DS91M040TSQE/NOPB	WQFN	RTV	32	250	208.0	191.0	35.0
DS91M040TSQX/NOPB	WQFN	RTV	32	4500	356.0	356.0	36.0



PLASTIC QUAD FLATPACK - NO LEAD

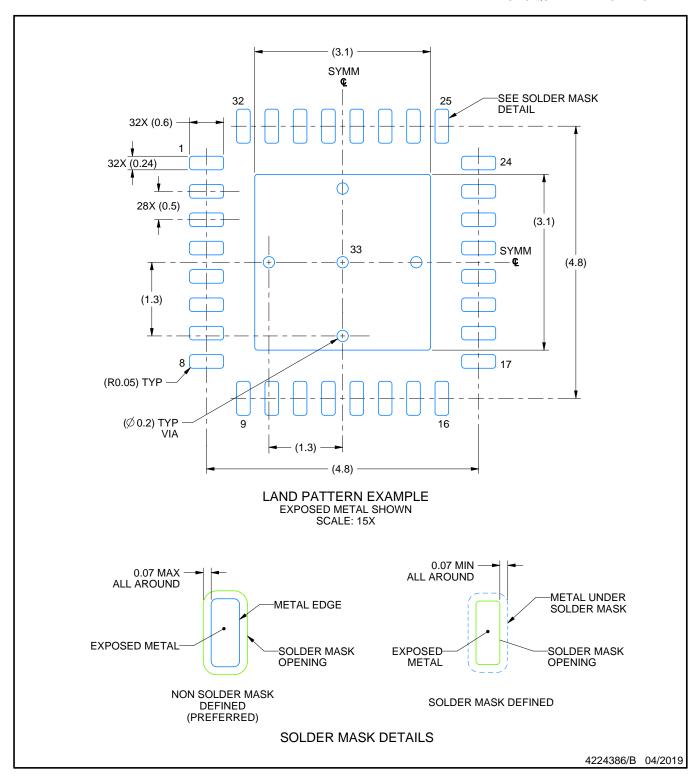


NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC QUAD FLATPACK - NO LEAD

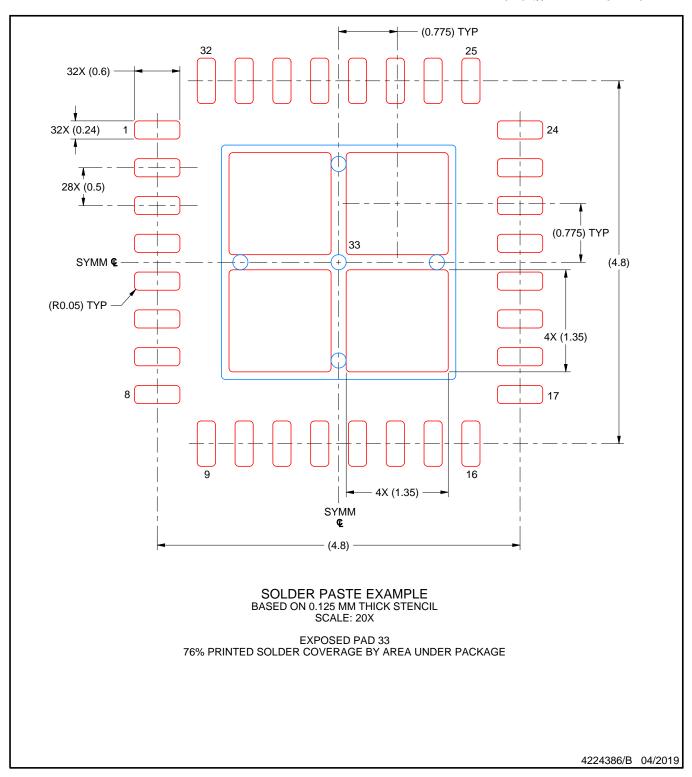


NOTES: (continued)

- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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