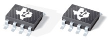


SoundPlus™ 低功率，低噪音和失真，双极输入音频运算放大器

查询样品: OPA1662, OPA1664

特性

- 低噪声： 1kHz 下为 3.3nV/√Hz
- 低失真：1kHz下为0.00006%
- 低静态电流：
  每通道1.5mA
- 转换速率： 17V/μs
- 宽增益带宽：22MHz(G = +1)
- 单位增益稳定
- 轨至轨输出
- 宽电源范围：
  ±1.5 V至 ±18 V，或者 +3 V至+36 V
- 双通道及四通道产品已供货
- 小封装尺寸：
  双通道：小外形尺寸(SO)-8和微型小外形尺寸(MSOP)-8
  四通道：小外形尺寸(SO)-14和薄型小尺寸(TSSOP)-14

应用范围

- USB和固件音频系统
- 模拟和数字混音器
- 便携式录音系统
- 音效处理器
- 高端A/V接收器
- 高端DVD和 蓝光(Blu-Ray)™ 播放器
- 高端车载音频

说明

OPA1662（双通道） 与 OPA1664（四通道）双极输入运算放大器系列产品能够以超低失真（1kHz 时为 0.00006%）实现 3.3nV/√Hz 的极低噪声密度。 OPA1662 与 OPA1664 系列运算放大器可在 2 kΩ 负载下支持 600 mV 以内的轨至轨输出摆幅，其可提高预留空间并达到增加动态范围。 此外，这些器件还具有 ±30mA 的高输出驱动能力。

这些器件可在 ±1.5 V 至 ±18 V，或者+3 V 至+36 V 很宽的电源电压范围内运行，每通道电源电流仅为 1.5 mA。 OPA1662 与 OPA1664运算放大器单位增益稳定并可在宽范围的负载条件下提供出色的动态性能。

它们还采用完全独立的电路系统，可将串扰降到最低，即便在过驱动或过载时也不受通道间相互作用而带来的干扰。

OPA1662 与 OPA1664 额定温度范围为 –40°C 至 +85°C。

English Data Sheet: SBOS489

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
OPA1662	SO-8	D	OP1662
	MSOP-8	DGK	OUQI
OPA1664	SO-14	D	OP1664
	TSSOP-14	PW	OP1664

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

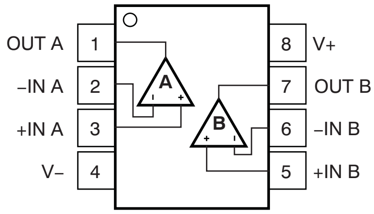
		OPA1662, OPA1664	UNIT
Supply voltage, V_S = (V+) – (V–)		40	V
Input voltage		(V–) – 0.5 to (V+) + 0.5	V
Input current (all pins except power-supply pins)		±10	mA
Output short-circuit(2)		Continuous	
Operating temperature range		–55 to +125	°C
Storage temperature range		–65 to +150	°C
Junction temperature		200	°C
ESD ratings	Human body model (HBM)	2	kV
	Charged device model (CDM)	1	kV
	Machine model (MM)	200	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

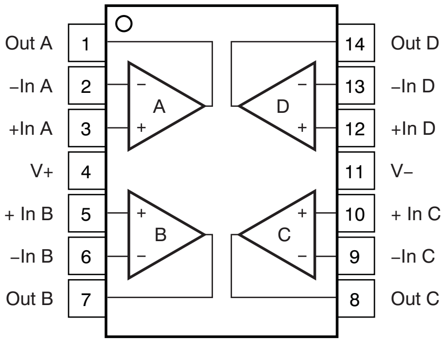
(2) Short-circuit to $V_S/2$ (ground in symmetrical dual supply setups), one amplifier per package.

PIN CONFIGURATIONS

OPA1662: D AND DGK PACKAGES
SO-8 AND MSOP-8
(TOP VIEW)



OPA1664: D AND PW PACKAGES
SO-14 AND TSSOP-14
(TOP VIEW)



ELECTRICAL CHARACTERISTICS: V_S = ±15 V

At T_A = +25°C and R_L = 2 kΩ, unless otherwise noted. V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

PARAMETER		CONDITIONS		OPA1662, OPA1664			UNIT
				MIN	TYP	MAX	
AUDIO PERFORMANCE							
THD+N	Total harmonic distortion + noise	G = +1, f = 1 kHz, V_O = 3 V_{RMS}			0.00006		%
					–124		dB
IMD	Intermodulation distortion	G = +1, V_O = 3 V_{RMS}	SMPTE/DIN two-tone, 4:1 (60 Hz and 7 kHz)		0.00004		%
					–128		dB
			DIM 30 (3-kHz square wave and 15-kHz sine wave)		0.00004		%
					–128		dB
			CCIF twin-tone (19 kHz and 20 kHz)		0.00004		%
					–128		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	G = +1			22		MHz
SR	Slew rate	G = –1			17		V/μs
	Full power bandwidth(1)	V_O = 1 V_P			2.7		MHz
	Overload recovery time	G = –10			1		μs
	Channel separation (dual and quad)	f = 1 kHz			–120		dB
NOISE							
e_n	Input voltage noise	f = 20 Hz to 20 kHz			2.8		μV_{PP}
	Input voltage noise density	f = 1 kHz			3.3		nV/√Hz
		f = 100 Hz			5		nV/√Hz
I_n	Input current noise density	f = 1 kHz			1		pA/√Hz
		f = 100 Hz			2		pA/√Hz
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = ±1.5 V to ±18 V			±0.5	±1.5	mV
		V_S = ±1.5 V to ±18 V, T_A = –40°C to +85°(2)			2	8	μV/°C
PSRR	Power-supply rejection ratio	V_S = ±1.5 V to ±18 V			1	3	μV/V
INPUT BIAS CURRENT							
I_B	Input bias current	V_{CM} = 0 V			600	1200	nA
I_{OS}	Input offset current	V_{CM} = 0 V			±25	±100	nA
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			(V–) +0.5		(V+) – 1	V
CMRR	Common-mode rejection ratio			106	114		dB
INPUT IMPEDANCE							
	Differential				170 || 2		kΩ || pF
	Common-mode				600 || 2.5		MΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.6 V ≤ V_O ≤ (V+) – 0.6 V, R_L = 2 kΩ		106	114		dB
OUTPUT							
V_{OUT}	Output voltage	R_L = 2 kΩ		(V–) + 0.6		(V+) – 0.6	V
I_{OUT}	Output current				See Typical Characteristics		mA
Z_O	Open-loop output impedance				See Typical Characteristics		Ω
I_{SC}	Short-circuit current(3)				±50		mA
C_{LOAD}	Capacitive load drive				200		pF

(1) Full-power bandwidth = SR/(2π × V_P), where SR = slew rate.
(2) Specified by design and characterization.
(3) One channel at a time.

ELECTRICAL CHARACTERISTICS: V_S = ±15 V (continued)

At T_A = +25°C and R_L = 2 kΩ, unless otherwise noted. V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

PARAMETER		CONDITIONS	OPA1662, OPA1664			UNIT
			MIN	TYP	MAX	
POWER SUPPLY						
V_S	Specified voltage range		±1.5		±18	V
I_Q	Quiescent current (per channel)	I_{OUT} = 0 A		1.5	1.8	mA
		I_{OUT} = 0 A, T_A = –40°C to +85°(4)			2	mA
TEMPERATURE						
	Specified range		–40		+85	°C
	Operating range		–55		+125	°C

(4) Specified by design and characterization.

ELECTRICAL CHARACTERISTICS: V_S = +5 V

At T_A = +25°C and R_L = 2 kΩ, unless otherwise noted. V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

PARAMETER		CONDITIONS		OPA1662, OPA1664			UNIT
				MIN	TYP	MAX	
AUDIO PERFORMANCE							
THD+N	Total harmonic distortion + noise	G = +1, f = 1 kHz, V_O = 3 V_{RMS}			0.0001		%
					–120		dB
IMD	Intermodulation distortion	G = +1, V_O = 3 V_{RMS}	SMPTE/DIN two-tone, 4:1 (60 Hz and 7 kHz)		0.00004		%
					–128		dB
			DIM 30 (3-kHz square wave and 15-kHz sine wave)		0.00004		%
					–128		dB
			CCIF twin-tone (19 kHz and 20 kHz)		0.00004		%
					–128		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	G = +1			20		MHz
SR	Slew rate	G = –1			13		V/μs
	Full power bandwidth(1)	V_O = 1 V_P			2		MHz
	Overload recovery time	G = –10			1		μs
	Channel separation (dual and quad)	f = 1 kHz			–120		dB
NOISE							
e_n	Input voltage noise	f = 20 Hz to 20 kHz			3.3		μV_{PP}
	Input voltage noise density	f = 1 kHz			3.3		nV/√Hz
		f = 100 Hz			5		nV/√Hz
I_n	Input current noise density	f = 1 kHz			1		pA/√Hz
		f = 100 Hz			2		pA/√Hz
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = ±1.5 V to ±18 V			±0.5	±1.5	mV
		V_S = ±1.5 V to ±18 V, T_A = –40°C to +85°(2)			2	8	μV/°C
PSRR	Power-supply rejection ratio	V_S = ±1.5 V to ±18 V			1	3	μV/V
INPUT BIAS CURRENT							
I_B	Input bias current	V_{CM} = 0 V			600	1200	nA
I_{OS}	Input offset current	V_{CM} = 0 V			±25	±100	nA
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			(V–) +0.5		(V+) – 1	V
CMRR	Common-mode rejection ratio			86	100		dB
INPUT IMPEDANCE							
	Differential				170 || 2		kΩ || pF
	Common-mode				600 || 2.5		MΩ || pF

(1) Full-power bandwidth = SR/(2π × V_P), where SR = slew rate.
(2) Specified by design and characterization.

ELECTRICAL CHARACTERISTICS: V_S = +5 V (continued)

At T_A = +25°C and R_L = 2 kΩ, unless otherwise noted. V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

PARAMETER		CONDITIONS	OPA1662, OPA1664			UNIT
			MIN	TYP	MAX	
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 0.6 V ≤ V_O ≤ (V+) – 0.6 V, R_L = 2 kΩ	90	100		dB
OUTPUT						
V_{OUT}	Output voltage	R_L = 2 kΩ	(V–) + 0.6		(V+) – 0.6	V
I_{OUT}	Output current		See Typical Characteristics			mA
Z_O	Open-loop output impedance		See Typical Characteristics			Ω
I_{SC}	Short-circuit current (3)			±40		mA
C_{LOAD}	Capacitive load drive			200		pF
POWER SUPPLY						
V_S	Specified voltage range		±1.5		±18	V
I_Q	Quiescent current (per channel)	I_{OUT} = 0 A		1.4	1.7	mA
		I_{OUT} = 0 A, T_A = –40°C to +85° (2)			2	mA
TEMPERATURE						
	Specified range		–40		+85	°C
	Operating range		–55		+125	°C

(3) One channel at a time.

THERMAL INFORMATION: OPA1662

THERMAL METRIC (1)		OPA1662		UNITS
		D (SO)	DGK (MSOP)	
		8 PINS	8 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	156.3	225.4	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	85.5	78.8	
θ_{JB}	Junction-to-board thermal resistance	64.9	110.5	
ψ_{JT}	Junction-to-top characterization parameter	33.8	14.6	
ψ_{JB}	Junction-to-board characterization parameter	64.3	108.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	N/A	

(1) 有关传统和新的热度量的更多信息，请参阅 *IC* 封装热度量 应用报告 SPRA953。

THERMAL INFORMATION:OPA1664

THERMAL METRIC (1)		OPA1664		UNITS
		D (SO)	PW (TSSOP)	
		14 PINS	14 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	78.6	125.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	37.0	45.2	
θ_{JB}	Junction-to-board thermal resistance	24.9	57.5	
ψ_{JT}	Junction-to-top characterization parameter	9.7	5.5	
ψ_{JB}	Junction-to-board characterization parameter	24.6	56.7	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	N/A	

(1) 有关传统和新的热度量的更多信息，请参阅 *IC* 封装热度量 应用报告 SPRA953。

TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

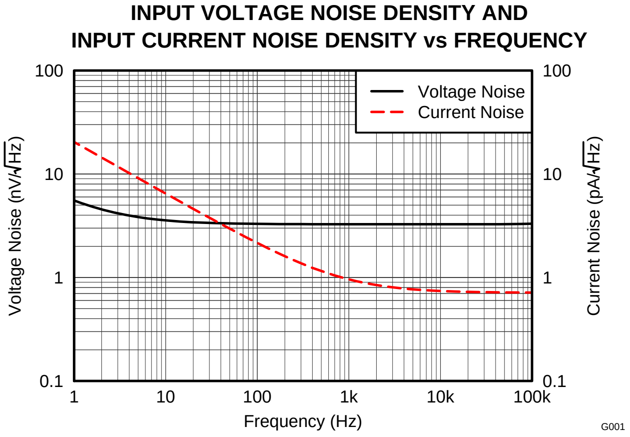


Figure 1.

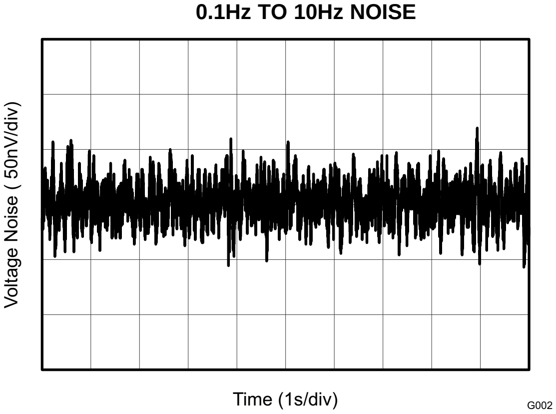


Figure 2.

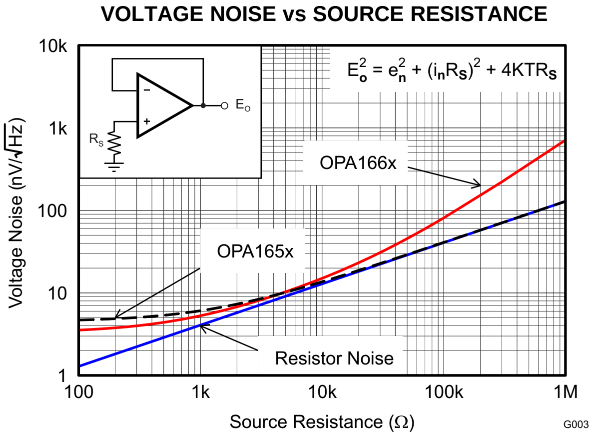


Figure 3.

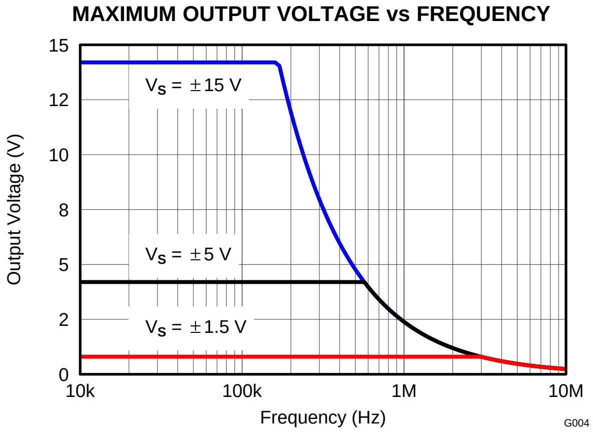


Figure 4.

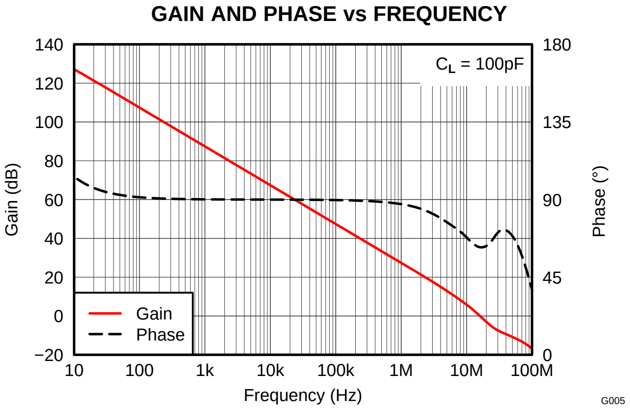


Figure 5.

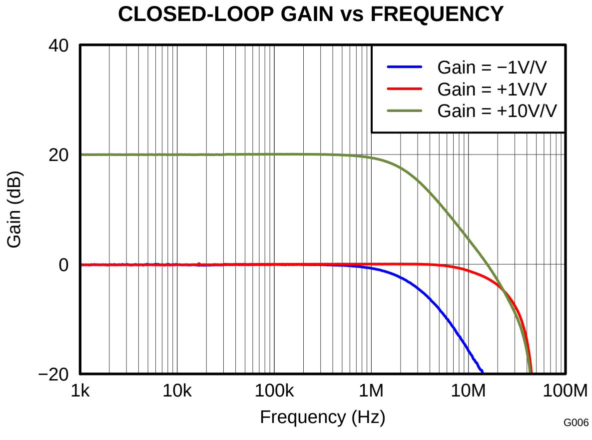


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

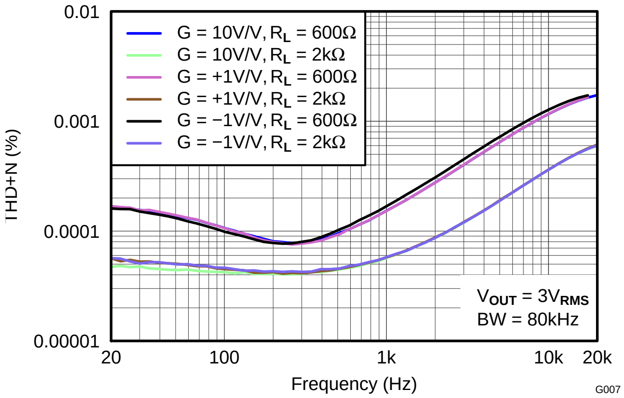

THD+N RATIO vs FREQUENCY

Figure 7.

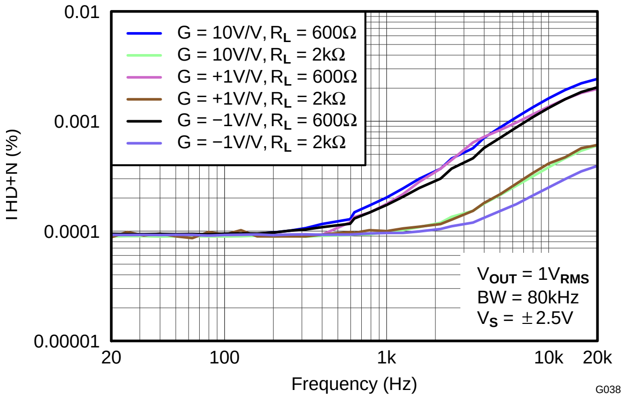

THD+N RATIO vs FREQUENCY

Figure 8.

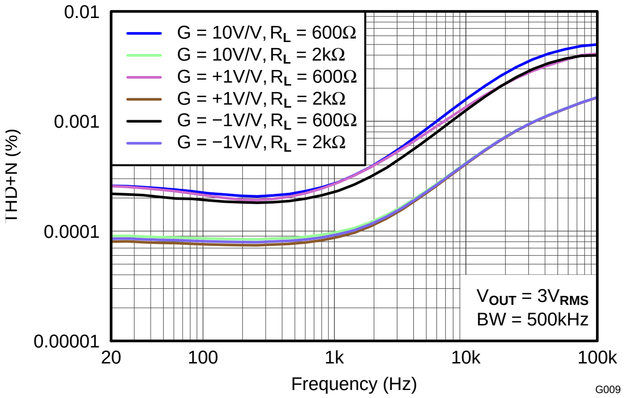

THD+N RATIO vs FREQUENCY

Figure 9.

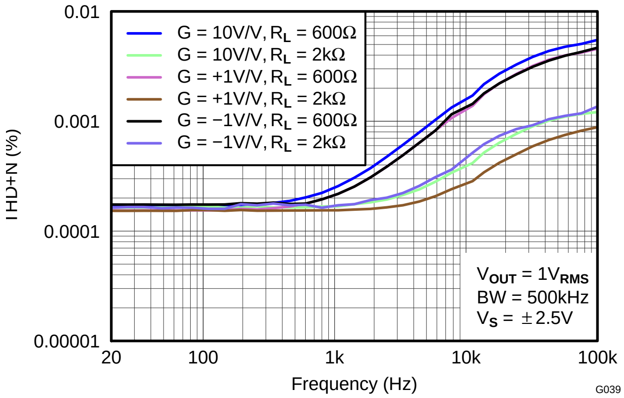

THD+N RATIO vs FREQUENCY

Figure 10.

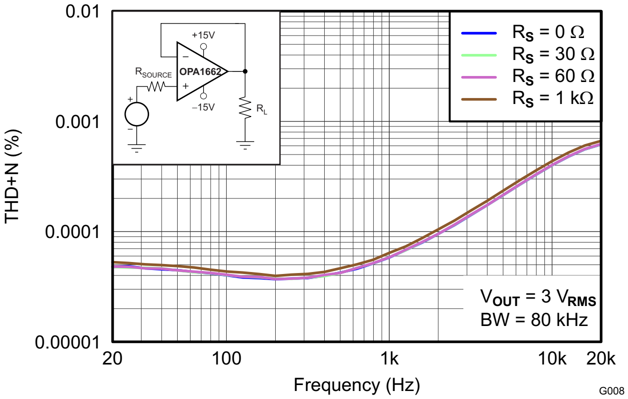

THD+N RATIO vs FREQUENCY

Figure 11.

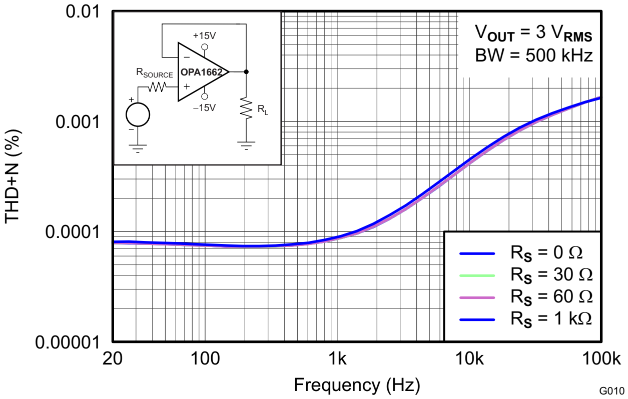

THD+N RATIO vs FREQUENCY

Figure 12.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

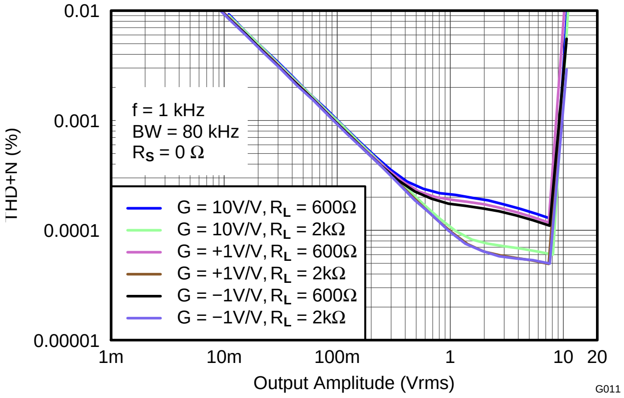

THD+N RATIO vs OUTPUT AMPLITUDE

Figure 13.

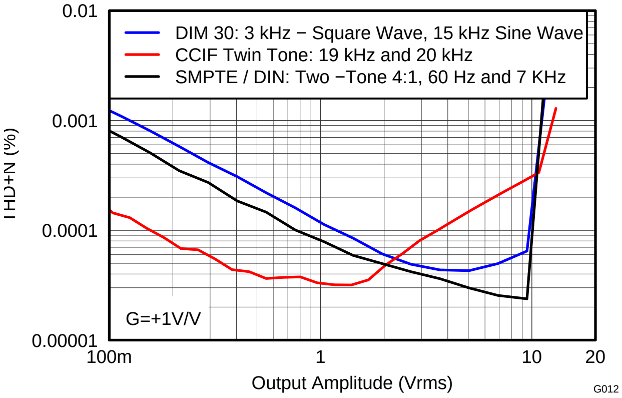

INTERMODULATION DISTORTION vs OUTPUT AMPLITUDE

Figure 14.

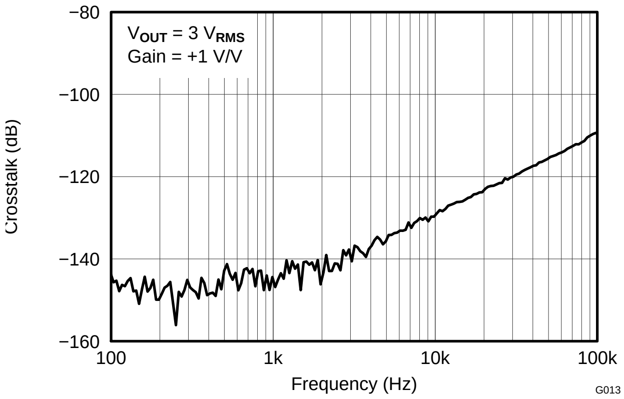

CHANNEL SEPARATION vs FREQUENCY

Figure 15.

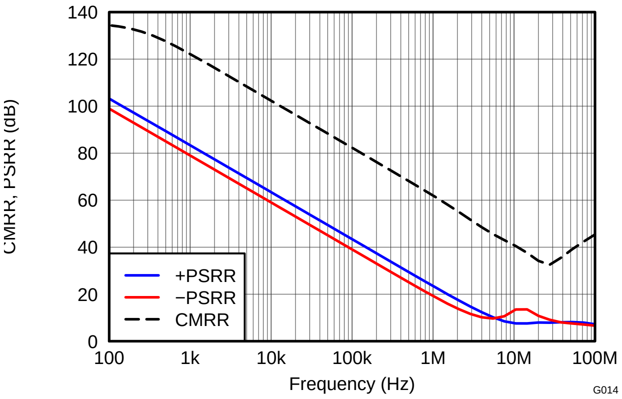

CMRR AND PSRR vs FREQUENCY (Referred to Input)

Figure 16.

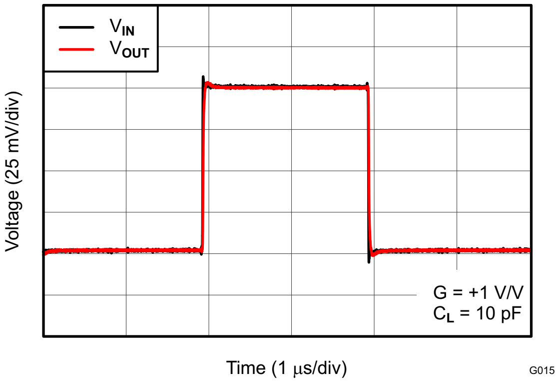

SMALL-SIGNAL STEP RESPONSE

Figure 17.

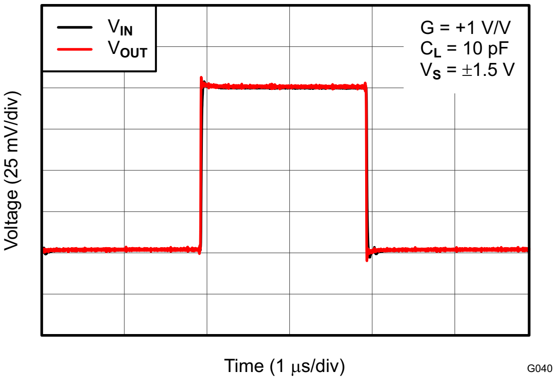

SMALL-SIGNAL STEP RESPONSE

Figure 18.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

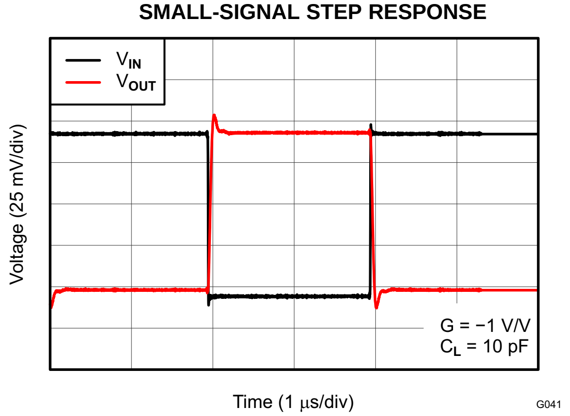


Figure 19.

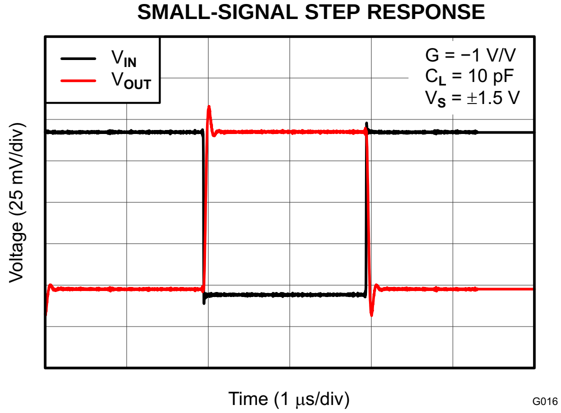


Figure 20.

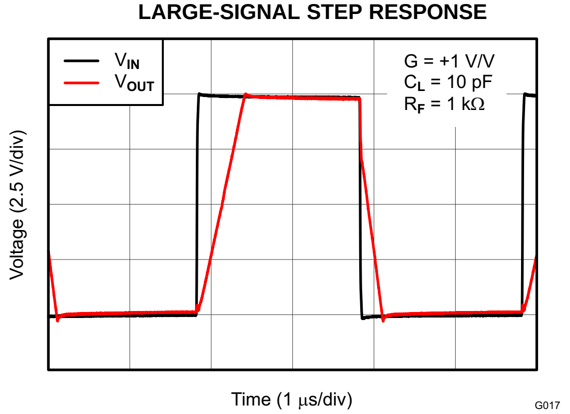


Figure 21.

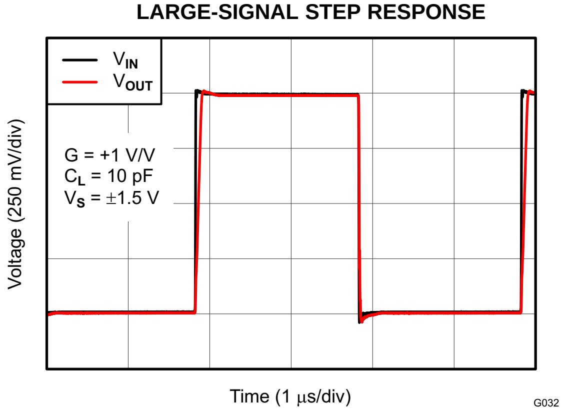


Figure 22.

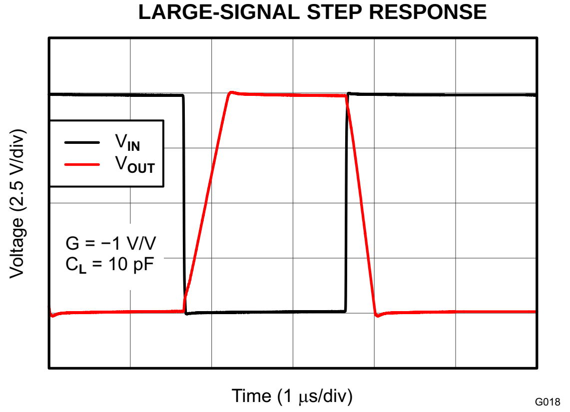


Figure 23.

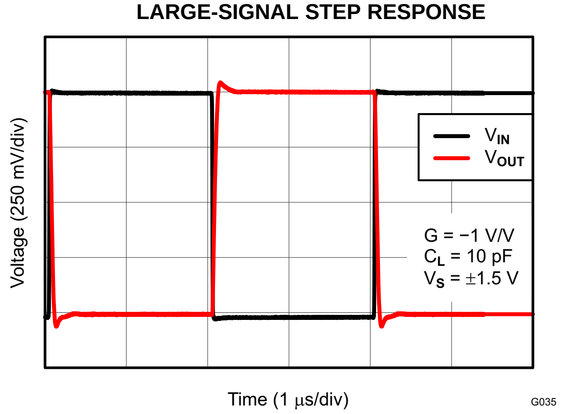


Figure 24.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD

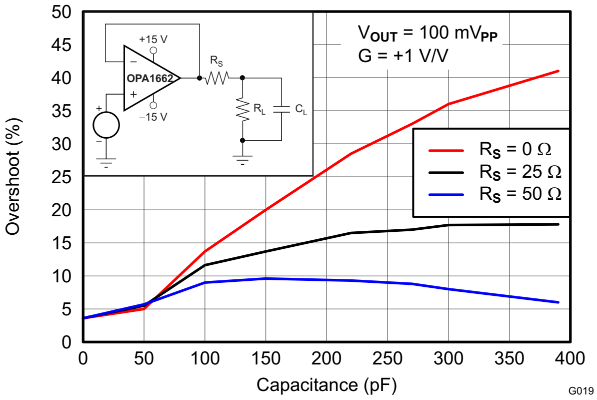


Figure 25.

SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD

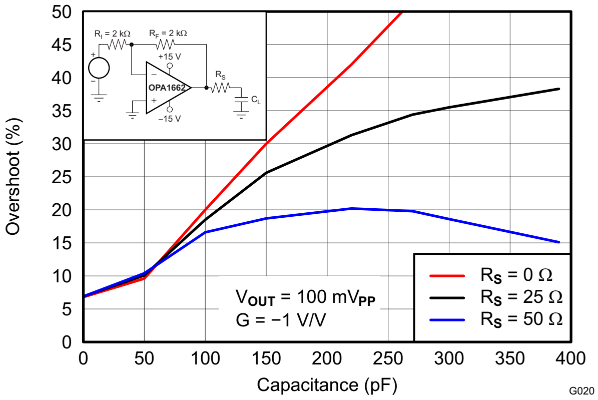


Figure 26.

SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD

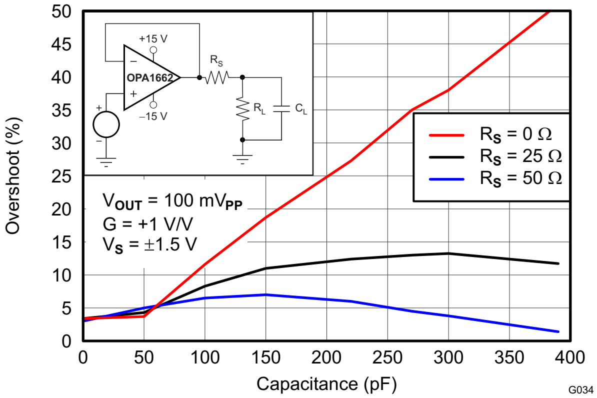


Figure 27.

SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD

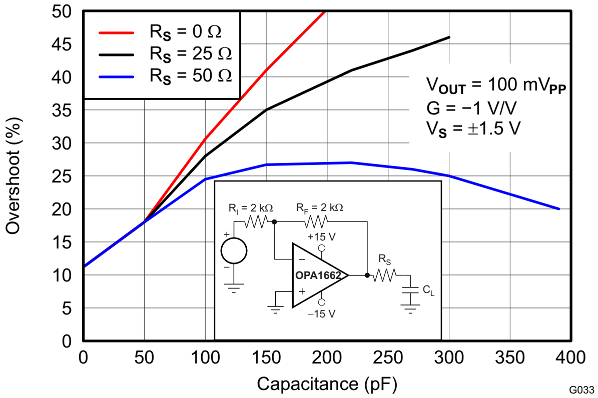


Figure 28.

SMALL-SIGNAL OVERSHOOT vs FEEDBACK CAPACITOR

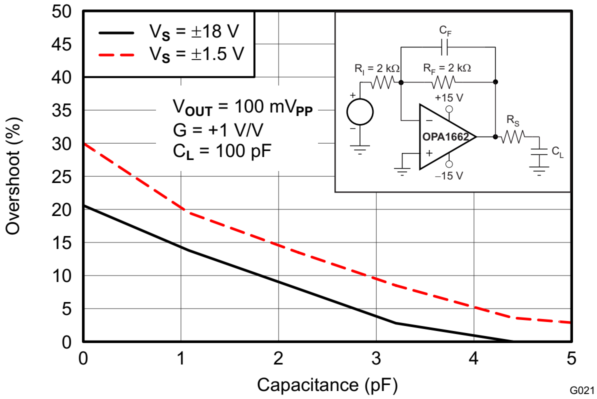


Figure 29.

PERCENT OVERSHOOT vs CAPACITIVE LOAD

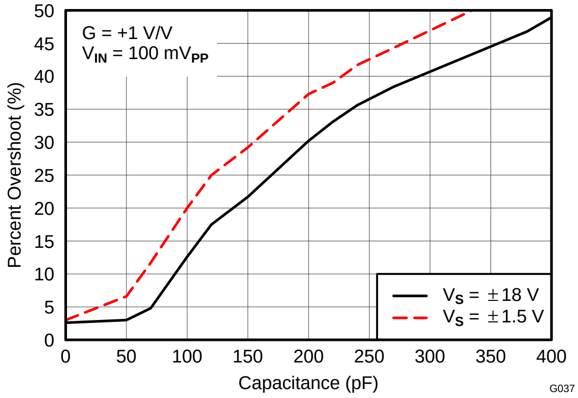


Figure 30.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

PHASE MARGIN vs CAPACITIVE LOAD

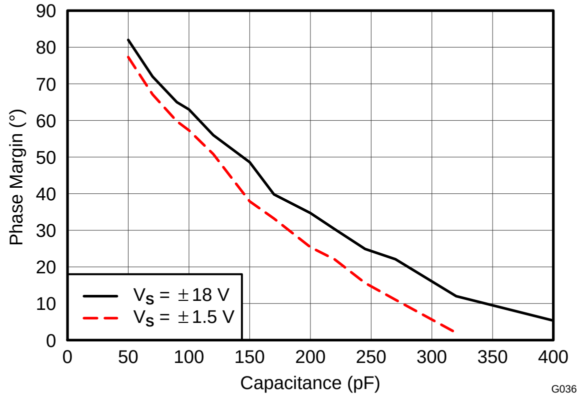


Figure 31.

OPEN-LOOP GAIN vs TEMPERATURE

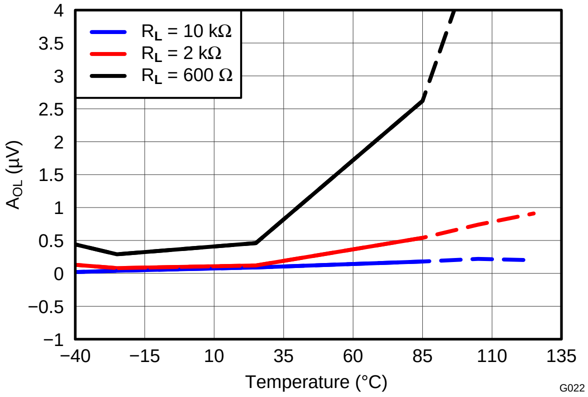


Figure 32.

I_B AND I_{OS} vs TEMPERATURE

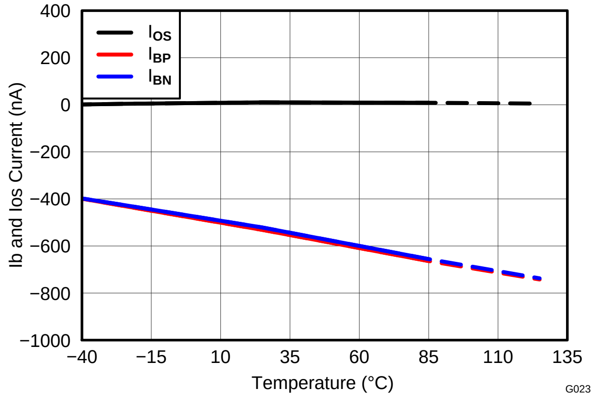


Figure 33.

I_B AND I_{OS} vs COMMON-MODE VOLTAGE

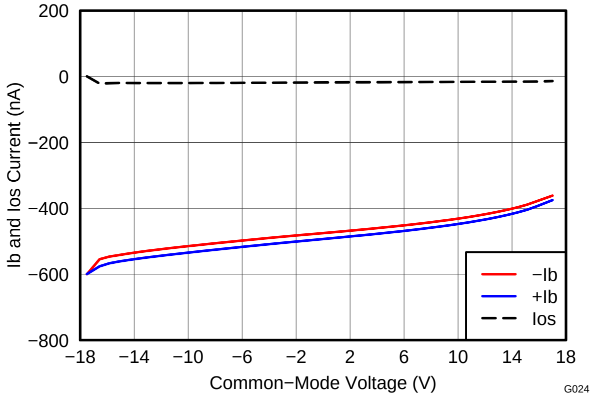


Figure 34.

SUPPLY CURRENT vs TEMPERATURE

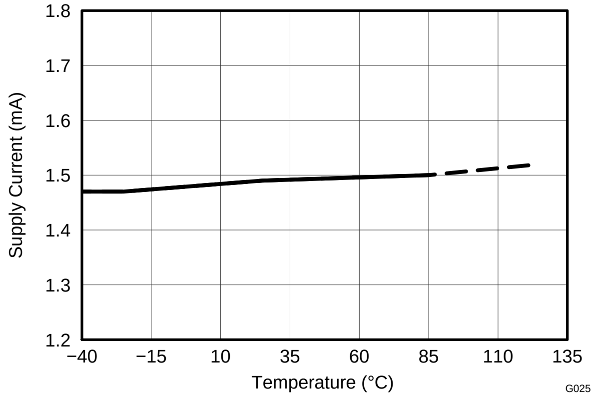


Figure 35.

SUPPLY CURRENT vs SUPPLY VOLTAGE

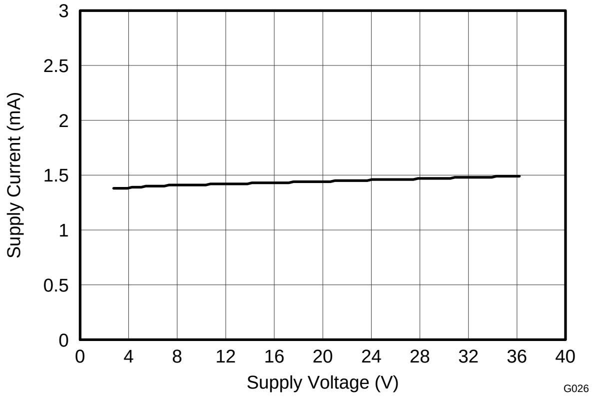


Figure 36.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

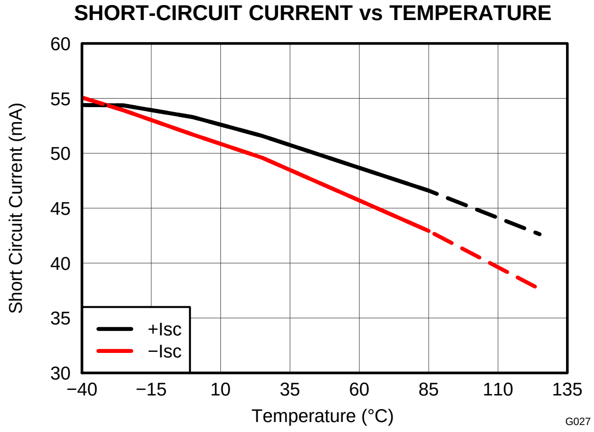


Figure 37.

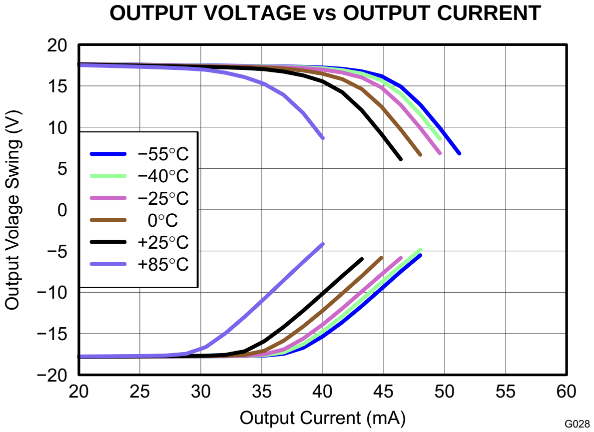


Figure 38.

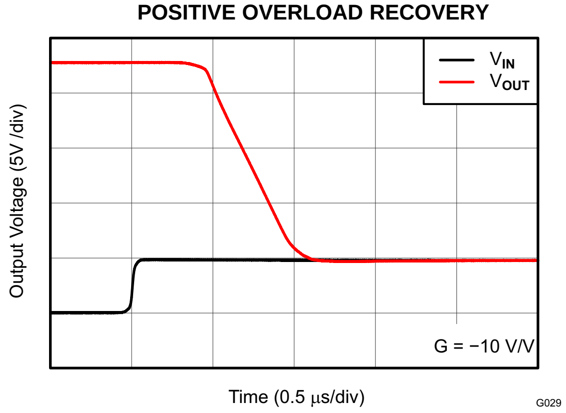


Figure 39.

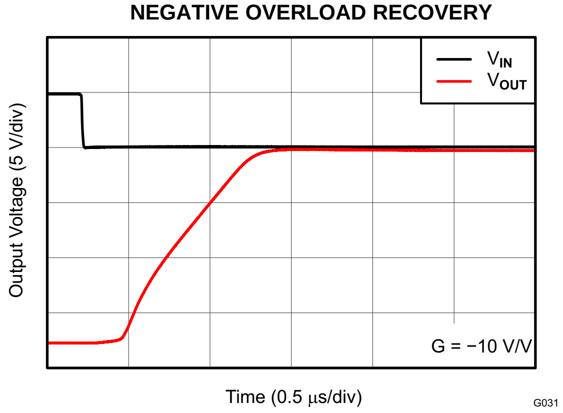


Figure 40.

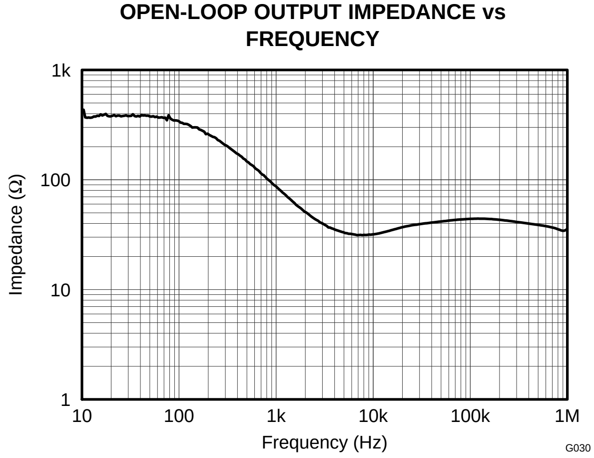


Figure 41.

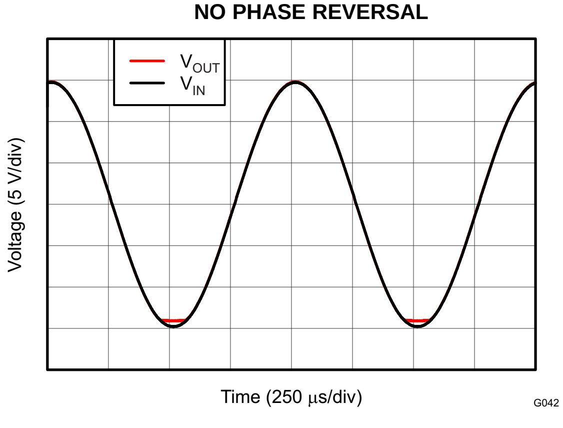


Figure 42.

APPLICATION INFORMATION

The OPA1662 and OPA1664 are unity-gain stable, precision dual and quad op amps with very low noise. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-μF capacitors are adequate. Figure 43 shows a simplified schematic of the OPA166x (one channel shown).

OPERATING VOLTAGE

The OPA166x series op amps operate from ±1.5 V to ±18 V supplies while maintaining excellent performance. The OPA166x series can operate with as little as +3 V between the supplies and with up to +36 V between the supplies. However, some applications do not require equal positive and negative output voltage swing. With the OPA166x series, power-supply voltages do not need to be equal. For example, the positive supply could be set to +25 V with the negative supply at –5 V.

In all cases, the common-mode voltage must be maintained within the specified range. In addition, key parameters are assured over the specified temperature range of T_A = –40°C to +85°C. Parameters that vary significantly with operating voltage or temperature are shown in the Typical Characteristics.

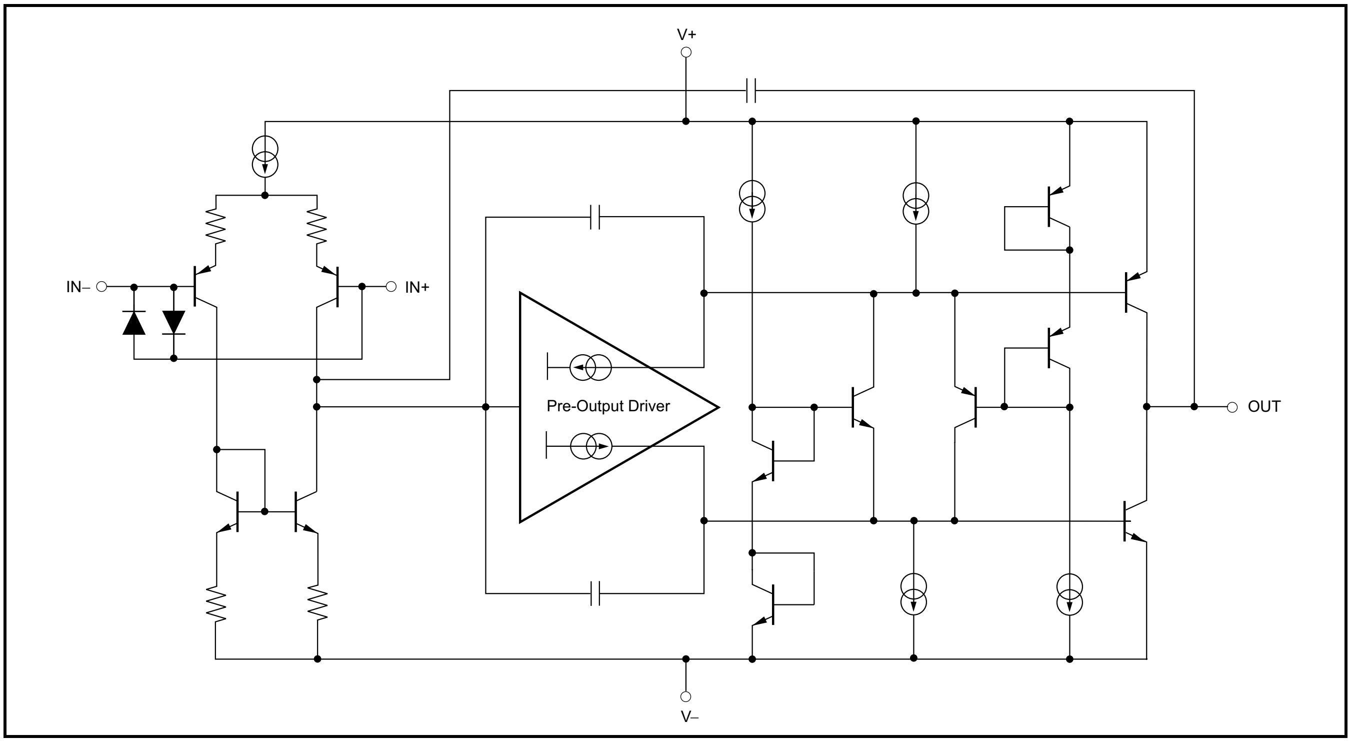


Figure 43. OPA166x Simplified Schematic

INPUT PROTECTION

The input terminals of the OPA1662 and OPA1664 are protected from excessive differential voltage with back-to-back diodes, as Figure 44 illustrates. In most circuit applications, the input protection circuitry has no consequence. However, in low-gain or G = +1 circuits, fast ramping input signals can forward bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward bias condition, the input signal current must be limited to 10 mA or less. If the input signal current is not inherently limited, an input series resistor (R_I) and/or a feedback resistor (R_F) can be used to limit the signal input current. This resistor degrades the low-noise performance of the OPA166x and is examined in the following *Noise Performance* section. Figure 44 shows an example configuration when both current-limiting input and feeback resistors are used.

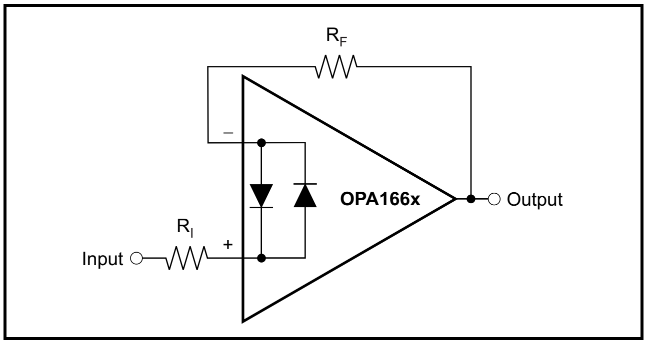


Figure 44. Pulsed Operation

NOISE PERFORMANCE

Figure 45 shows the total circuit noise for varying source impedances with the op amp in a unity-gain configuration (no feedback resistor network, and therefore no additional noise contributions).

The OPA166x (GBW = 22 MHz, G = +1) is shown with total circuit noise calculated. The op amp itself contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise op amp for a given application depends on the source impedance. For low source impedance, current noise is negligible, and voltage noise generally dominates. The low voltage noise of the OPA166x series op amps makes them a better choice for low source impedances of less than 1 kΩ.

The equation in Figure 45 shows the calculation of the total circuit noise, with these parameters:

- e_n = Voltage noise
- i_n = Current noise
- R_S = Source impedance
- k = Boltzmann's constant = 1.38×10^{-23} J/K
- T = Temperature in Kelvins (K)

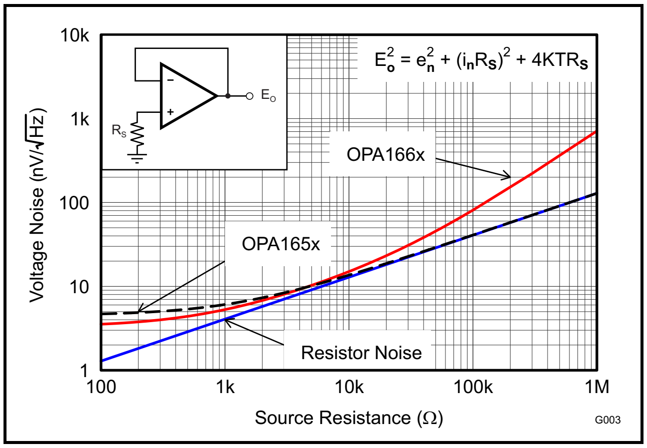


Figure 45. Noise Performance of the OPA166x in Unity-Gain Buffer Configuration

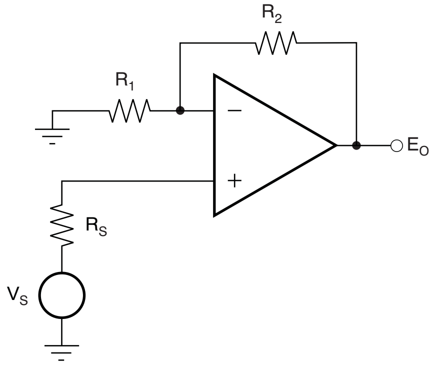
BASIC NOISE CALCULATIONS

Design of low-noise op amp circuits requires careful consideration of a variety of possible noise contributors: noise from the signal source, noise generated in the op amp, and noise from the feedback network resistors. The total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. Figure 45 plots this equation. The source impedance is usually fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

Figure 46 illustrates both inverting and noninverting op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. The current noise of the op amp reacts with the feedback resistors to create additional noise components. The feedback resistor values can generally be chosen to make these noise sources negligible. The equations for total noise are shown for both configurations.

A) Noise in Noninverting Gain Configuration



Noise at the output:

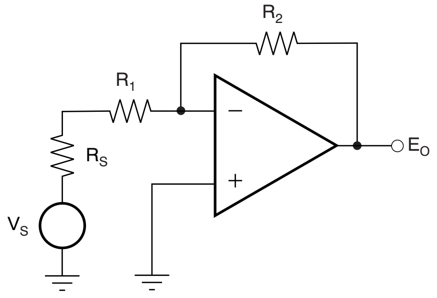
$$E_O^2 = \left(1 + \frac{R_2}{R_1}\right)^2 e_n^2 + \left(\frac{R_2}{R_1}\right)^2 e_1^2 + e_2^2 + \left(1 + \frac{R_2}{R_1}\right)^2 e_s^2$$

Where $e_S = \sqrt{4kTR_S}$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1}$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

B) Noise in Inverting Gain Configuration



Noise at the output:

$$E_O^2 = \left(1 + \frac{R_2}{R_1 + R_S}\right)^2 e_n^2 + \left(\frac{R_2}{R_1 + R_S}\right)^2 e_1^2 + e_2^2 + \left(\frac{R_2}{R_1 + R_S}\right)^2 e_s^2$$

Where $e_S = \sqrt{4kTR_S}$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1}$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

Note: For the OPA166x series of op amps at 1 kHz, e_n = 3.3 nV/√Hz.

Figure 46. Noise Calculation in Gain Configurations

TOTAL HARMONIC DISTORTION MEASUREMENTS

The OPA166x series op amps have excellent distortion characteristics. THD + noise is below 0.0006% (G = +1, V_O = 3 V_{RMS}, BW = 80kHz) throughout the audio frequency range, 20 Hz to 20 kHz, with a 2-kΩ load (see Figure 7 for characteristic performance).

The distortion produced by the OPA166x series op amps is below the measurement limit of many commercially available distortion analyzers. However, a special test circuit (such as Figure 47 shows) can be used to extend the measurement capabilities.

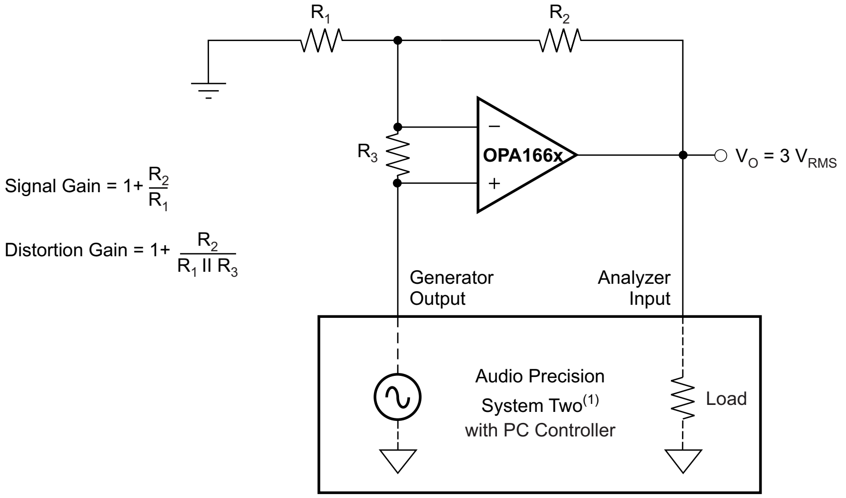
Op amp distortion can be considered an internal error source that can be referred to the input. Figure 47 shows a circuit that causes the op amp distortion to be gained up (refer to the table in Figure 47 for the distortion gain factor for various signal gains). The addition of R_3 to the otherwise standard noninverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by the distortion gain factor, thus extending the resolution by the same amount. Note that the input signal and load applied to the op amp are the same as with conventional feedback without R_3. The value of R_3 should be kept small to minimize its effect on the distortion measurements.

The validity of this technique can be verified by duplicating measurements at high gain and/or high frequency where the distortion is within the measurement capability of the test equipment. Measurements for this data sheet were made with an Audio Precision System Two distortion/noise analyzer, which greatly simplifies such repetitive measurements. The measurement technique can, however, be performed with manual distortion measurement instruments.

CAPACITIVE LOADS

The dynamic characteristics of the OPA1662 and OPA1664 have been optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (R_S equal to 50 Ω, for example) in series with the output.

This small series resistor also prevents excess power dissipation if the output of the device becomes shorted. Figure 25 illustrates a graph of *Small-Signal Overshoot vs Capacitive Load* for several values of R_S. Also, refer to Applications Bulletin AB-028 (literature number SBOA015, available for download from the TI web site) for details of analysis techniques and application circuits.



$$\text{Signal Gain} = 1 + \frac{R_2}{R_1}$$

$$\text{Distortion Gain} = 1 + \frac{R_2}{R_1 \parallel R_3}$$

SIGNAL GAIN	DISTORTION GAIN	R_1	R_2	R_3
+1	101	∞	1 kΩ	10 Ω
–1	101	4.99 kΩ	4.99 kΩ	49.9 Ω
+10	110	549 Ω	4.99 kΩ	49.9 Ω

(1) For measurement bandwidth, see Figure 7 through Figure 12.

Figure 47. Distortion Test Circuit

POWER DISSIPATION

The OPA1662 and OPA1664 series op amps are capable of driving 2-kΩ loads with a power-supply voltage up to ±18 V and full operating temperature range. Internal power dissipation increases when operating at high supply voltages. Copper leadframe construction used in the OPA166x series op amps improves heat dissipation compared to conventional materials. Circuit board layout can also help minimize junction temperature rise. Wide copper traces help dissipate the heat by acting as an additional heat sink. Temperature rise can be further minimized by soldering the devices to the circuit board rather than using a socket.

ELECTRICAL OVERSTRESS

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

It is helpful to have a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event. Figure 48 illustrates the ESD circuits contained in the OPA166x (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device internal to the OPA166x triggers when a fast ESD voltage pulse is impressed across the supply pins. Once triggered, it quickly activates, clamping the ESD pulse to a safe voltage level.

When the operational amplifier connects into a circuit such as that illustrated in Figure 48, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.

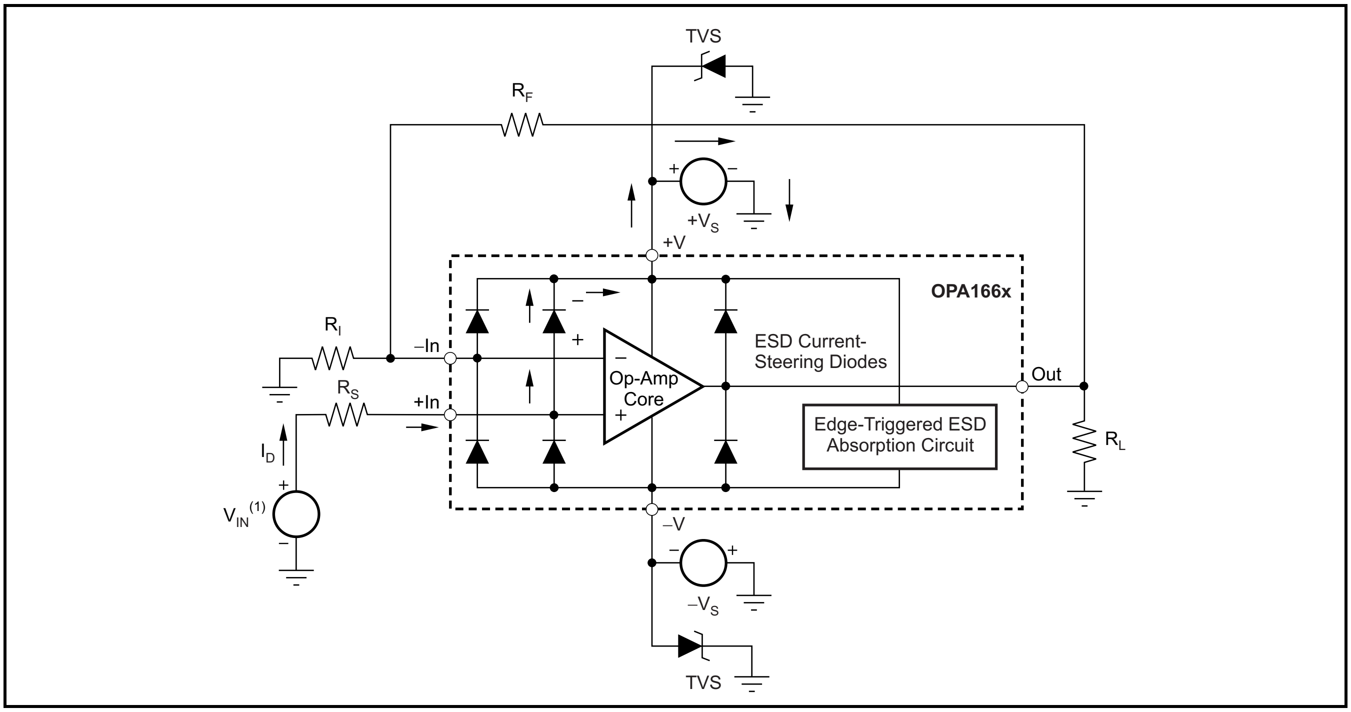
Figure 48 depicts a specific example where the input voltage, V_{IN}, exceeds the positive supply voltage ($+V_S$) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the datasheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings. In extreme but rare cases, the absorption device triggers on while $+V_S$ and $–V_S$ are applied. If this event happens, a direct current path is established between the $+V_S$ and $–V_S$ supplies. The power dissipation of the absorption device is quickly exceeded, and the extreme internal heating destroys the operational amplifier.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ and/or $–V_S$ are at 0 V. Again, it depends on the supply characteristic while at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source via the current steering diodes. This state is not a normal bias condition; the amplifier most likely will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is an uncertainty about the ability of the supply to absorb this current, external zener diodes may be added to the supply pins as shown in Figure 48.

The zener voltage must be selected such that the diode does not turn on during normal operation. However, its zener voltage should be low enough so that the zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.



(1) $V_{IN} = +V_S + 500mV$.

Figure 48. Equivalent Internal ESD Circuitry and Its Relation to a Typical Circuit Application (Single Channel Shown)

APPLICATION CIRCUIT

An additional application idea is shown in Figure 49.

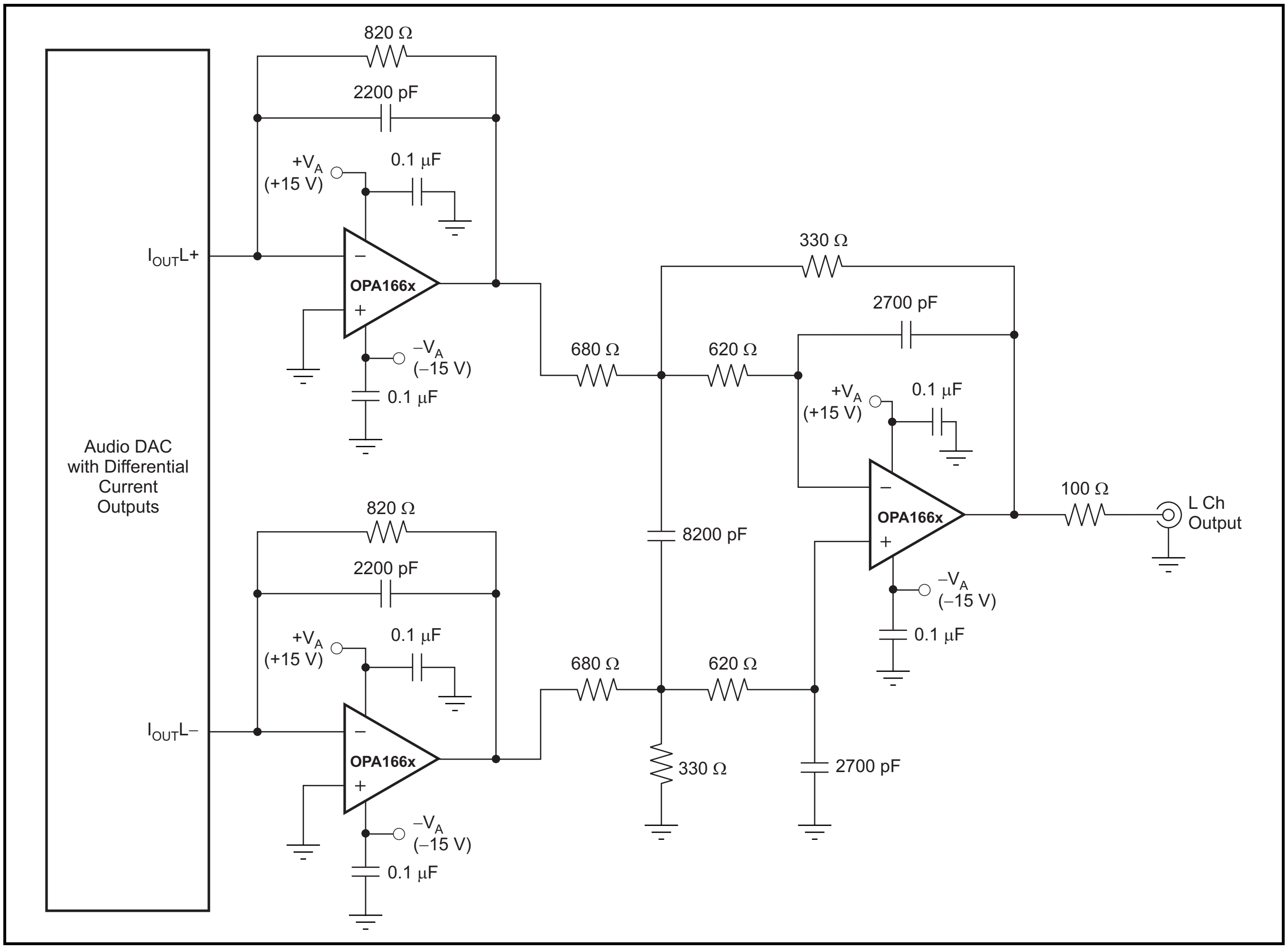


Figure 49. Audio DAC I/V Converter and Output Filter

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA1662AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP1662	Samples
OPA1662AIDGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	OUQI	Samples
OPA1662AIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | SN | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	OUQI	Samples
OPA1662AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP1662	Samples
OPA1664AID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA1664	Samples
OPA1664AIDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA1664	Samples
OPA1664AIPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA1664	Samples
OPA1664AIPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA1664	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

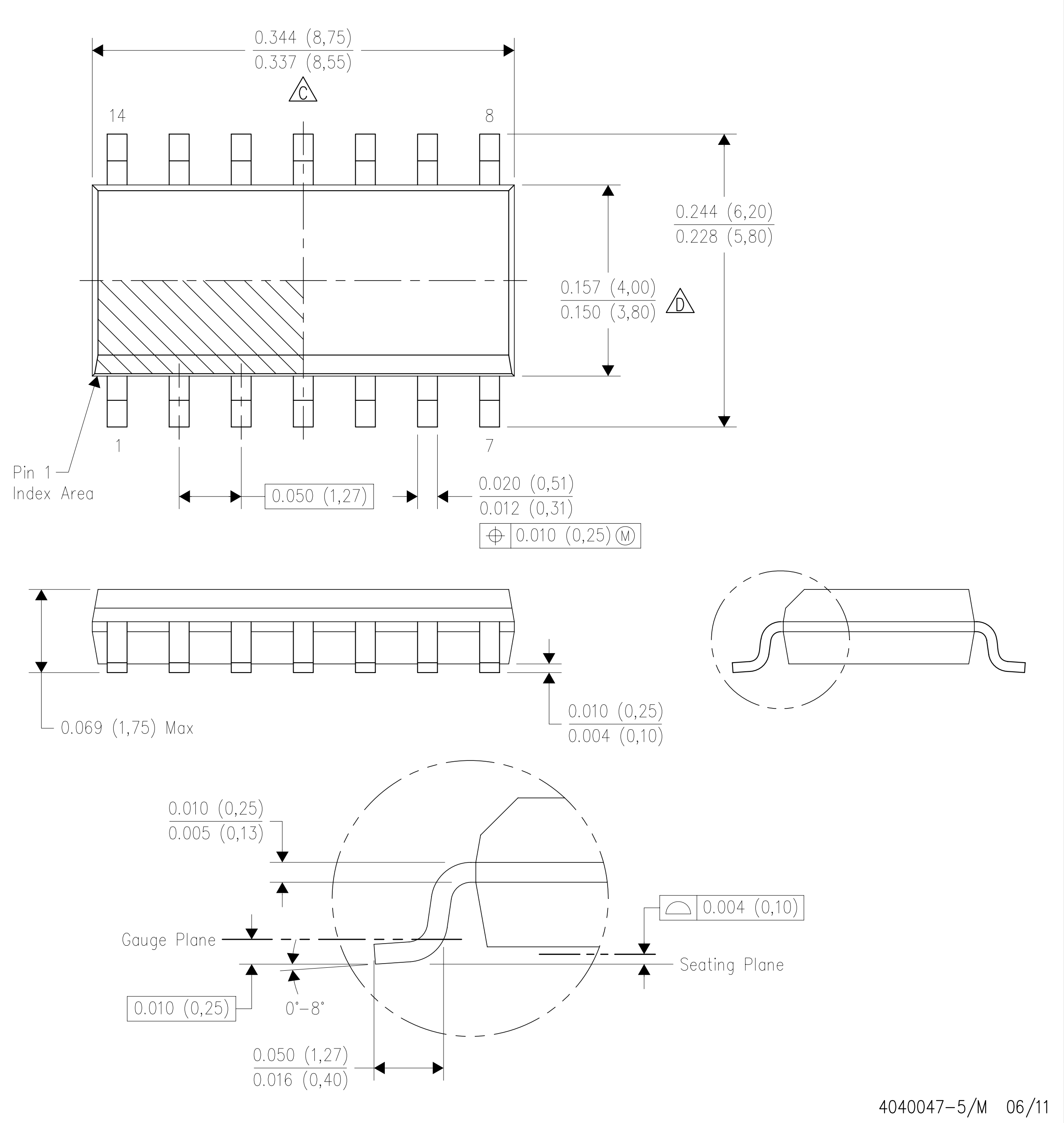
OTHER QUALIFIED VERSIONS OF OPA1662 :

- Automotive : OPA1662-Q1

NOTE: Qualified Version Definitions:

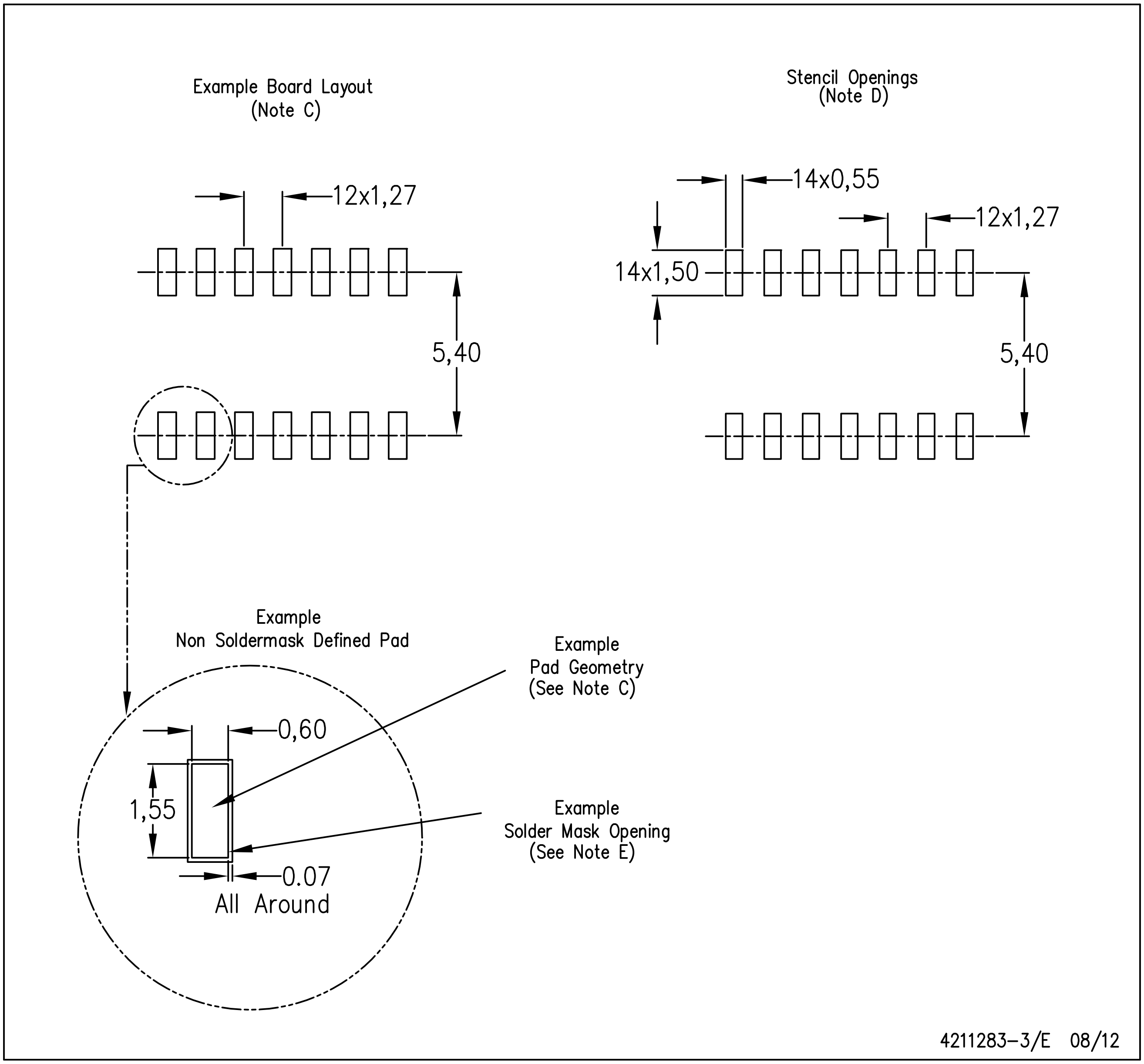
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



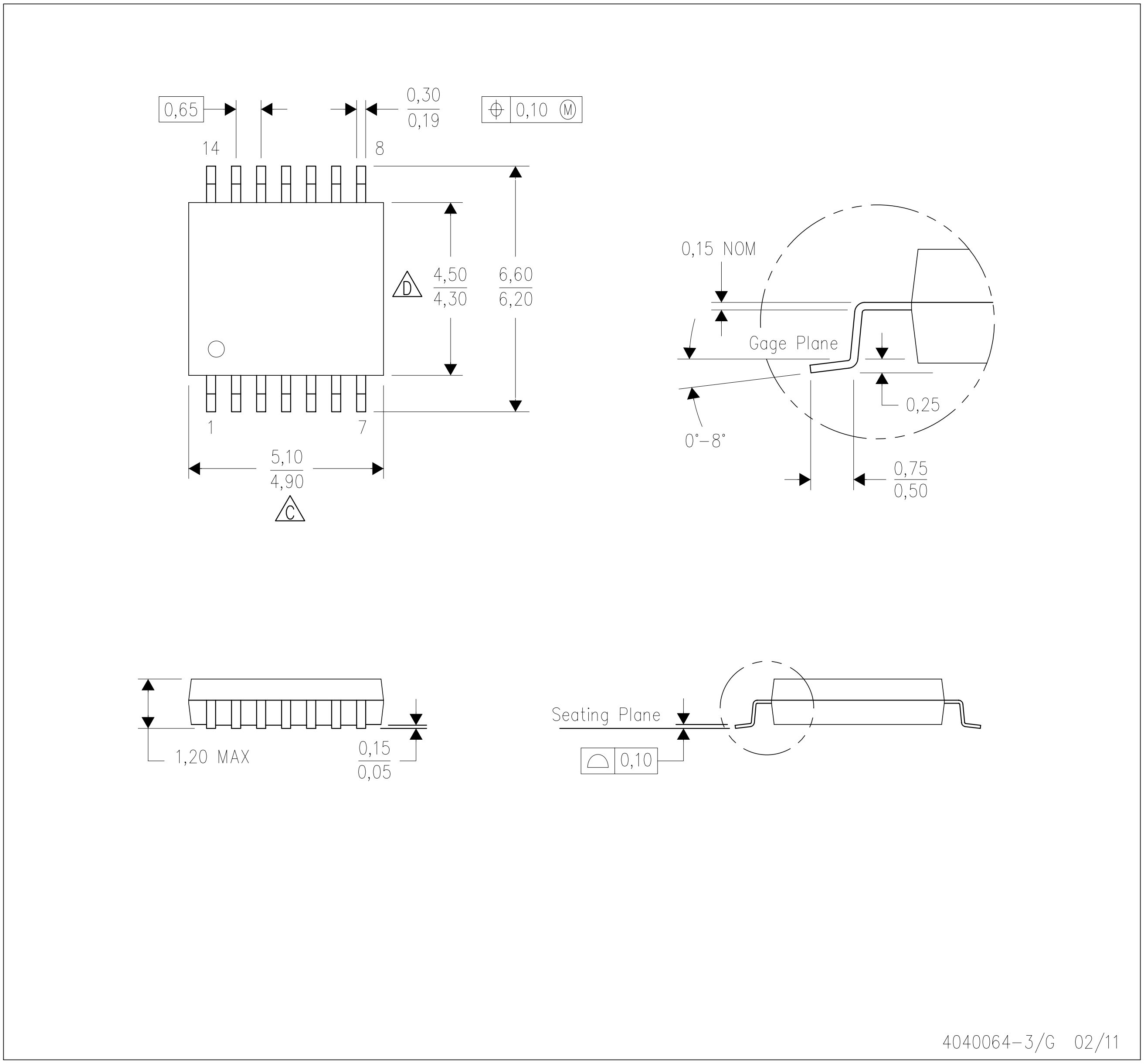
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE

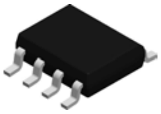


NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO–153

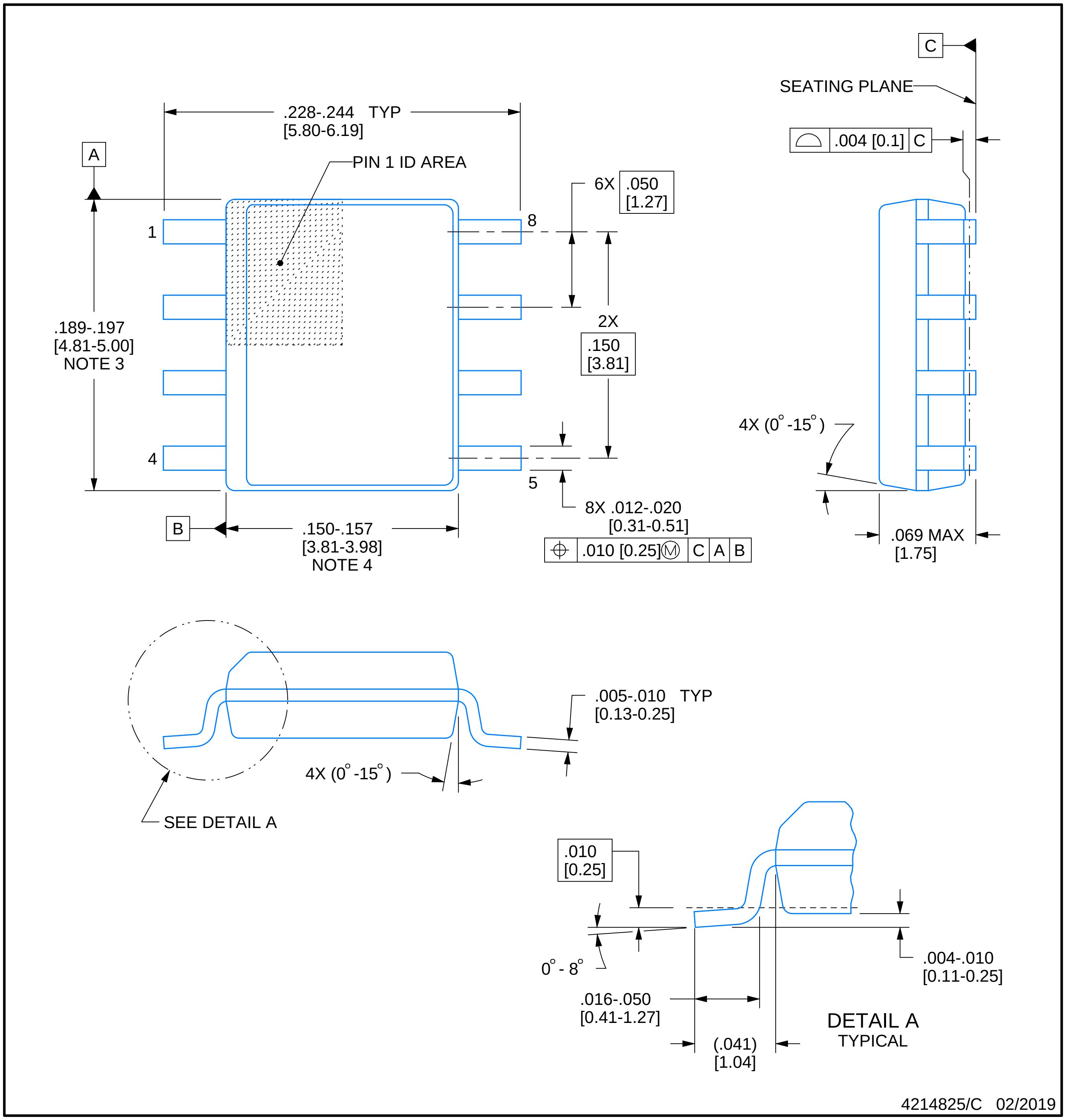


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

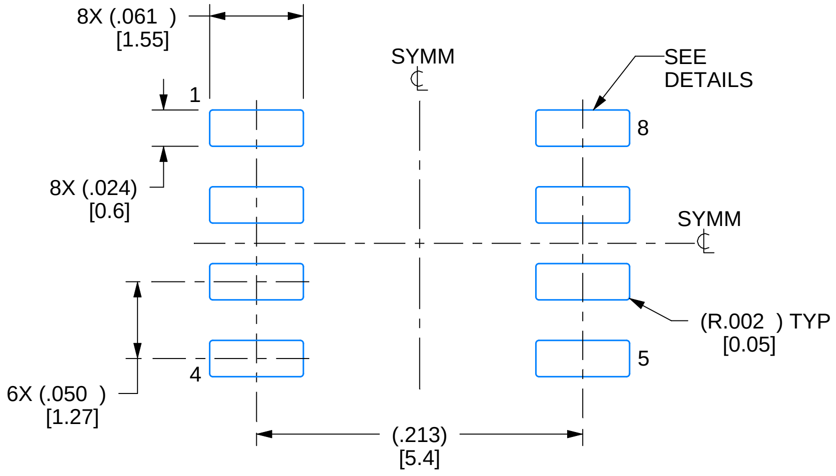
SMALL OUTLINE INTEGRATED CIRCUIT



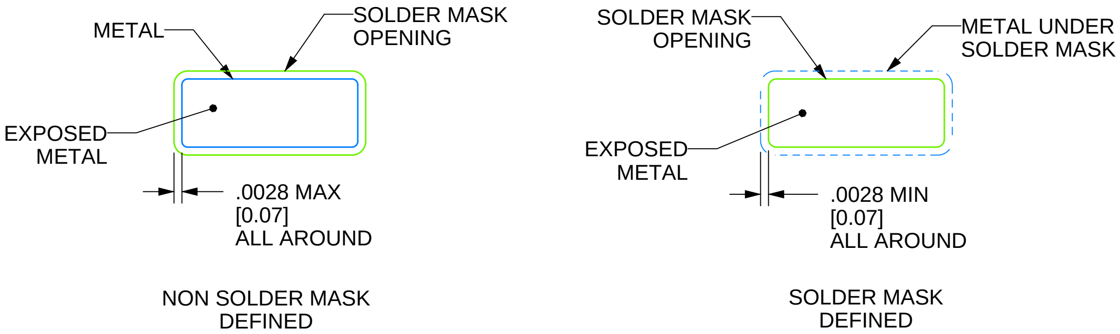
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



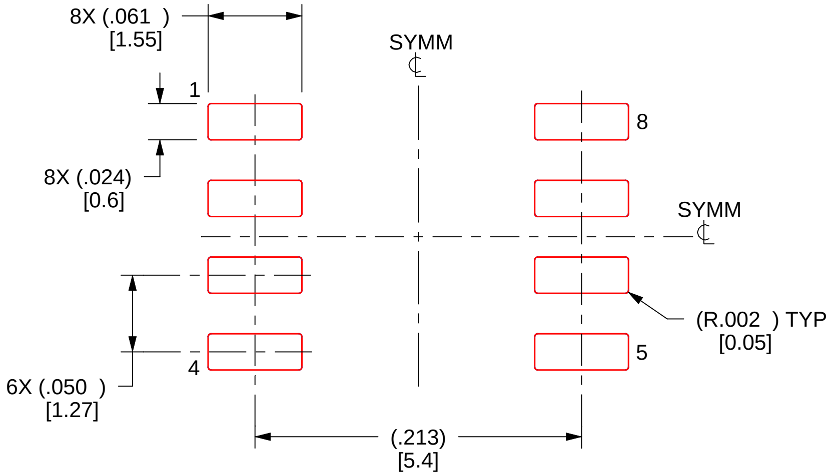
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

NOTES: (continued)

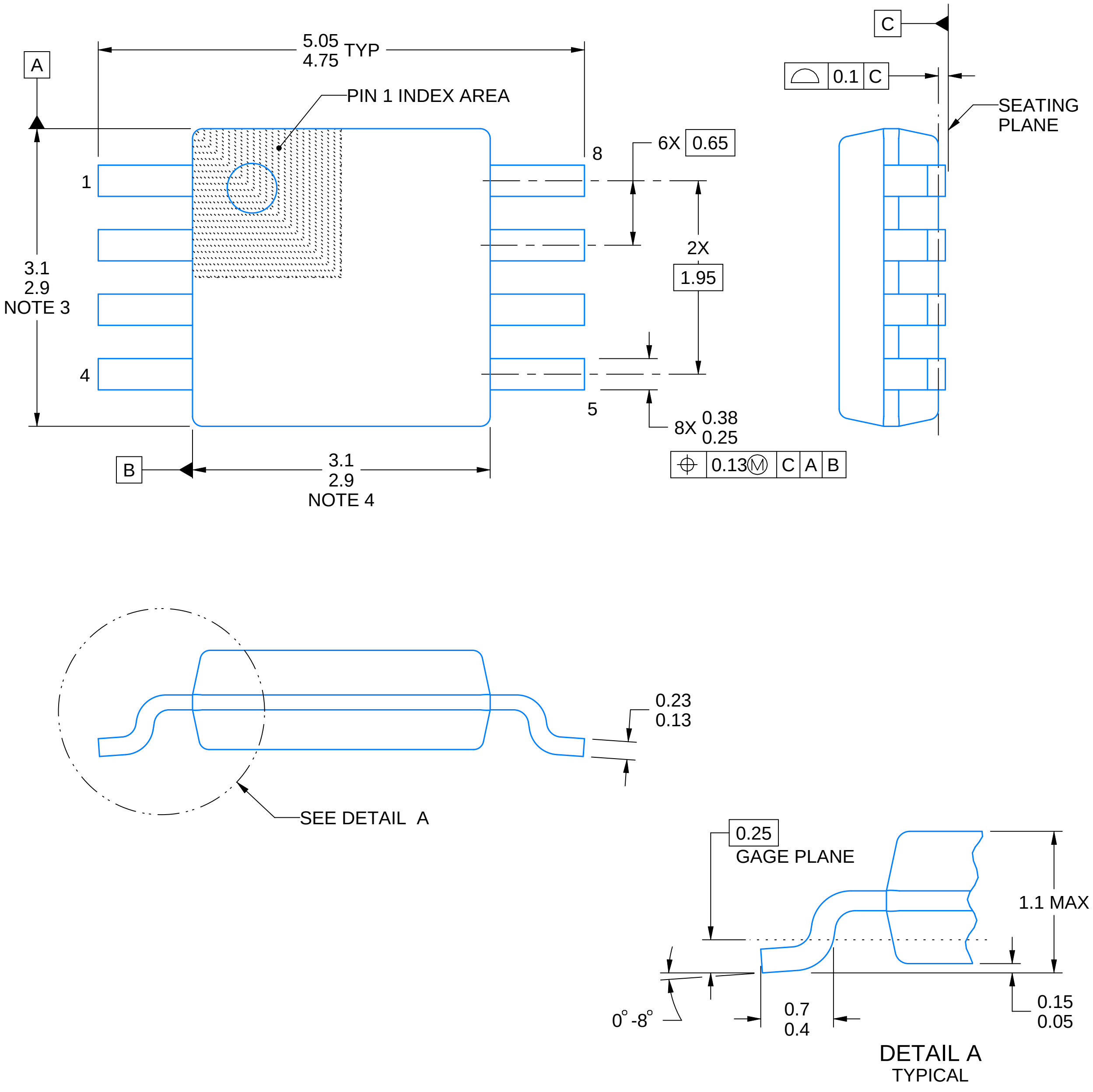
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

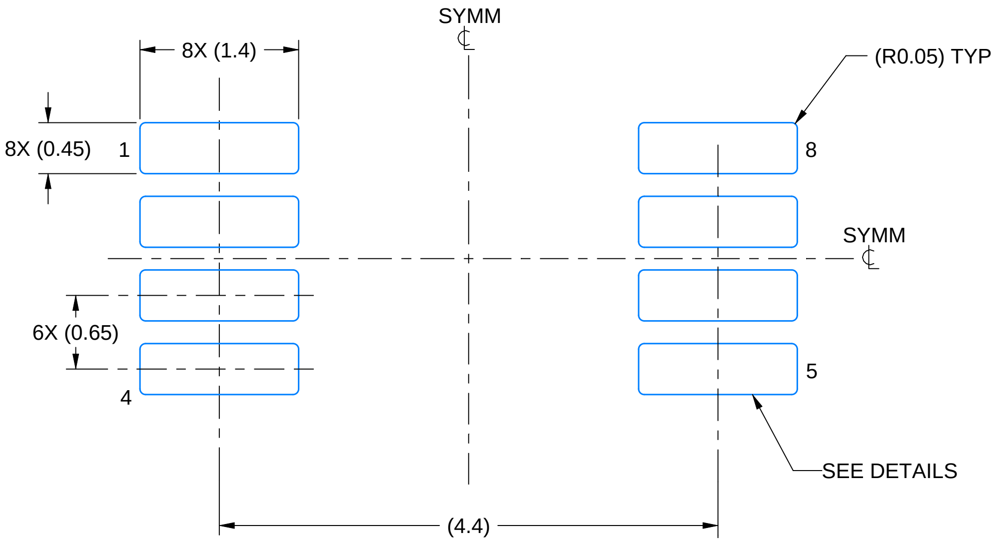


4214862/A 04/2023

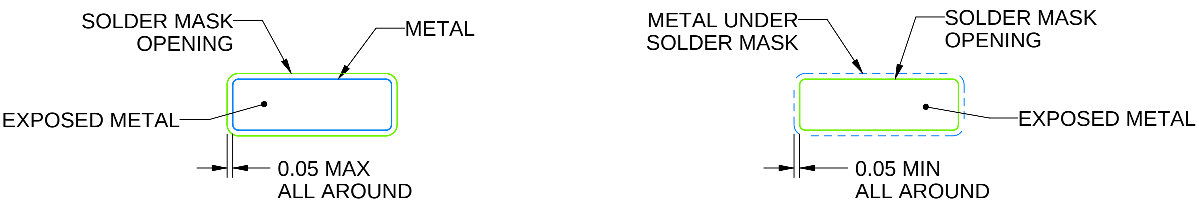
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



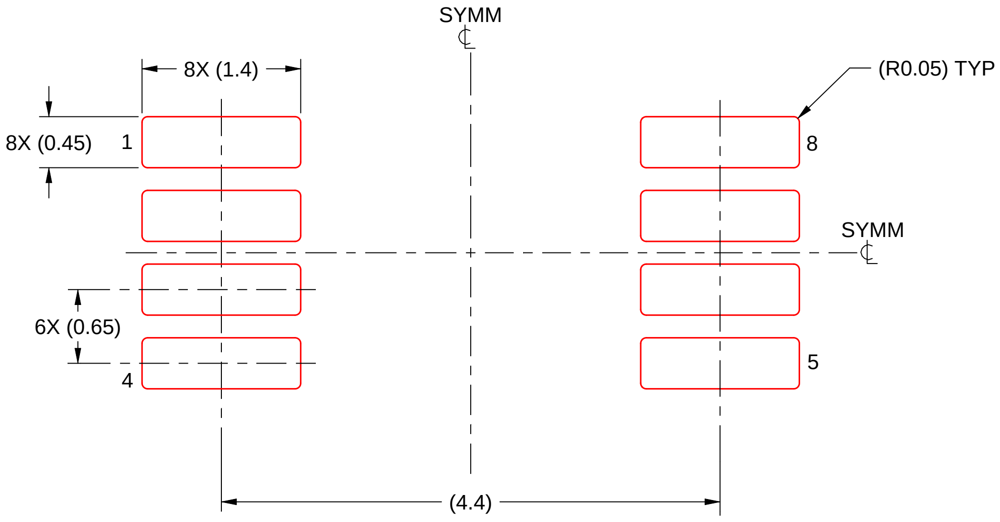
NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.