

SN65LBC174、SN75LBC174 四通道低功耗差分线路接收器

1 特性

- 符合或超出标准 EIA-485
- 适用于嘈杂环境中长总线上的高速多点传输
- 支持高达并超过每秒 1000 万次传输的数据速率
- 7V 至 12V 的共模输出电压范围
- 正负电流限制
- 低功耗：1.5mA 最大电流（禁用输出）
- 与 SN75174 在功能上可以互换

2 应用

- 化学和气体传感器
- 现场变送器：温度传感器和压力传感器
- 电机控制：无刷直流和有刷直流
- 采用 Modbus 的温度传感器和控制器

3 说明

SN65LBC174 和 SN75LBC174 是具有三态输出的单片四通道差分线路接收器。这两种器件都符合电子工业协会标准 EIA-485 的要求。这些器件经优化，能够以高达和超过 10Mbit/s 的速率实现平衡多点总线传输。每个驱动器都具有较宽的正负共模输出电压范围、电流限制和热关断保护，因此适用于嘈杂环境中的合用线应

用。这两种器件采用 LinBiCMOS™ 进行设计，有助于实现超低功耗和固有的稳健性。

SN65LBC174 和 SN75LBC174 均可提供正负电流限制和热关断功能，避免传输总线出现线路故障状况。这些器件会在与 SN75LBC173 或 SN75LBC175 四通道线路驱动器配合使用时提供卓越性能。SN65LBC174 和 SN75LBC174 采用 16 端子 DIP 封装 (N) 和 20 端子宽体 Small-outline Integrated Circuit (SOIC) 封装 (DW)。

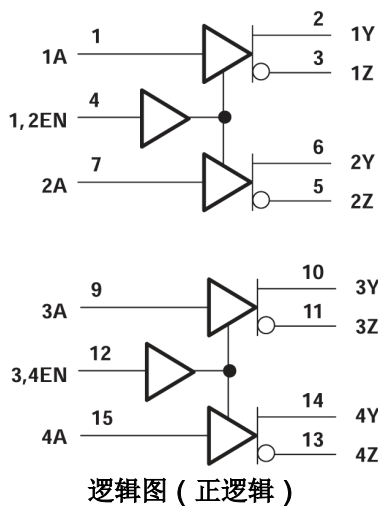
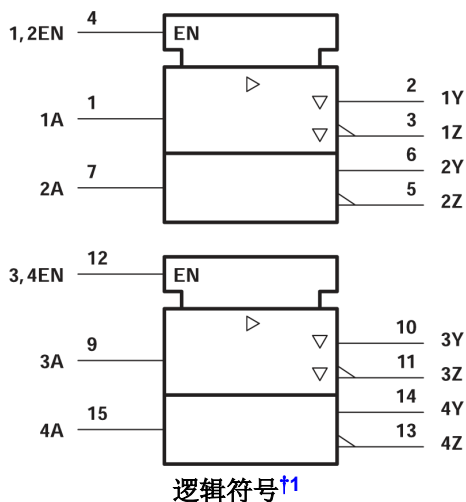
SN75LBC174 可在 0°C 至 70°C 的商业温度范围内运行。SN65LBC174 可在 -40°C 至 85°C 的工业温度范围内运行。

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾
SN65LBC174	DW	12.8mm x 10.3mm
	N	19.3mm x 9.4mm
SN75LBC174	DW	12.8mm x 10.3mm
	N	19.3mm x 9.4mm

(1) 有关更多信息，请参阅节 10。

(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



[†] 此符号符合 ANSI/IEEE 标准 91-1984 和 IEC 出版物 617-12。

¹ 所示引脚编号适用于 N 封装。



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4 Pin Configuration and Functions

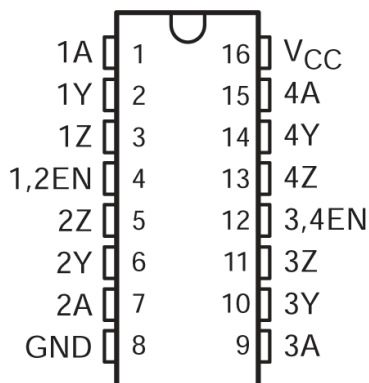
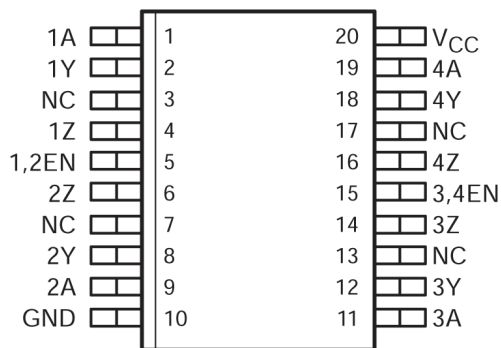


图 4-1. N Package (Top View)

表 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
1A	1	I	Driver 1 input
1Y	2	O	Driver 1 output
1Z	3	O	Driver 1 inverted output
1,2EN	4	I	Active high driver enable channel 1 and 2
2Z	5	O	Driver 2 inverted output
2Y	6	O	Driver 2 output
2A	7	I	Driver 2 input
GND	8	-	Ground pin
3A	9	I	Driver 3 input
3Y	10	O	Driver 3 output
3Z	11	O	Driver 3 inverted output
3,4EN	12	I	Active high driver enable channel 3 and 4
4Z	13	O	Driver 4 inverted output
4Y	14	O	Driver 4 output
4A	15	I	Driver 4 input
V _{CC}	16	-	Power pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.



NC – No internal connection

图 4-2. DW Package (Top View)

表 4-2. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
1A	1	I	Driver 1 input
1Y	2	O	Driver 1 output
NC	3	-	No Internal Connection
1Z	4	O	Driver 1 inverted output
1,2EN	5	I	Active high driver enable channel 1 and 2
2Z	6	O	Driver2 inverted output
NC	7	-	No Internal Connection
2Y	8	O	Driver 2 output
2A	9	I	Driver 2 input
GND	10	-	Ground pin
3A	11	I	Driver 3 input
3Y	12	O	Driver 3 output
NC	13	-	No Internal Connection
3Z	14	O	Driver 3 inverted output
3,4EN	15	I	Active high driver enable channel 3 and 4
4Z	16	O	Driver 4 inverted output
NC	17	-	No Internal Connection
4Y	18	O	Driver 4 output
4A	19	I	Driver 4 input
V _{CC}	20	-	Power pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) ⁽¹⁾

			MIN	MAX	UNIT
V_{CC} (see Note 1)	Supply voltage range, see Note ⁽²⁾		- 0.3	7	V
V_O	Output voltage range		- 10	15	V
V	Voltage range at A, 1/2EN, 3/4EN		- 0.3	$V_{CC} + 0.5$	V
P_D	Continuous total power dissipation		Internally limited ⁽²⁾		
T_A	Operating free-air temperature range:	SN65LBC174	- 40	85	°C
		SN75LBC174	0	70	°C
T_{stg}	Storage temperature range		- 65	150	°C
T_{lead}	Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds			260	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The maximum operating junction temperature is internally limited. Use the Dissipation Rating Table to operate below this temperature.
NOTE 1: All voltage values are with respect to GND.

5.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Voltage at any bus terminal (separately or common-mode), V_O	Y or Z			12	V
				- 7	
High-level output current, I_{OH}	Y or Z			- 60	mA
Low-level output current, I_{OL}	Y or Z			60	mA
Continuous total power dissipation		See Dissipation Rating Table			
Operating free-air temperature, T_A	SN65LBC174	- 40		85	°C
	SN75LBC174	0		70	

5.3 Dissipation Rating Table

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
DW	1125mW	9.0mW/°C	720mW	585mW
N	1150mW	9.2mW/°C	736mW	598mW

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		DW	UNIT
		20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	66.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	39	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -18\text{mA}$				-1.5	V
$ V_{OD} $	Differential output voltage ⁽²⁾	$R_L = 54\ \Omega$, See 图 6-1	SN65LBC174	1.1	1.8	5	V
			SN75LBC174	1.5	1.8	5	
		$R_L = 60\ \Omega$, See 图 6-2	SN65LBC174	1.1	1.7	5	
			SN75LBC174	1.5	1.7	5	
$\Delta V_{OD} $	Change in magnitude of common-mode output voltage ⁽³⁾	$R_L = 54\ \Omega$, See 图 6-1				± 0.2	V
V_{OC}	Common-mode output voltage			-1		3	V
$\Delta V_{OC} $	Change in magnitude of common-mode output voltage ⁽³⁾					± 0.2	V
I_O	Output current with power off	$V_{CC} = 0$,	$V_O = -7\text{V to }12\text{V}$			± 100	μA
I_{OZ}	High-impedance-state output current	$V_O = -7\text{V to }12\text{V}$				± 100	μA
I_{IH}	High-level input current	$V_I = 2.4\text{V}$				-100	μA
I_{IL}	Low-level input current	$V_I = 0.4\text{V}$				-100	μA
I_{OS}	Short-circuit output current	$V_O = -7\text{V to }12\text{V}$				± 250	mA
I_{CC}	Supply current (all drivers)	No load	Outputs enabled			7	mA
			Outputs disabled			1.5	

- (1) All typical values are at $V_{CC} = 5\text{V}$ and $T_A = 25^\circ\text{C}$.
 (2) The minimum V_{OD} specification does not fully comply with EIA-485 at operating temperatures below 0°C . The lower output signal should be used to determine the maximum signal transmission distance.
 (3) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} , respectively, that occur when the input is changed from a high level to a low level.

5.6 Switching Characteristics

$V_{CC} = 5V$, $T_A = 25^\circ C$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	$R_L = 54\Omega$,	See 图 6-3	2	11	20	ns
$t_{t(OD)}$	Differential output transition time			9	15	25	ns
t_{PZH}	Output enable time to high level	$R_L = 110\Omega$,	See 图 6-3		20	30	ns
t_{PZL}	Output enable time to low level	$R_L = 110\Omega$,	See 图 6-5		21	30	ns
t_{PHZ}	Output disable time from high level	$R_L = 110\Omega$,	See 图 6-4		48	70	ns
t_{PLZ}	Output disable time from low level	$R_L = 110\Omega$,	See 图 6-5		21	30	ns

5.7 Typical Characteristics

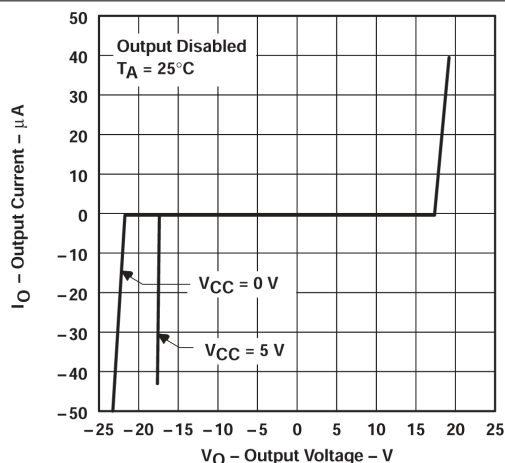


图 5-1. Output Current vs Output Voltage

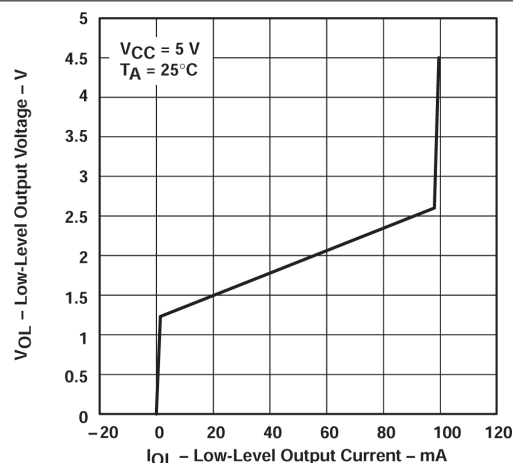


图 5-2. Low-level Output Voltage vs Low-level Output Current

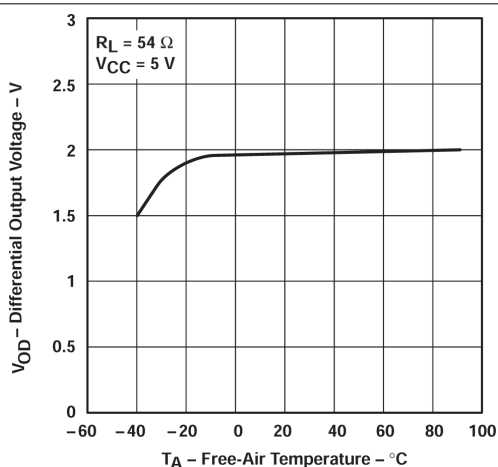


图 5-3. Differential Output Voltage vs Free-air Temperature

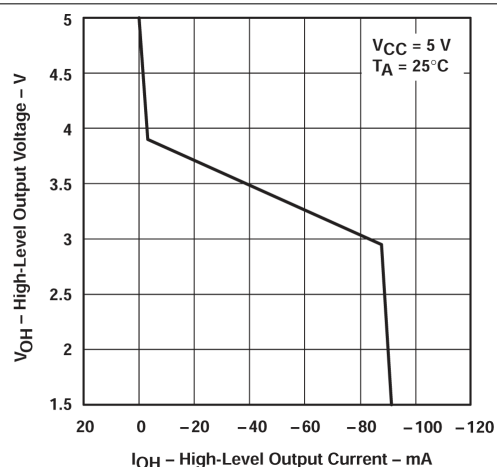


图 5-4. High-level Output Voltage vs High-level Output Current

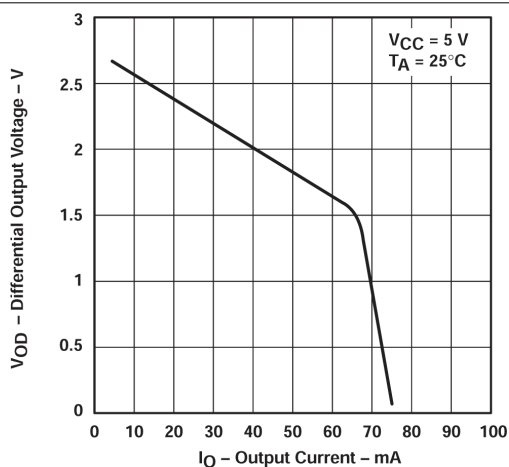


图 5-5. Differential Output Voltage vs Output Current

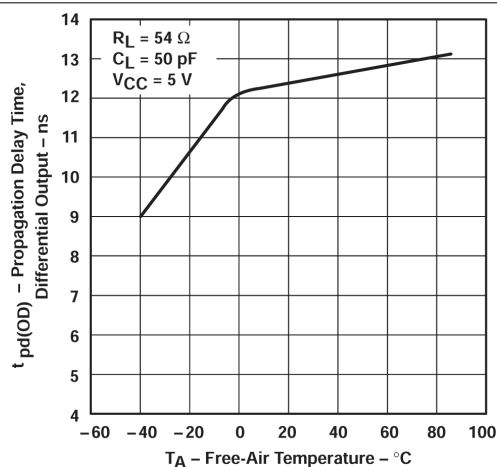


图 5-6. Propagation Delay Time, Differential Output vs Free-air Temperature

6 Parameter Measurement Information

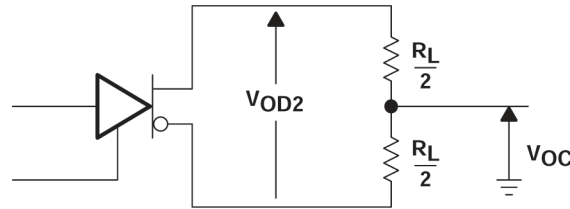


图 6-1. Differential and Common-Mode Output Voltages

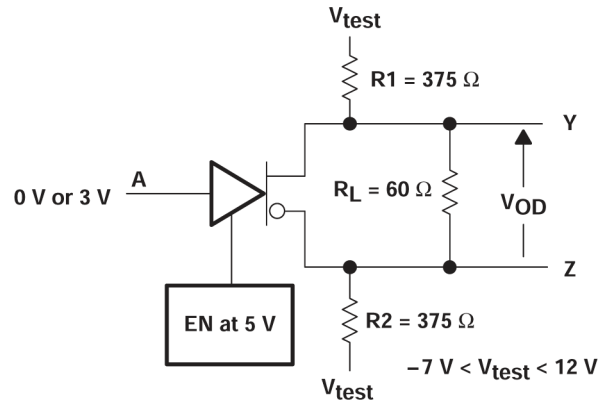
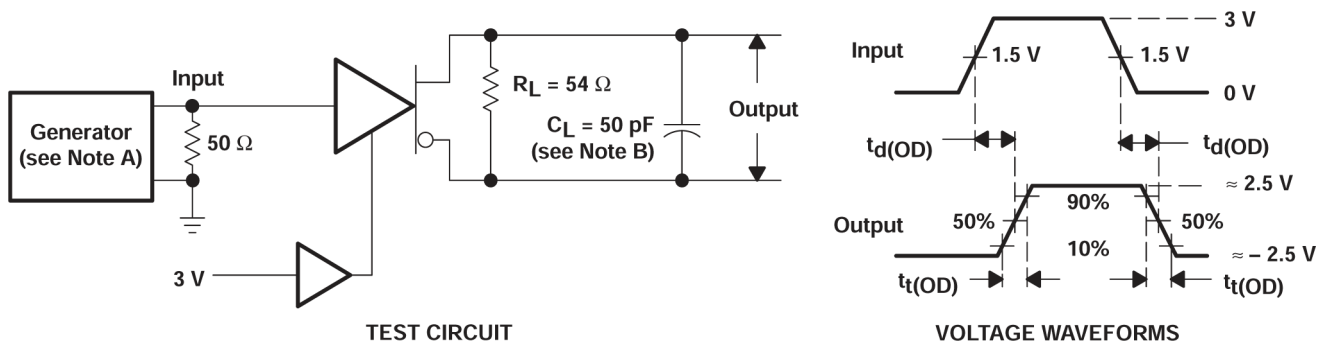


图 6-2. Driver V_{OD} Test Circuit



- A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1\text{ MHz}$, duty cycle = 50%, $t_r \leq 5\text{ ns}$, $t_f \leq 5\text{ ns}$, $Z_O = 50\Omega$.
- B. C_L includes probe and stray capacitance.

图 6-3. Time Waveforms for Driver Differential Output Test Circuit Delay and Transition

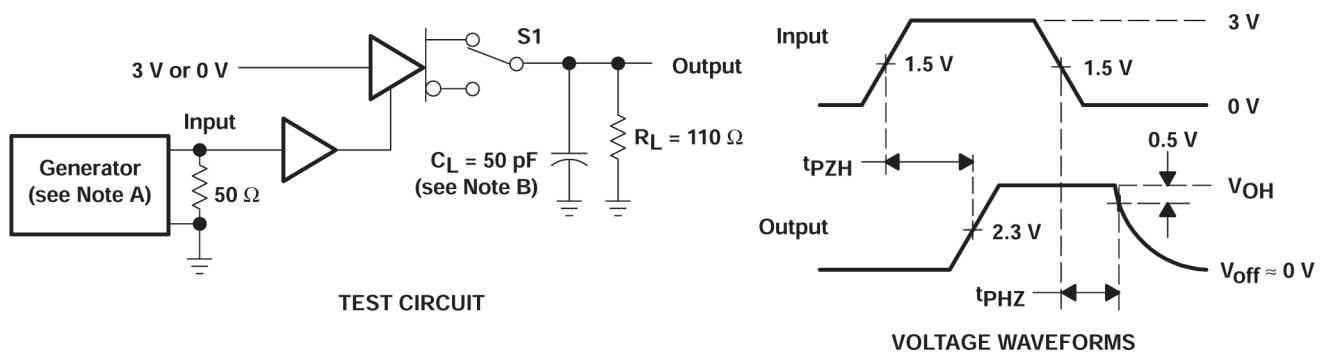
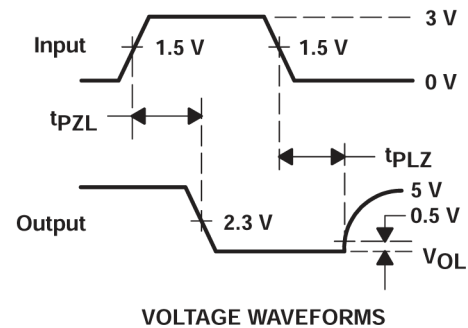
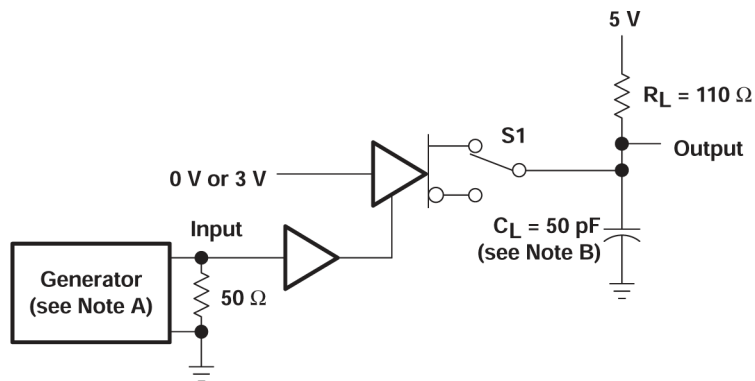


图 6-4. t_{PZH} and t_{PHZ} Test Circuit and Waveforms



TEST CIRCUIT

- The input pulse is supplied by a generator having the following characteristics: $\text{PRR} \leq 1\text{MHz}$, duty cycle = 50%, $t_r \leq 5\text{ns}$, $t_f \leq 5\text{ns}$, $Z_O = 50\ \Omega$.
- C_L includes probe and stray capacitance.

图 6-5. t_{pZL} and t_{pLZ} Test Circuit and Waveforms

7 Detailed Description

7.1 Thermal Characteristics of Ic Packages

θ_{JA} (Junction-to-Ambient Thermal Resistance) is defined as the difference in junction temperature to ambient temperature divided by the operating power

θ_{JA} is NOT a constant and is a strong function of

- the PCB design (50% variation)
- altitude (20% variation)
- device power (5% variation)

θ_{JA} can be used to compare the thermal performance of packages if the specific test conditions are defined and used. Standardized testing includes specification of PCB construction, test chamber volume, sensor locations, and the thermal characteristics of holding fixtures. θ_{JA} is often misused when it is used to calculate junction temperatures for other installations.

TI uses two test PCBs as defined by JEDEC specifications. The low-k board gives *average* in-use condition thermal performance and consists of a single trace layer 25mm long and 2-oz thick copper. The high-k board gives *best case* in-use condition and consists of two 1-oz buried power planes with a single trace layer 25 mm long with 2-oz thick copper. A 4% to 50% difference in θ_{JA} can be measured between these two test cards

θ_{JC} (Junction-to-Case Thermal Resistance) is defined as difference in junction temperature to case divided by the operating power. It is measured by putting the mounted package up against a copper block cold plate to force heat to flow from die, through the mold compound into the copper block.

θ_{JC} is a useful thermal characteristic when a heatsink is applied to package. It is NOT a useful characteristic to predict junction temperature as it provides pessimistic numbers if the case temperature is measured in a non-standard system and junction temperatures are backed out. It can be used with θ_{JB} in 1-dimensional thermal simulation of a package system.

θ_{JB} (Junction-to-Board Thermal Resistance) is defined to be the difference in the junction temperature and the PCB temperature at the center of the package (closest to the die) when the PCB is clamped in a cold-plate structure. θ_{JB} is only defined for the high-k test card.

θ_{JB} provides an overall thermal resistance between the die and the PCB. Including a bit for the PCB thermal resistance (especially for BGAs with thermal balls), and can be used for simple 1-dimensional network analysis of package system (see 图 7-1).

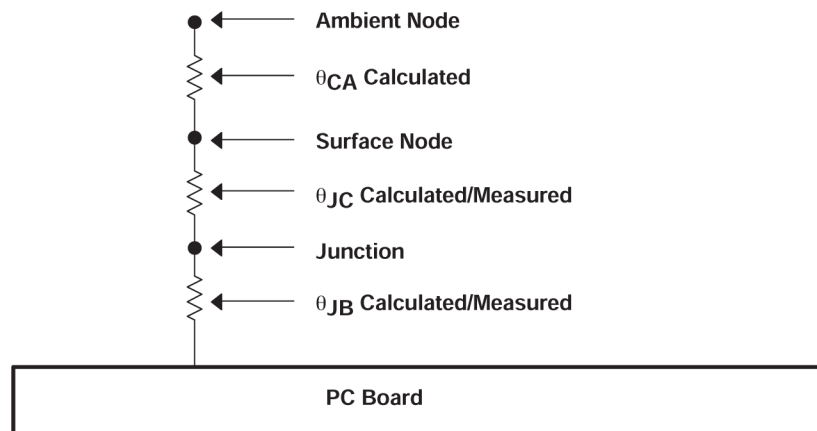


图 7-1. Thermal Resistance

7.2 Device Functional Modes

表 7-1. Functional Tables (Each Driver)

INPUT ⁽¹⁾	ENABLE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)

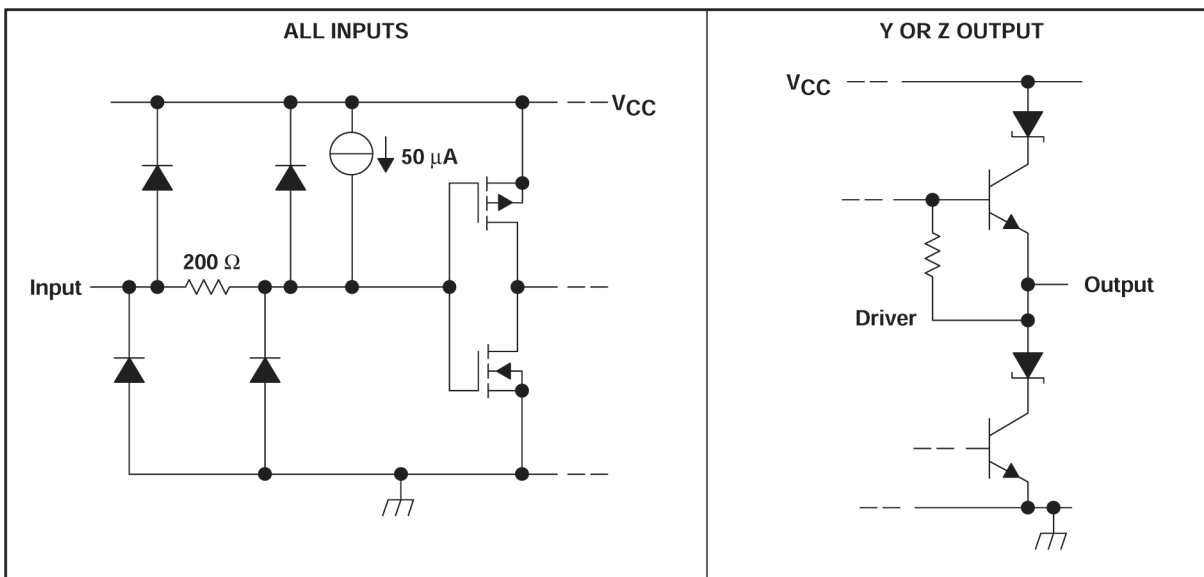


图 7-2. Schematic of Inputs and Outputs

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.2 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

8.3 Trademarks

LinBiCMOS™ and TI E2E™ are trademarks of Texas Instruments.
所有商标均为其各自所有者的财产。

8.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision E (April 2006) to Revision F (April 2024)	Page
• 更改了整个文档中的表格、图和交叉参考的编号格式.....	1
• Added the <i>Thermal Information</i> table.....	6
• Changed the $t_{(OD)}$ MIN value from 10ns to 9ns in the <i>Switching Characteristics</i>	7

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65LBC174DW	Obsolete	Production	SOIC (DW) 20	-	-	Call TI	Call TI	-40 to 85	SN65LBC174
SN65LBC174DWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SN65LBC174
SN65LBC174DWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SN65LBC174
SN65LBC174N	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN65LBC174N
SN65LBC174N.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	SN65LBC174N
SN75LBC174DW	Obsolete	Production	SOIC (DW) 20	-	-	Call TI	Call TI	0 to 70	SN75LBC174
SN75LBC174N	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75LBC174N
SN75LBC174N.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75LBC174N

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN75LBC174 :

- Military : [SN55LBC174](#)

NOTE: Qualified Version Definitions:

- Military - QML certified for Military and Defense Applications

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



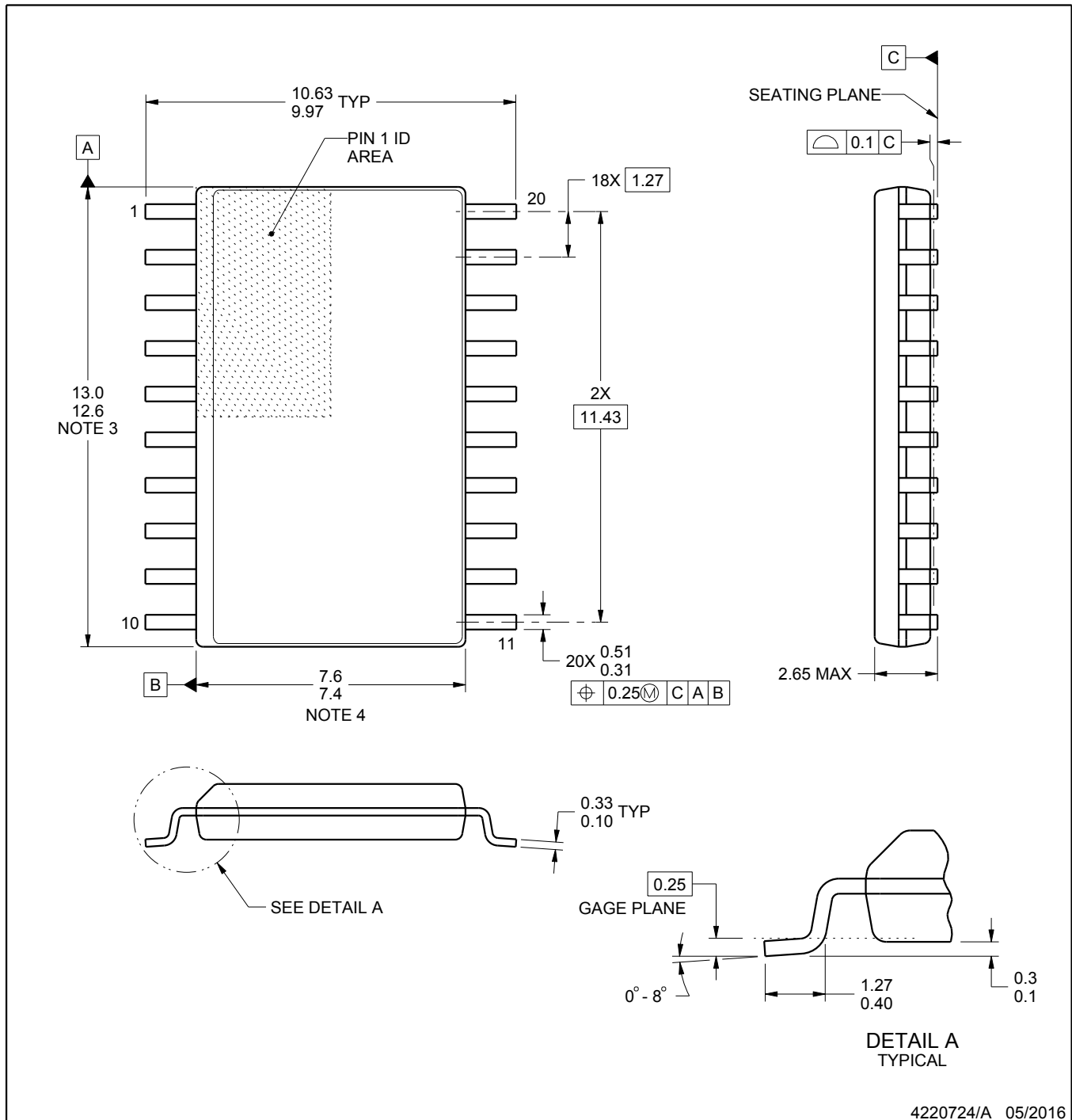
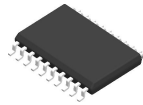
PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.



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NOTES:

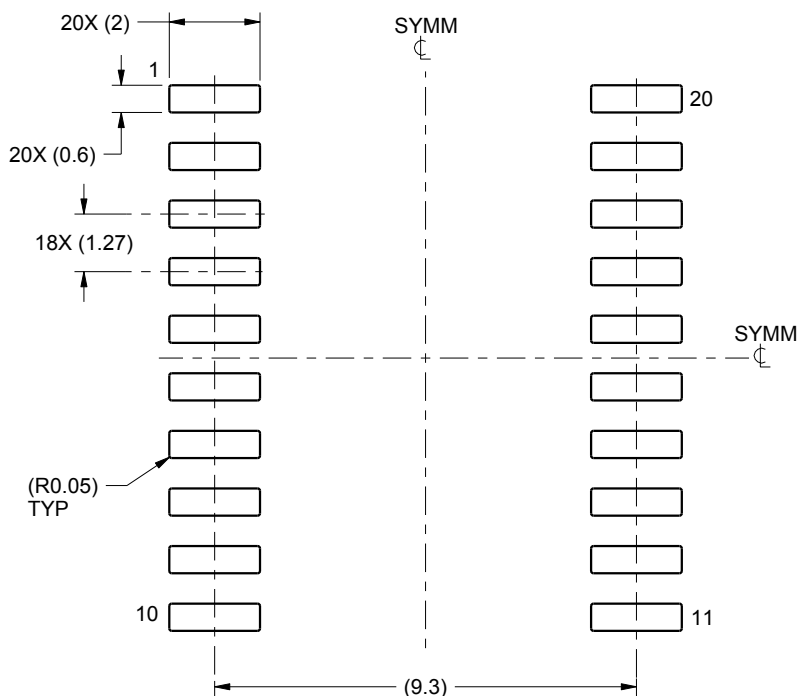
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

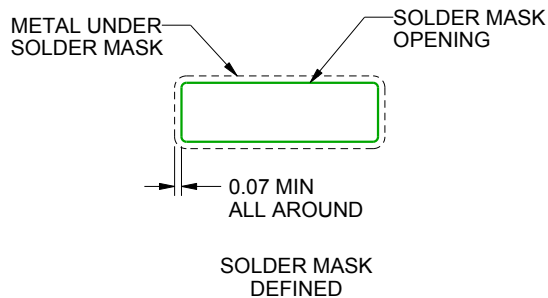
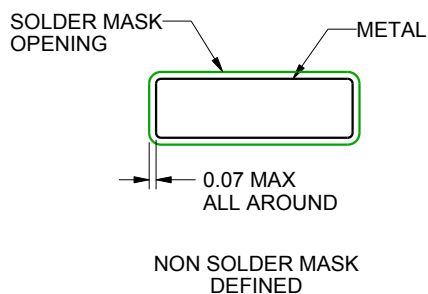
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月