SNx4AHC125 具有三态输出的四路总线缓冲门

1 特性

- 工作电压范围为 2V 至 5.5V
- 闩锁性能超过 250mA，符合 JESD 17 规范
- 四个独立输出使能引脚

2 应用

- 流量计
- 可编程逻辑控制器
- 以太网供电 (PoE)
- 电机驱动与控制
- 电子销售终端

3 说明

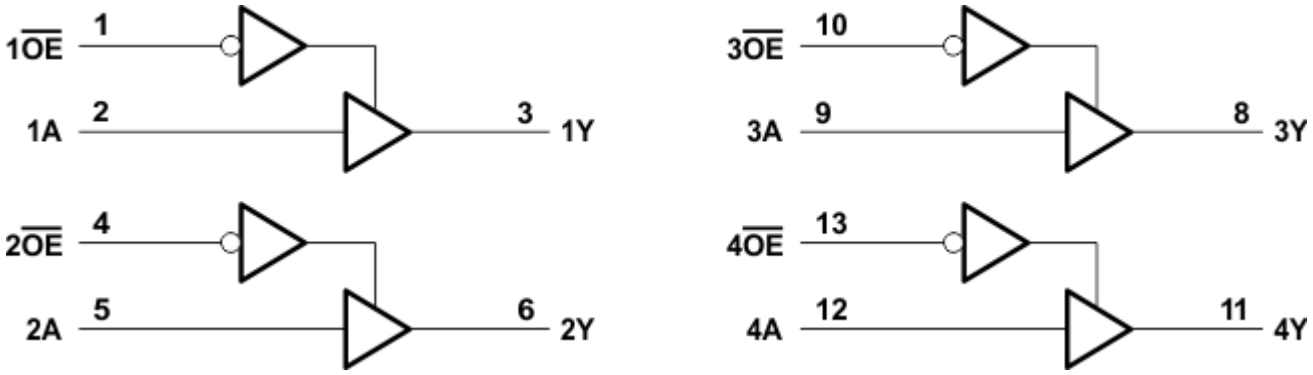
SNx4AHC125 器件是四路总线缓冲门，采用具有三态输出的独立线路驱动器。当每个输出的相关输出使能 ($\overline{OE}$) 输入为高电平时，输出被禁用。当 $\overline{OE}$ 为低电平时，相应的逻辑门会将来自 A 输入的数据传递到 Y 输出。

为了确保加电或断电期间的高阻抗状态，$\overline{OE}$ 必须通过一个上拉电阻器被连接至 V_{CC}；该电阻器的最小值由驱动器的电流灌入能力来决定。

器件信息

器件型号	封装(1)	封装尺寸(2)
SN54AHC125	J（CDIP，14）	8.89mm x 8.89mm
	W（CFP，14）	19.56mm × 6.67mm
	FK（LCCC，20）	9.21mm × 5.97mm
SN74AHC125	DB（SSOP，14）	6.20mm x 5.30mm
	D（SOIC，14）	8.65mm × 3.91mm
	NS（SO，14）	10.30mm × 5.30mm
	DGV（TVSOP，14）	3.60mm × 4.40mm
	PW（TSSOP，14）	5.00mm × 4.40mm
	N（PDIP，14）	19.30mm × 6.35mm
	RGY（VQFN，14）	3.50mm × 3.50mm
	BQA（WQFN，14）	3mm × 2.5mm

(1) 更多相关信息，请参阅第 11 节。
(2) 封装尺寸（长 × 宽）为标称值，不包括引脚。



所示引脚编号用于 D、DB、DGV、J、N、NS、PW、RGY 和 W 封装。

逻辑图（正逻辑）

内容

4 引脚配置和功能

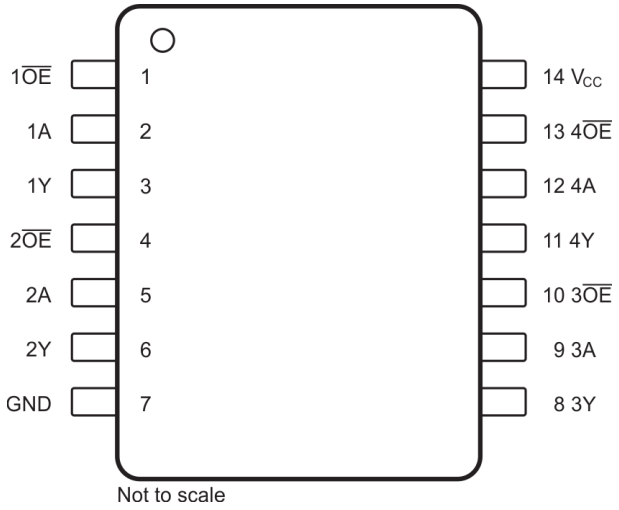


图 4-1. D、DB、DGV、N、NS、J、W 或 PW 封装 14 引脚 SOIC、SSOP、TVSOP、PDIP、SO、CDIP、CFP 或 TSSOP 顶视图

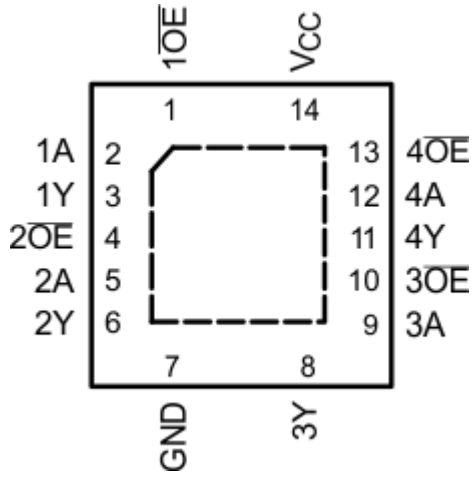


图 4-2. RGY 或 BQA 封装 14 引脚 VQFN 顶视图

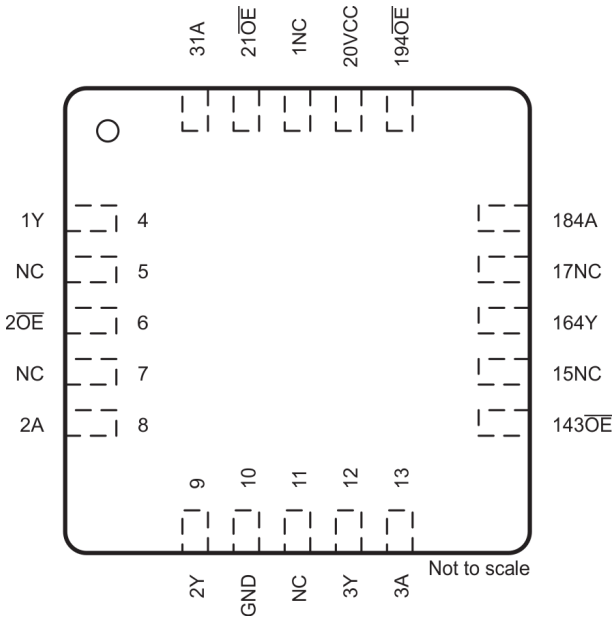


图 4-3. FK 封装 20 引脚 LCCC 顶视图

表 4-1. 引脚功能

引脚			I/O	说明
名称	SOIC、SSOP、TVSOP、PDIP、SO、CDIP、CFP、TSSOP、VQFN	LCCC		
1 $\overline{OE}$	1	2	I	栅极 1 的输出使能
1A	2	3	I	栅极 1 输入
1Y	3	4	O	栅极 1 输出
2 $\overline{OE}$	4	6	I	栅极 2 的输出使能
2A	5	8	I	栅极 2 输入
2Y	6	9	O	栅极 2 输出
3 $\overline{OE}$	10	14	I	栅极 3 的输出使能
3A	9	13	I	栅极 3 输入
3Y	8	12	O	栅极 3 输出
4 $\overline{OE}$	13	19	I	栅极 4 的输出使能
4A	12	18	I	栅极 4 输入
4Y	11	16	O	栅极 4 输出
GND	7	10	—	接地引脚
NC	—	1、5、7、11、15、17	—	无内部连接
V_{CC}	14	20	—	电源引脚

5 规格

5.1 绝对最大额定值

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

		最小值	最大值	单位
电源电压		-0.5	7	V
输入电压(2)		-0.5	7	V
输出电压(2)		-0.5	V_{CC}+0.5	V
输入钳位电流	V_I < 0		-20	mA
输出钳位电流	V_O < 0 或 V_O > V_{CC}		±20	mA
持续输出电流	V_O = 0 至 V_{CC}		±25	mA
通过 V_{CC} 或 GND 的持续电流			±50	mA
工作等效结温，T_J			150	°C
贮存温度，T_{stg}		-65	150	°C

(1) 超出*绝对最大额定值*下列出的压力可能会对器件造成永久损坏。这些仅仅是压力额定值，并不表示器件在这些条件下以及在*建议运行条件*以外的任何其他条件下能够正常运行。长时间处于绝对最大额定条件下可能会影响器件的可靠性。
(2) 如果遵守输入和输出电流额定值，输入和输出电压可超过额定值。

5.2 ESD 等级

			值	单位
$V_{(ESD)}$	静电放电	人体放电模型 (HBM)，符合 ANSI/ESDA/JEDEC JS-001 标准(1)	±1500	V
		充电器件模型 (CDM)，符合 JEDEC 规范 JESD22-C101(2)	±1000	

(1) JEDEC 文档 JEP155 指出：500V HBM 能够在标准 ESD 控制流程下安全生产。
(2) JEDEC 文档 JEP157 指出：250V CDM 能够在标准 ESD 控制流程下安全生产。

5.3 建议运行条件

在自然通风条件下的工作温度范围内测得（除非另有说明）

			最小值	最大值	单位
V_{CC}	电源电压		2	5.5	V
V_{IH}	高电平输入电压	V_{CC} = 2V	1.5		V
		V_{CC} = 3V	2.1		
		V_{CC} = 5.5V	3.85		
V_{IL}	低电平输入电压	V_{CC} = 2V		0.5	V
		V_{CC} = 3V		0.9	
		V_{CC} = 5.5V		1.65	
V_I	输入电压		0	5.5	V
V_O	输出电压		0	V_{CC}	V
I_{OH}	高电平输出电流	V_{CC} = 2V		-50	μA
		V_{CC} = 3.3V ± 0.3V		-4	mA
		V_{CC} = 5V ± 0.5V		-8	
I_{OL}	低电平输出电流	V_{CC} = 2V		50	μA
		V_{CC} = 3.3V ± 0.3V		4	mA
		V_{CC} = 5V ± 0.5V		8	
$\Delta t/\Delta v$	输入转换上升或下降速率	V_{CC} = 3.3V ± 0.3V		100	ns/V
		V_{CC} = 5V ± 0.5V		20	
T_A	自然通风条件下的工作温度范围		-40	125	°C

5.4 热性能信息

热指标(1)		SNx4AHC125								单位
		D (SOIC)	DB (SSOP)	NS (SO)	DGV (TVSOP)	PW (TSSOP)	N (PDIP)	RGY (VQFN)	BQA (WQFN)	
		14 引脚	14 引脚	14 引脚	14 引脚	14 引脚	14 引脚	14 引脚	14 引脚	
$R_{\theta JA}$	结至环境热阻	124.5	107.3	89.9	134.6	147.7	56.3	87.1	88.3	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	78.8	59.3	47.7	53.9	77.4	43.9	92.6	90.9	°C/W
$R_{\theta JB}$	结至电路板热阻	81	54.7	48.6	63.8	90.9	36.1	62.5	56.8	°C/W
ψ_{JT}	结至顶部特征参数	37	24	17.5	6.3	27.2	29.2	22.8	9.9	°C/W
ψ_{JB}	结至电路板特征参数	80.6	54.1	48.3	63.2	90.2	36	61.7	56.7	°C/W
$R_{\theta JC(bot)}$	结至外壳（底部）热阻	不适用	不适用	不适用	不适用	不适用	不适用	45.1	33.4	°C/W

(1) 有关新旧热指标的更多信息，请参阅*半导体和 IC 封装热指标*应用报告。

5.5 电气特性

在自然通风条件下的建议运行温度范围内测得（除非另有说明）

参数	测试条件			最小值	典型值	最大值	单位
V_{OH}	I_{OH} = -50μA	V_{CC} = 2V	T_A = 25°C	1.9	2		V
			T_A = –55°C 至 125°C (SN54AHC125)	1.9			
			T_A = –40°C 至 85°C (SN74AHC125)	1.9			
			T_A = –40°C 至 125°C（建议 SN74AHC125）	1.9			
		V_{CC} = 3V	T_A = 25°C	2.9	3		
			T_A = –55°C 至 125°C (SN54AHC125)	2.9			
			T_A = –40°C 至 85°C (SN74AHC125)	2.9			
			T_A = –40°C 至 125°C（建议 SN74AHC125）	2.9			
		V_{CC} = 4.5V	T_A = 25°C	4.4	4.5		
			T_A = –55°C 至 125°C (SN54AHC125)	4.4			
			T_A = –40°C 至 85°C (SN74AHC125)	4.4			
			T_A = –40°C 至 125°C（建议 SN74AHC125）	4.4			
	I_{OH} = –4mA 且 V_{CC} = 3V		T_A = 25°C	2.58			
			T_A = –55°C 至 125°C (SN54AHC125)	2.48			
			T_A = –40°C 至 85°C (SN74AHC125)	2.48			
			T_A = –40°C 至 125°C（建议 SN74AHC125）	2.48			
	I_{OH} = –8mA 且 V_{CC} = 4.5V		T_A = 25°C	3.94			
			T_A = –55°C 至 125°C (SN54AHC125)	3.8			
			T_A = –40°C 至 85°C (SN74AHC125)	3.8			
			T_A = –40°C 至 125°C（建议 SN74AHC125）	3.8			

5.5 电气特性（续）

在自然通风条件下的建议运行温度范围内测得（除非另有说明）

参数	测试条件			最小值	典型值	最大值	单位
V_{OL}	I_{OL} = 50μA	V_{CC} = 2V	T_A = 25°C			0.1	V
			T_A = –55°C 至 125°C (SN54AHC125)			0.1	
			T_A = –40°C 至 85°C (SN74AHC125)			0.1	
			T_A = –40°C 至 125°C（建议 SN74AHC125）			0.1	
		V_{CC} = 3V	T_A = 25°C			0.1	
			T_A = –55°C 至 125°C (SN54AHC125)			0.1	
			T_A = –40°C 至 85°C (SN74AHC125)			0.1	
			T_A = –40°C 至 125°C（建议 SN74AHC125）			0.1	
		V_{CC} = 4.5V	T_A = 25°C			0.1	
			T_A = –55°C 至 125°C (SN54AHC125)			0.1	
			T_A = –40°C 至 85°C (SN74AHC125)			0.1	
			T_A = –40°C 至 125°C（建议 SN74AHC125）			0.1	
	I_{OH} = 4mA 且 V_{CC} = 3V		T_A = 25°C			0.36	
			T_A = –55°C 至 125°C (SN54AHC125)			0.5	
			T_A = –40°C 至 85°C (SN74AHC125)			0.44	
			T_A = –40°C 至 125°C（建议 SN74AHC125）			0.5	
	I_{OH} = 8mA 且 V_{CC} = 4.5V		T_A = 25°C			0.36	
			T_A = –55°C 至 125°C (SN54AHC125)			0.5	
			T_A = –40°C 至 85°C (SN74AHC125)			0.44	
			T_A = –40°C 至 125°C（建议 SN74AHC125）			0.5	
I_I	V_I = 5.5V 或 GND 并且 V_{CC} = 0V 至 5.5V		T_A = 25°C			±0.1	μA
			T_A = –55°C 至 125°C (SN54AHC125)			±1(1)	
			T_A = –40°C 至 85°C (SN74AHC125)			±1	
			T_A = –40°C 至 125°C（建议 SN74AHC125）			±1	
I_{OZ}	V_O = V_{CC} 或 GND 且 V_{CC} = 5.5V		T_A = 25°C			±0.25	μA
			T_A = –55°C 至 125°C (SN54AHC125)			±2.5	
			T_A = –40°C 至 85°C (SN74AHC125)			±2.5	
			T_A = –40°C 至 125°C（建议 SN74AHC125）			±2.5	
I_{CC}	V_I = V_{CC} 或 GND，I_O = 0，V_{CC} = 5.5V		T_A = 25°C			4	μA
			T_A = –55°C 至 125°C (SN54AHC125)			40	
			T_A = –40°C 至 85°C (SN74AHC125)			40	
			T_A = –40°C 至 125°C（建议 SN74AHC125）			40	
C_i	V_I = V_{CC} 或 GND 且 V_{CC} = 5V		T_A = 25°C		4	10	pF
			T_A = –40°C 至 85°C (SN74AHC125)			10	

(1) 对于符合 MIL-PRF-38535 标准的产品，此参数未经量产测试（在 V_{CC} = 0V 时）。

5.6 开关特性，V_{CC} = 3.3V ± 0.3V

在推荐的自然通风条件下的工作温度范围内，并且 V_{CC} = 3.3V ± 0.3V（除非另有说明；请参阅负载电路和电压波形）

参数	从（输入）	到（输出）	测试条件		最小值	典型值	最大值	单位
t_{PHL}，t_{PLH}	A	Y	C_L = 15pF	T_A = 25°C		5.6(1)	8(1)	ns
				T_A = –55°C 至 125°C (SN54AHC125)	1(1)		9.5(1)	
				T_A = –40°C 至 85°C (SN74AHC125)	1		9.5	
				T_A = –40°C 至 125°C（建议 SN74AHC125）	1		9.5	
t_{PZL}、t_{PZH}	$\overline{OE}$	Y	C_L = 15pF	T_A = 25°C		5.4(1)	8(1)	ns
				T_A = –55°C 至 125°C (SN54AHC125)	1(1)		9.5(1)	
				T_A = –40°C 至 85°C (SN74AHC125)			9.5	
				T_A = –40°C 至 125°C（建议 SN74AHC125）			9.5	
t_{PLZ}、t_{PHZ}	$\overline{OE}$	Y	C_L = 15pF	T_A = 25°C		7.0(1)	9.7(1)	ns
				T_A = –55°C 至 125°C (SN54AHC125)	1(1)		11.5(1)	
				T_A = –40°C 至 85°C (SN74AHC125)	1(1)		11.5(1)	
				T_A = –40°C 至 125°C（建议 SN74AHC125）	1(1)		11.5(1)	
t_{PHL}，t_{PLH}	A	Y	C_L = 50pF	T_A = 25°C		8.1	11.5	ns
				T_A = –55°C 至 125°C (SN54AHC125)	1		13	
				T_A = –40°C 至 85°C (SN74AHC125)	1		13	
				T_A = –40°C 至 125°C（建议 SN74AHC125）	1		13	
t_{PZL}、t_{PZH}	$\overline{OE}$	Y	C_L = 50pF	T_A = 25°C		7.9	11.5	ns
				T_A = –55°C 至 125°C (SN54AHC125)	1		13	
				T_A = –40°C 至 85°C (SN74AHC125)	1		13	
				T_A = –40°C 至 125°C（建议 SN74AHC125）	1		13	
t_{PLZ}、t_{PHZ}	$\overline{OE}$	Y	C_L = 50pF	T_A = 25°C		9.5	13.2	ns
				T_A = –55°C 至 125°C (SN54AHC125)	1		15	
				T_A = –40°C 至 85°C (SN74AHC125)	1		15	
				T_A = –40°C 至 125°C（建议 SN74AHC125）	1		15	
tsk(o)	$\overline{OE}$	Y	C_L = 50pF	T_A = 25°C			1.5(2)	ns
				T_A = –40°C 至 85°C (SN74AHC125)			1.5	

(1) 对于符合 MIL-PRF-38535 标准的产品，此参数未经量产测试。
(2) 对于符合 MIL-PRF-38535 标准的产品，此参数不适用。

5.7 开关特性，V_{CC} = 5V ± 0.5V

在推荐的自然通风条件下的工作温度范围内，并且 V_{CC} = 5V ± 0.5V（除非另有说明；请参阅负载电路和电压波形）

参数	从（输入）	到（输出）	测试条件		最小值	典型值	最大值	单位
t_{PLH}、t_{PHL}	A	Y	C_L = 15pF	T_A = 25°C		3.8(1)	5.5(1)	ns
				T_A = –55°C 至 125°C (SN54AHC125)	1(1)		6.5(1)	
				T_A = –40°C 至 85°C (SN74AHC125)	1		6.5	
				T_A = –40°C 至 125°C（建议 SN74AHC125）	1		6.5	
t_{PZH}，t_{PZL}	$\overline{OE}$	Y	C_L = 15pF	T_A = 25°C		3.6(1)	5.1(1)	ns
				T_A = –55°C 至 125°C (SN54AHC125)	1(1)		6(1)	
				T_A = –40°C 至 85°C (SN74AHC125)	1		6	
				T_A = –40°C 至 125°C（建议 SN74AHC125）	1		6	
t_{PHZ}，t_{PLZ}	$\overline{OE}$	Y	C_L = 15pF	T_A = 25°C		4.6(1)	6.8(1)	ns
				T_A = –55°C 至 125°C (SN54AHC125)	1(1)		8(1)	
				T_A = –40°C 至 85°C (SN74AHC125)	1(1)		8(1)	
				T_A = –40°C 至 125°C（建议 SN74AHC125）	1(1)		8(1)	
t_{PLH}、t_{PHL}	A	Y	C_L = 50pF	T_A = 25°C		5.3	7.5	ns
				T_A = –55°C 至 125°C (SN54AHC125)	1		8.5	
				T_A = –40°C 至 85°C (SN74AHC125)	1		8.5	
				T_A = –40°C 至 125°C（建议 SN74AHC125）	1		8.5	
t_{PZH}，t_{PZL}	$\overline{OE}$	Y	C_L = 50pF	T_A = 25°C		5.1	7.1	ns
				T_A = –55°C 至 125°C (SN54AHC125)	1		8	
				T_A = –40°C 至 85°C (SN74AHC125)	1		8	
				T_A = –40°C 至 125°C（建议 SN74AHC125）	1		8	
t_{PHZ}，t_{PLZ}	$\overline{OE}$	Y	C_L = 50pF	T_A = 25°C		6.1	8.8	ns
				T_A = –55°C 至 125°C (SN54AHC125)	1		10	
				T_A = –40°C 至 85°C (SN74AHC125)	1		10	
				T_A = –40°C 至 125°C（建议 SN74AHC125）	1		10	
tsk(o)	$\overline{OE}$	Y	C_L = 50pF	T_A = 25°C			1(2)	ns
				T_A = –40°C 至 85°C (SN74AHC125)			1	

5.8 噪声特性

V_{CC} = 5V，C_L = 50pF 且 T_A = 25°C(1)

参数		最小值	最大值	单位
$V_{OL(P)}$	安静输出，最大动态 (V_{OL})		0.8	V
$V_{OL(V)}$	安静输出，最小动态 (V_{OL})		-0.8	V
$V_{OH(V)}$	安静输出，最小动态 (V_{OH})	4.4		V
$V_{IH(D)}$	高电平动态输入电压	3.5		V
$V_{IL(D)}$	低电平动态输入电压		1.5	V

(1) 特性仅适用于表面贴装封装。

5.9 工作特性

V_{CC} = 5V 且 T_A = 25°C

参数		测试条件	典型值	单位
C_{pd}	功率耗散电容	空载且 f = 1MHz	9.5	pF

5.10 典型特性

图 5-1 显示了 V_{CC} 为 5V ± 0.5V 且 T_A = 25°C 时，不断变化的 V_{IN} 值所对应的 I_{CC}。

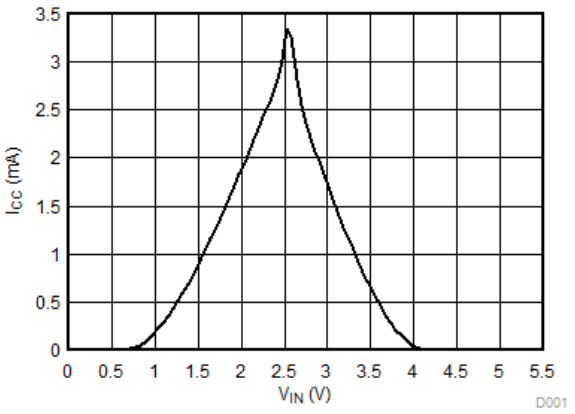
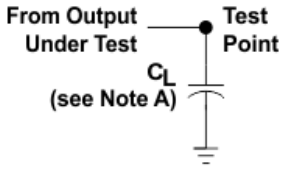
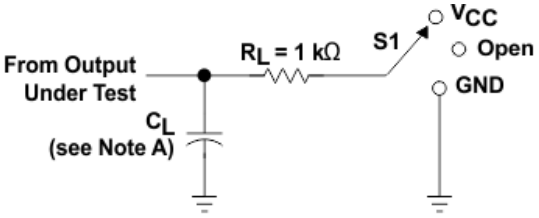


图 5-1. V_{IN} 与 I_{CC} 间的关系

6 参数测量信息

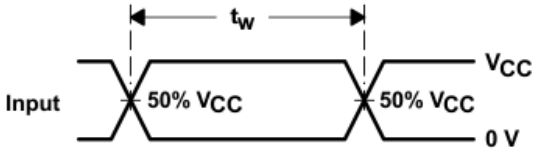


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

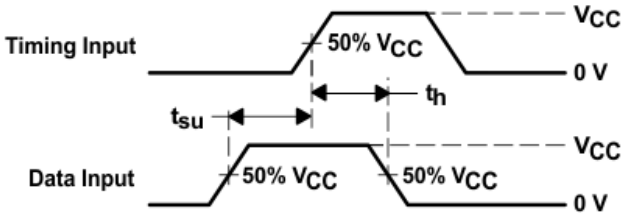


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

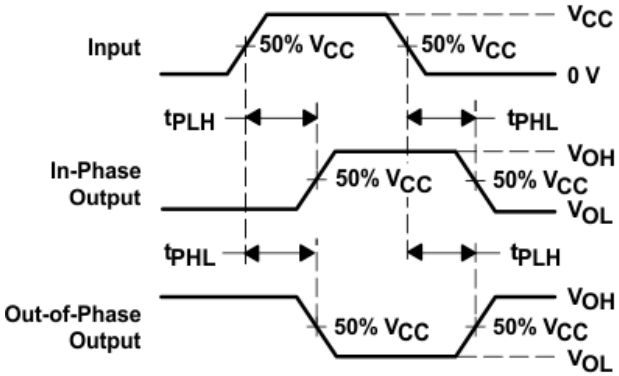
TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	VCC
tPHZ/tPZH	GND
Open Drain	VCC



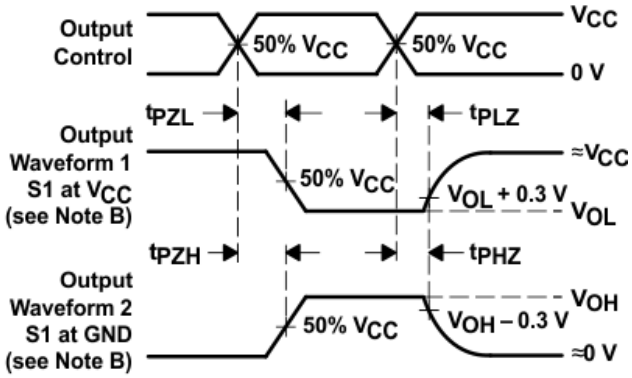
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

A. C_L 包括探头和夹具电容。

B. 波形 1 用于具有内部条件的输出，使得输出为低电平，除非被输出控制禁用。波形 2 用于具有内部条件的输出，使得输出为高电平，除非被输出控制禁用。

C. 所有输入脉冲均由具有以下特性的发生器提供：PRR ≤ 1MHz，Z_O = 50 Ω，t_r ≤ 3 ns，t_f ≤ 3 ns。

D. 一次测量一个输出，每次测量一个输入转换。

E. 并非所有参数和波形都适用于所有器件。

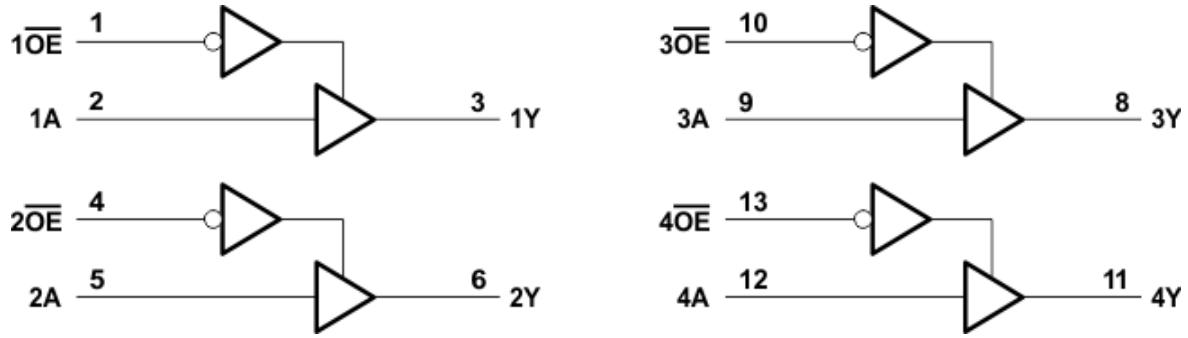
图 6-1. 负载电路和电压波形

7 详细说明

7.1 概述

SNx4AHC125 器件具有四个集成总线缓冲器门。每个门都可以通过各自的输出使能引脚单独控制，或者连接在一起同时控制。这允许从一个器件控制多达四条不同的线路。通常，微控制器对单个引脚提供多个功能选项。通过使用 GPIO 引脚启用特定缓冲器，SNx4AHC125 可以充当多路复用器，根据微控制器上选择的引脚功能来选择特定数据线。同时，未选择的线路将与引脚隔离。

7.2 功能方框图



所示引脚编号用于 D、DB、DGV、J、N、NS、PW、RGY 和 W 封装。

7.3 特性说明

每个缓冲器都有自己的输出使能。这允许单独控制每个缓冲器。当输出使能为低电平时，输入被传递到输出。当输出使能为高电平时，输出为高阻抗。此功能在可能需要隔离的应用中非常有用。

7.4 器件功能模式

表 7-1 列出了 SNx4AHC125 器件的功能模式。

表 7-1. 功能表
（每个缓冲器）

输入		输出
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

8 应用和实施

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 应用信息

SNx4AHC125 器件具有宽工作电压范围，可用于各种应用中。除宽工作电压范围外，这款器件与同类器件的不同之处在于它们具有可通过其独立输出使能 ($\overline{OE}$) 引脚单独控制的四个缓冲器。每个缓冲器可以处于启用状态并将数据从 A 传递到 Y，也可以禁用并设置为高阻抗状态。

8.2 典型应用

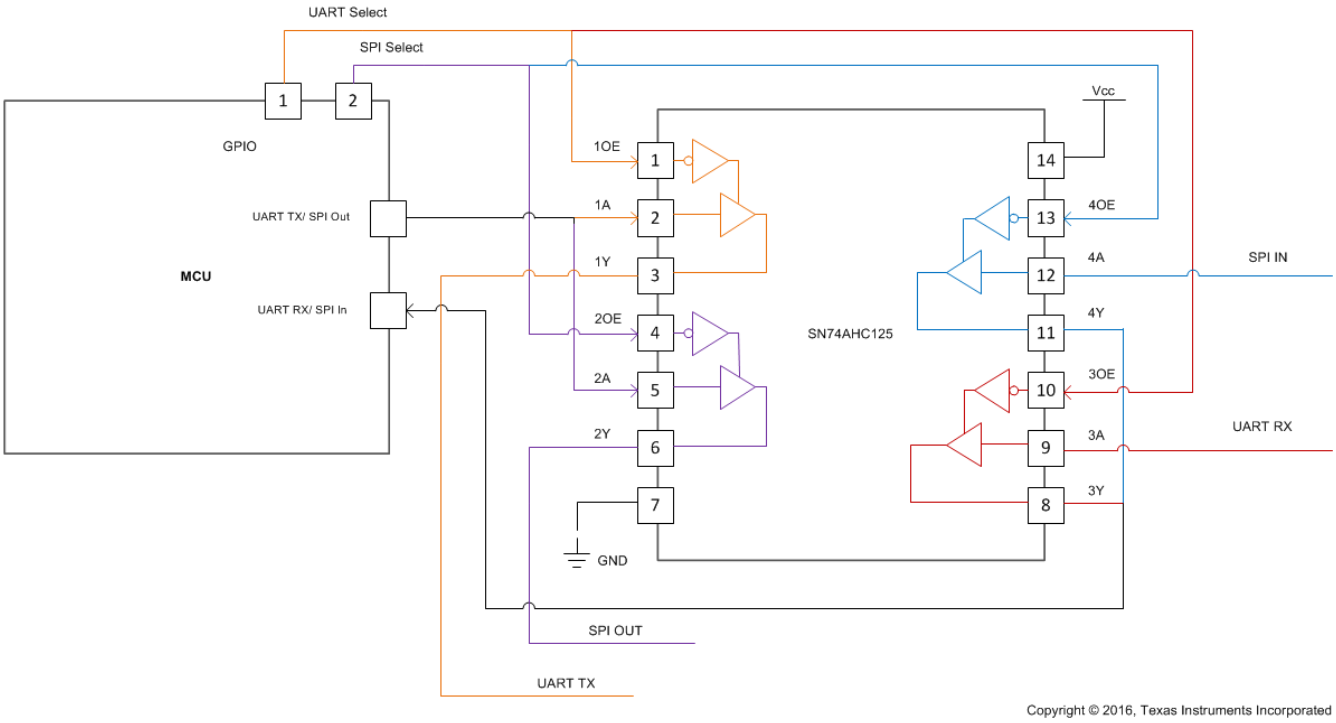


图 8-1. 数字多路复用器

8.2.1 设计要求

最好将 SN74AHC125 的 V_{CC} 设置为与微控制器逻辑电平相同的电平，以便实现出色的性能。SN74AHC125 可以安全地处理 –0.5V 至 7V 的输入电平。不过，如果接收到的逻辑电平与器件的 V_{CC} 电平不同，则可能会发生错误。例如，如果 V_{CC} 为 5.5V，则最低高电平输入电压 (V_{IH}) 电平为 3.85V。这意味着，如果微控制器正在发送高电平信号，但高电平 = 3.3V，则该电平对于 SNx4AHC125 来说太低而无法将其寄存为所需的值。在这种情况下，为降低 V_{IH} 的最小值，必须降低 V_{CC} 的值。对于低电平输入电压 (V_{IL})，可采取相反的操作。如果 VCC 设置为 2V，则 V_{IL} 最大值为 0.5V。根据微控制器逻辑电平，低电平信号可能不会低至 SNx4AHC125 无法对其进行寄存的水平。

8.2.2 详细设计过程

1. 建议的输入条件：
   - 有关不同 V_{CC} 下的 V_{IH} 和 V_{IL} 电平，请参阅*建议运行条件*。
   - 请注意输出使能引脚的上升时间和下降时间规格，确保及时启用正确的缓冲器并禁用其他缓冲器。这样可以更大限度地减少对微控制器引脚和外部电路的干扰。有关更多详细信息，请参阅*开关特性，V_{CC} = 3.3V ± 0.3V* 和 *开关特性，V_{CC} = 5V ± 0.5V* 表。
2. 建议的输出条件：
   - 每路输出的负载电流不能超过 I_O 最大值，且不能超过该器件的总电流（通过 V_{CC} 或 GND 的持续电流）。这些限值位于*绝对最大额定值*中。
   - 输出不应被拉至高于 V_{CC}。

8.2.3 应用曲线

典型器件 (25°C)

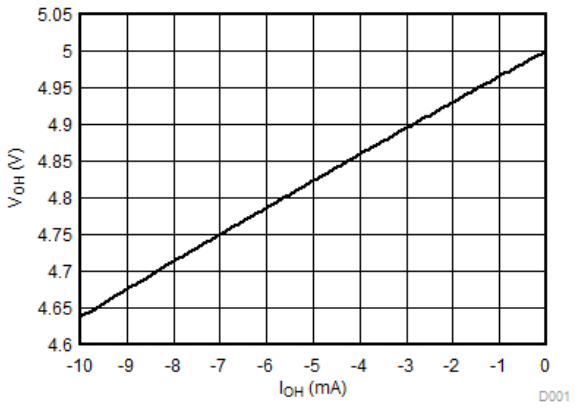


图 8-2. I_{OH} 与 V_{OH} 间的关系

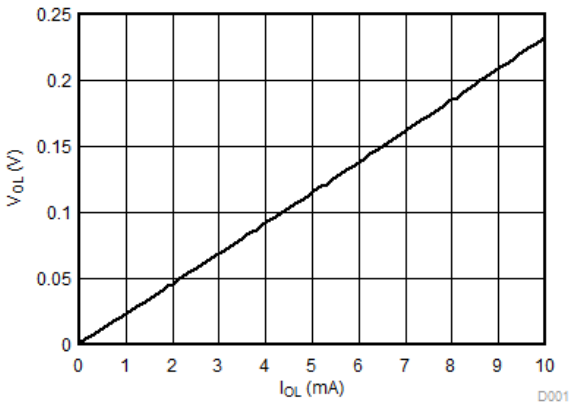


图 8-3. I_{OL} 与 V_{OL} 间的关系

8.3 电源相关建议

电源可以是*建议运行条件*中最小和最大电源电压额定值之间的任何电压。

每个 V_{CC} 引脚必须具有一个良好的旁路电容器，以防止功率干扰。对于单电源器件，建议使用 0.1μF 电容器；如果有多个 V_{CC} 引脚，则建议为每个电源引脚使用 0.01μF 或 0.022μF 电容器。可以并联多个旁路电容器以抑制不同的噪声频率。0.1μF 和 1μF 电容器通常并联使用。为了获得更佳效果，旁路电容器必须尽可能靠近电源引脚安装。

8.4 布局

8.4.1 布局指南

当使用多位逻辑器件时，输入决不能悬空。在许多情况下，未使用数字逻辑器件的功能或部分功能；例如，当仅使用三输入与门的两个输入或仅使用 4 个缓冲门中的 3 个时。此类输入引脚不得悬空，因为外部连接处的未定义电压会导致未定义的运行状态。以下指定了在所有情况下都必须遵守的规则。数字逻辑器件的所有未使用输入必须连接至一个高或低偏置以防止悬空。必须应用于任何特定未使用输入的逻辑电平取决于器件的功能。通常，它们会连接到 GND 或 V_{CC}（具体取决于哪种更合理或更方便）。

8.4.1.1 布局示例

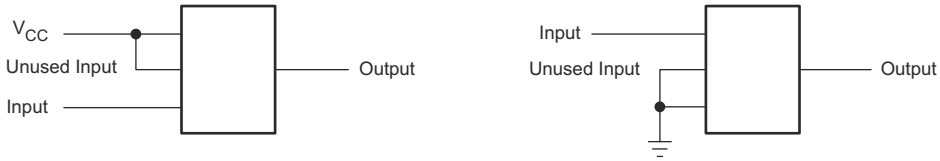


图 8-4. 布局图

9 器件和文档支持

9.1 文档支持（模拟）

9.1.1 相关文档

请参阅以下相关文档：

慢速或浮点 CMOS 输入的影响 (SCBA004)

9.1.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 9-1. 相关链接

器件	产品文件夹	样片 & 购买	技术文档	工具 & 软件	支持 & 社区
SN54AHC125	点击此处	点击此处	点击此处	点击此处	点击此处
SN74AHC125	点击此处	点击此处	点击此处	点击此处	点击此处

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.4 商标

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision N (October 2023) to Revision O (February 2024)	Page
• 将 RGY 封装的热性能值 RθJA 从 55.1 更新为 87.1，将 RθJC(top) 从 52.3 更新为 92.6，将 RθJB 从 49.4 更新为 30.9，将 ΨJT 从 14.6 更新为 2.4，将 ΨJB 从 31 更新为 61.7，将 RθJC(bot) 从 12.7 更新为 45.1，所有值均以 °C/W 为单位	6

Changes from Revision M (June 2023) to Revision N (October 2023) **Page**

- 更新了 D 和 PW 封装的 R θ JC(top)、R θ JB、Ψ JT、Ψ JB 和 R θ JC(bot)，所有值均以 °C/W 为单位.....6

11 机械、封装和可订购信息

下述页面包含机械、封装和订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9686801Q2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9686801Q2A SNJ54AHC 125FK	Samples
5962-9686801QCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9686801QCA SNJ54AHC125J	Samples
5962-9686801QDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9686801QDA SNJ54AHC125W	Samples
SN74AHC125BQAR	ACTIVE	WQFN	BQA	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC125	Samples
SN74AHC125D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 125	AHC125	
SN74AHC125DBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA125	Samples
SN74AHC125DGVR	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA125	Samples
SN74AHC125DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC125	Samples
SN74AHC125N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHC125N	Samples
SN74AHC125NE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHC125N	Samples
SN74AHC125NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC125	Samples
SN74AHC125PW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 125	HA125	
SN74AHC125PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	HA125	Samples
SN74AHC125RGYR	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HA125	Samples
SNJ54AHC125FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9686801Q2A SNJ54AHC 125FK	Samples
SNJ54AHC125J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9686801QCA SNJ54AHC125J	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54AHC125W	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9686801QDA SNJ54AHC125W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN54AHC125, SN74AHC125 :

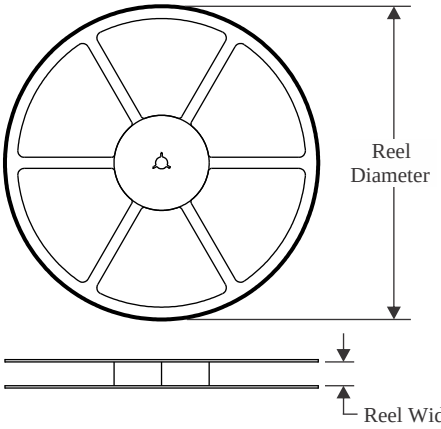
- Catalog : SN74AHC125
- Automotive : SN74AHC125-Q1, SN74AHC125-Q1
- Enhanced Product : SN74AHC125-EP, SN74AHC125-EP
- Military : SN54AHC125

NOTE: Qualified Version Definitions:

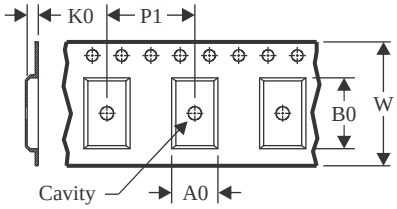
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

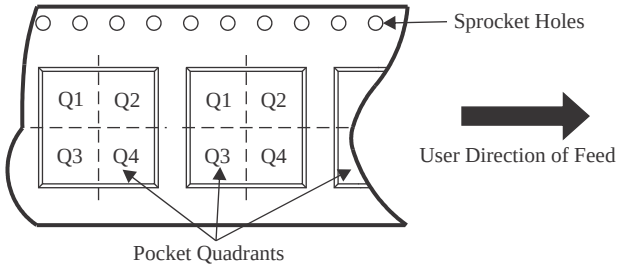


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

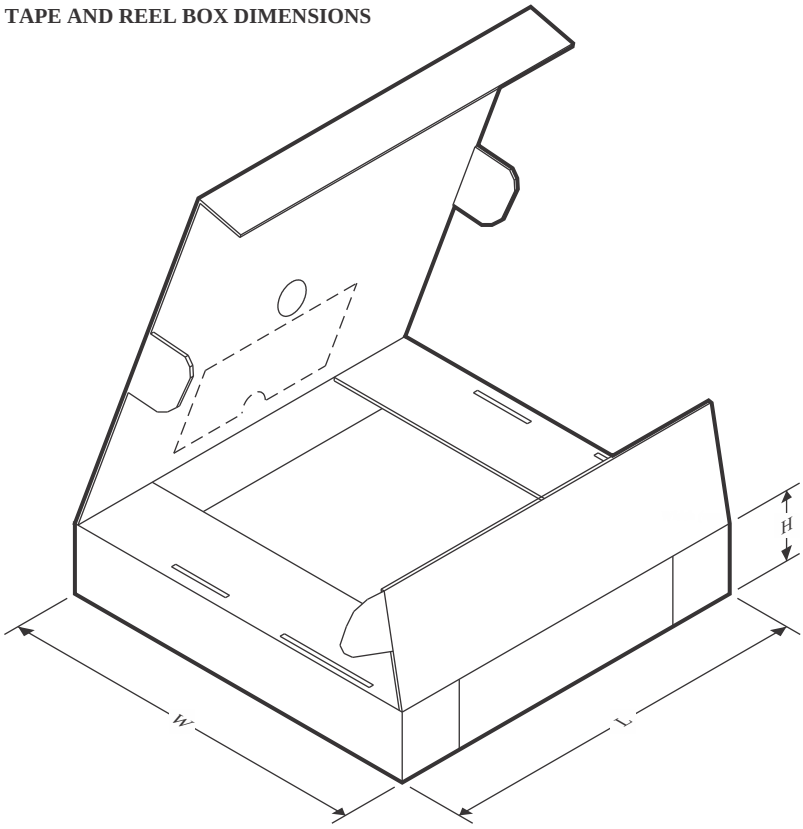
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC125BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74AHC125DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHC125DGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHC125DR	SOIC	D	14	2500	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
SN74AHC125DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC125DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC125DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74AHC125NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AHC125PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC125PWR	TSSOP	PW	14	2000	330.0	12.4	6.85	5.45	1.6	8.0	12.0	Q1
SN74AHC125PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC125RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

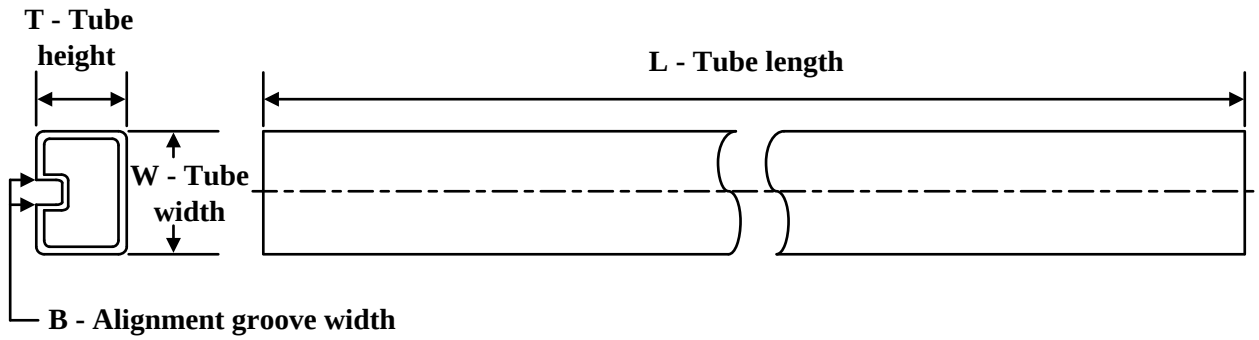
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC125BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74AHC125DBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74AHC125DGVR	TVSOP	DGV	14	2000	356.0	356.0	35.0
SN74AHC125DR	SOIC	D	14	2500	340.5	336.1	32.0
SN74AHC125DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74AHC125DR	SOIC	D	14	2500	333.2	345.9	28.6
SN74AHC125DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74AHC125NSR	SO	NS	14	2000	356.0	356.0	35.0
SN74AHC125PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74AHC125PWR	TSSOP	PW	14	2000	366.0	364.0	50.0
SN74AHC125PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74AHC125RGYR	VQFN	RGY	14	3000	356.0	356.0	35.0

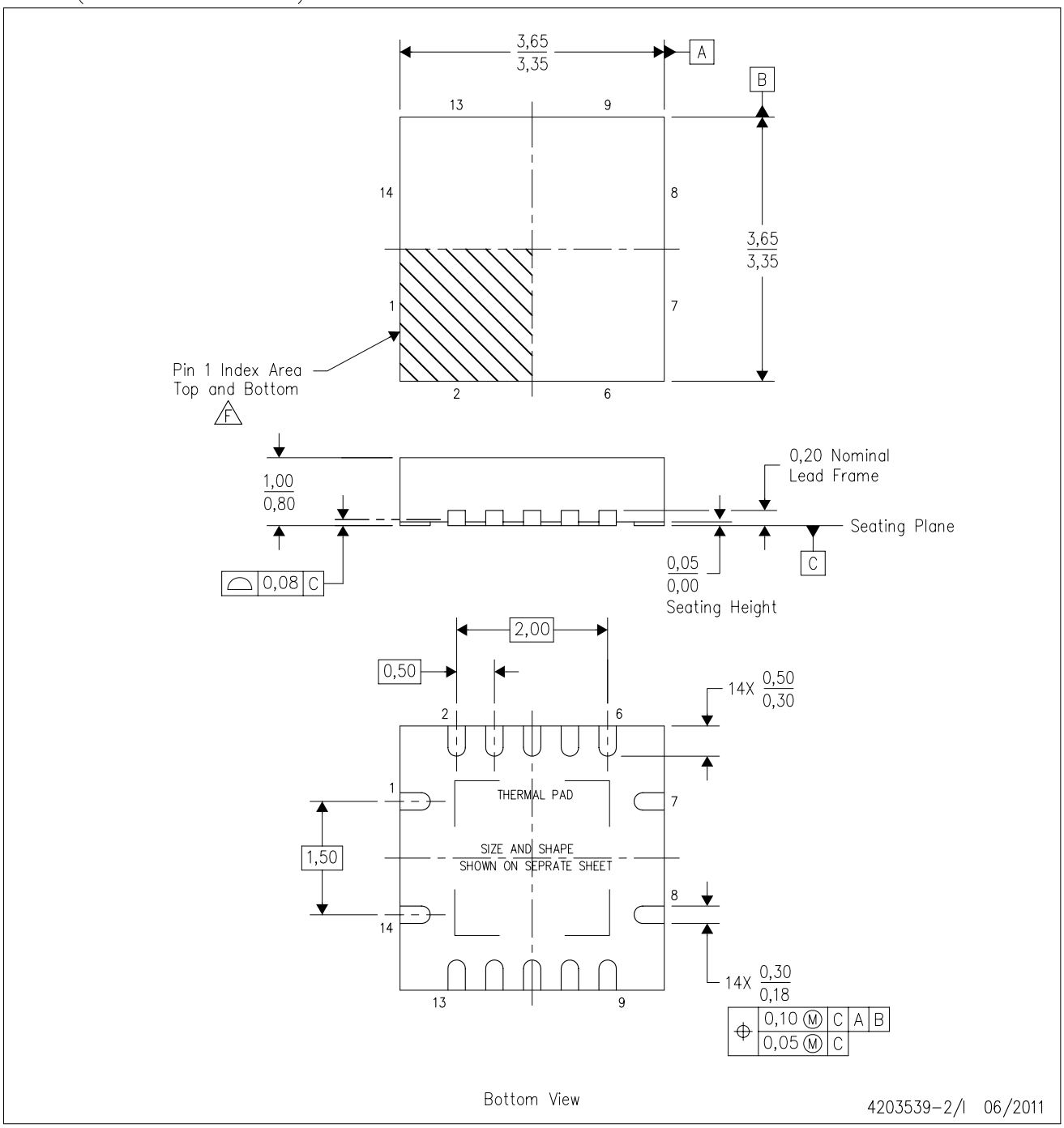
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9686801Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9686801QDA	W	CFP	14	25	506.98	26.16	6220	NA
SN74AHC125N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC125N	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC125NE4	N	PDIP	14	25	506	13.97	11230	4.32
SN74AHC125NE4	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54AHC125FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHC125W	W	CFP	14	25	506.98	26.16	6220	NA

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

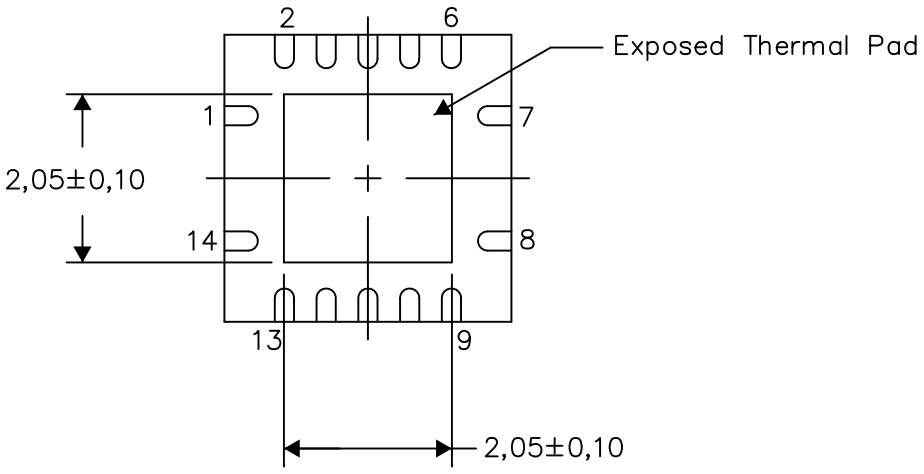
RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



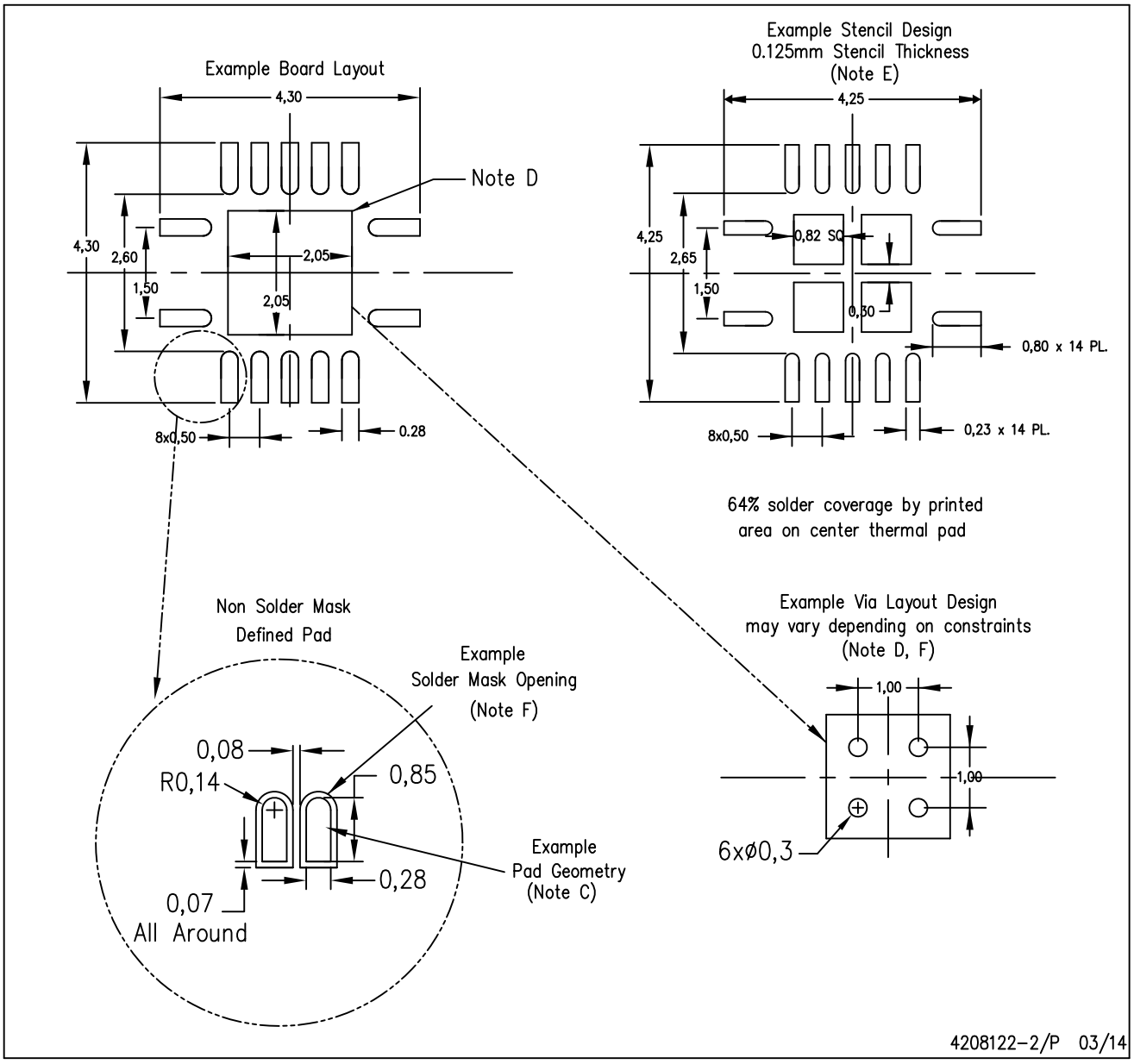
Bottom View

Exposed Thermal Pad Dimensions

4206353–2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

GENERIC PACKAGE VIEW

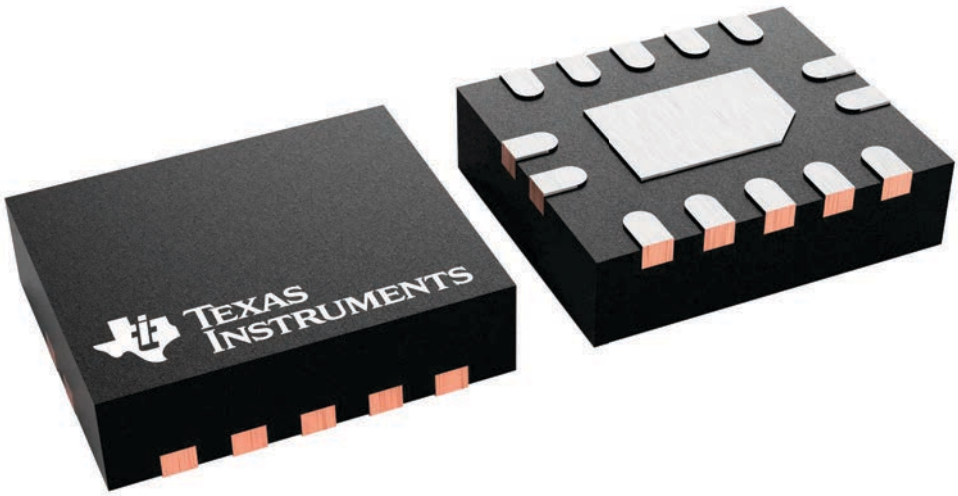
BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

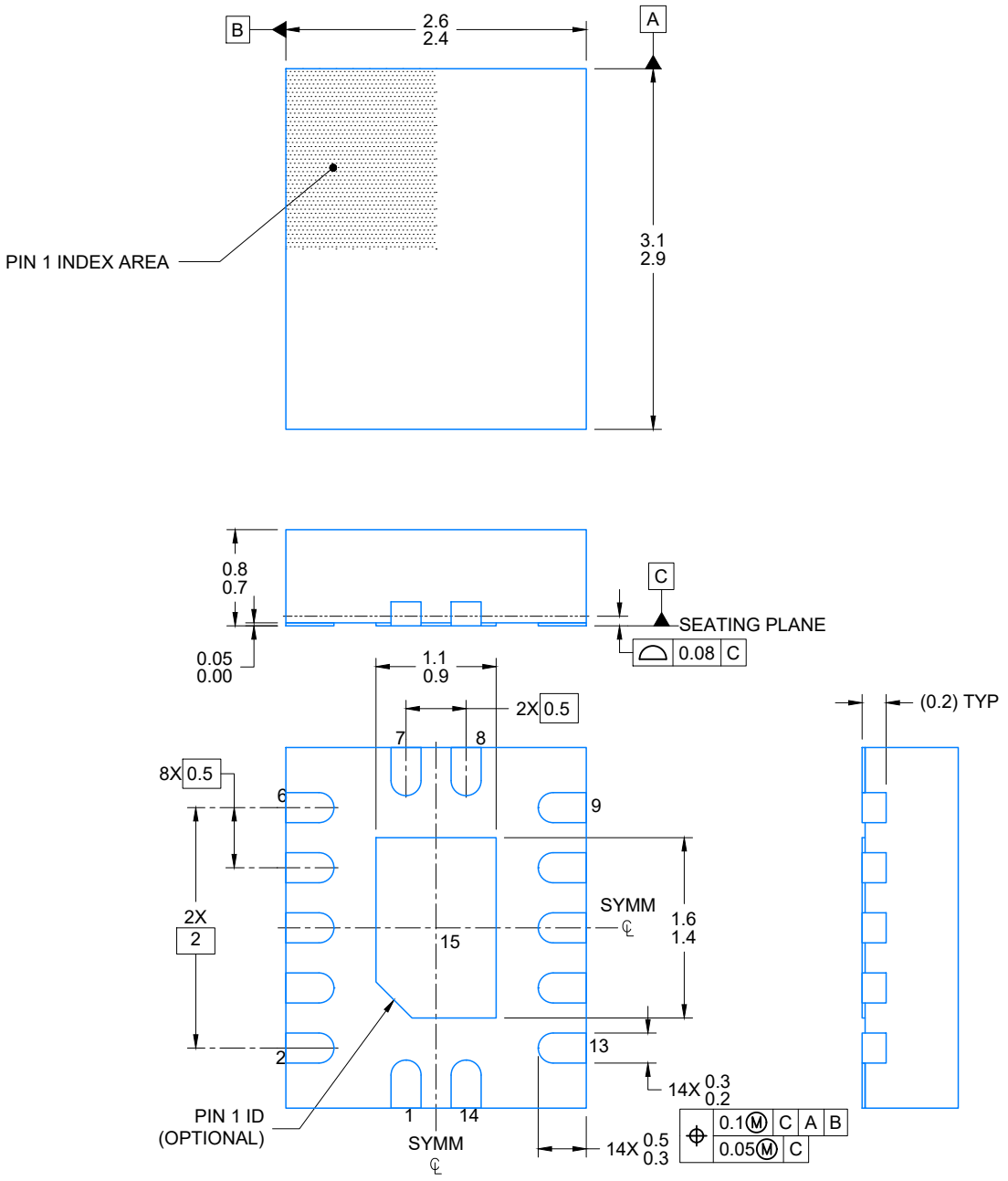


PACKAGE OUTLINE

BQA0014A

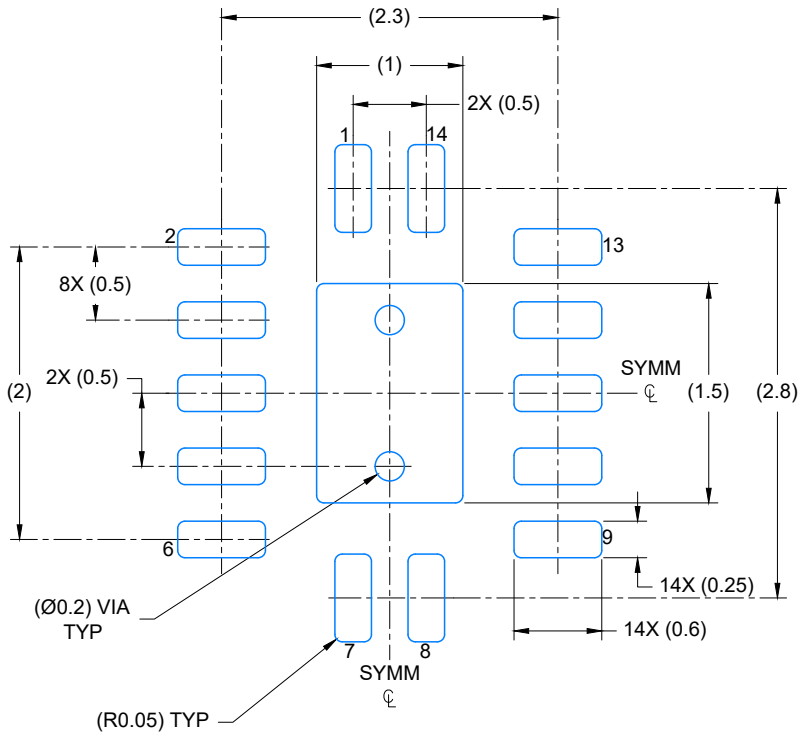
WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

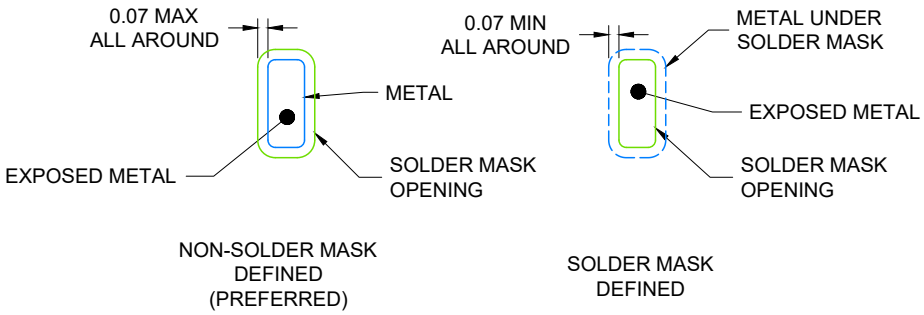


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



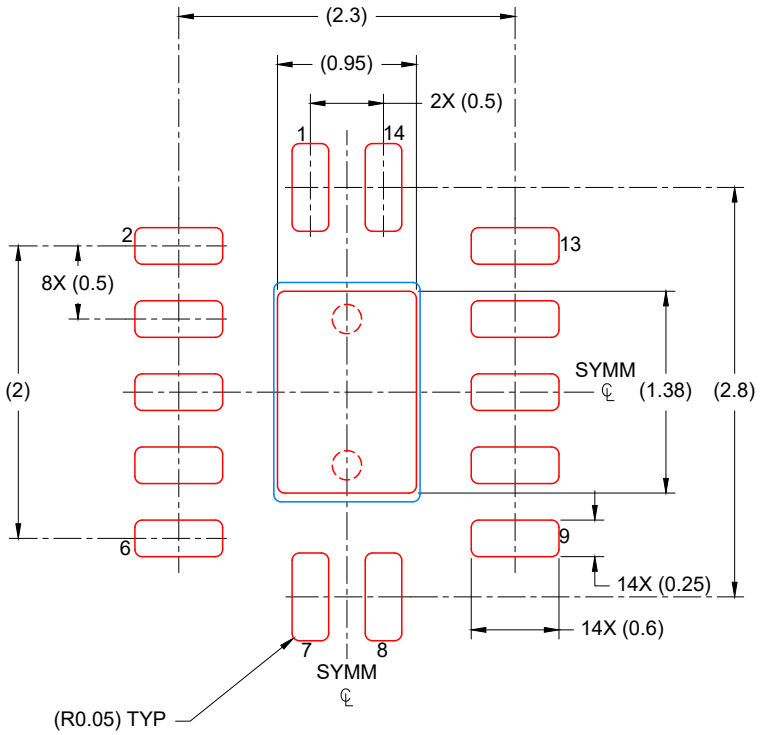
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

4224636/A 11/2018

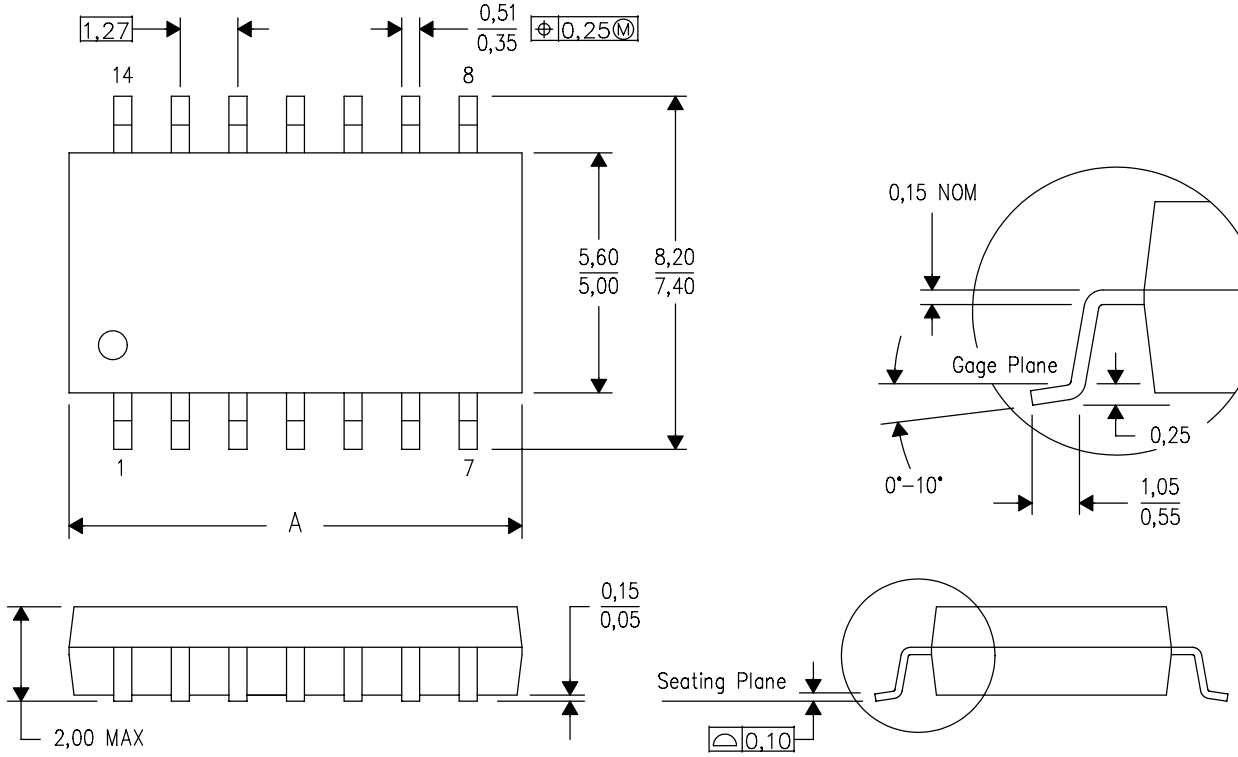
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

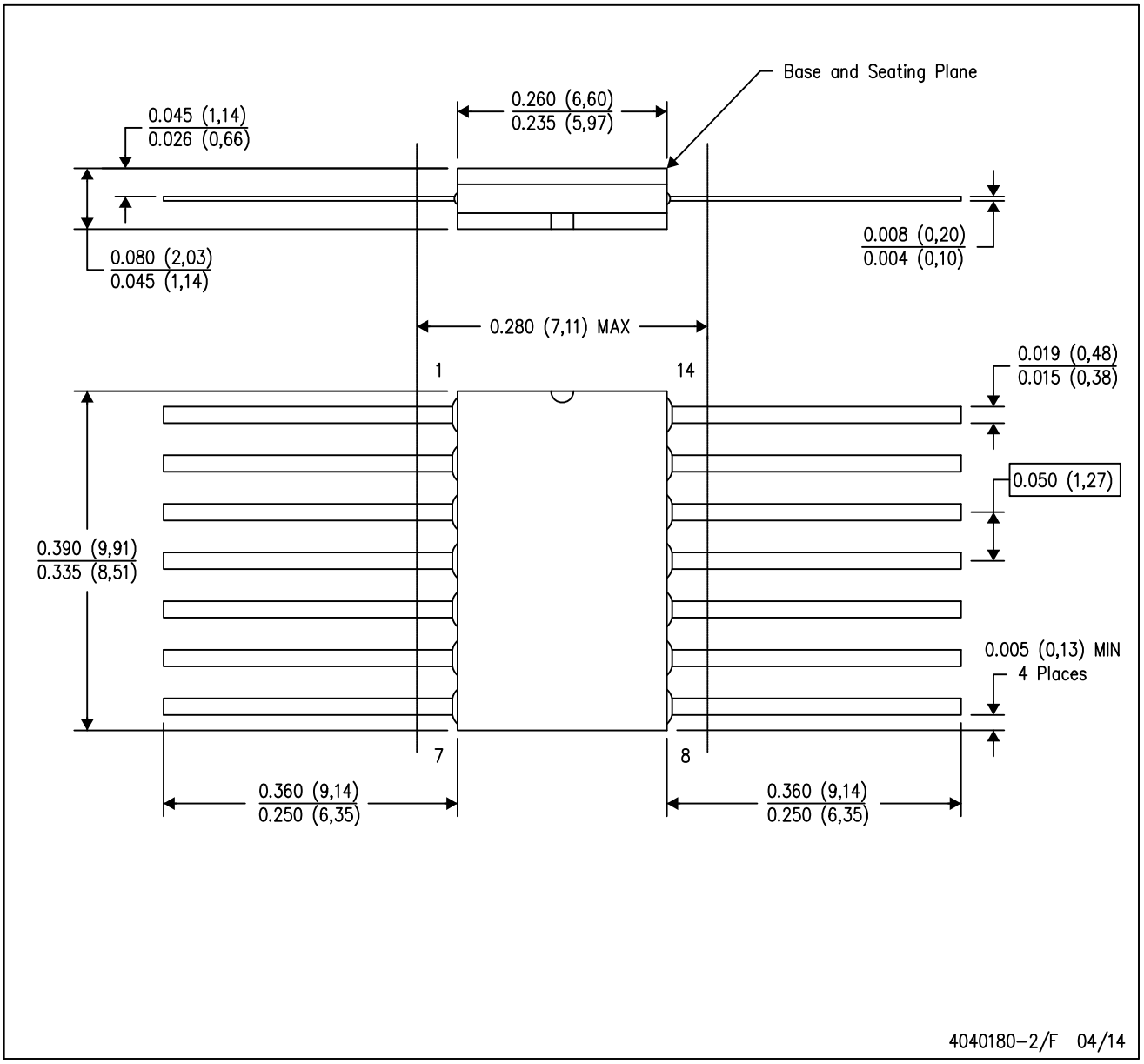


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

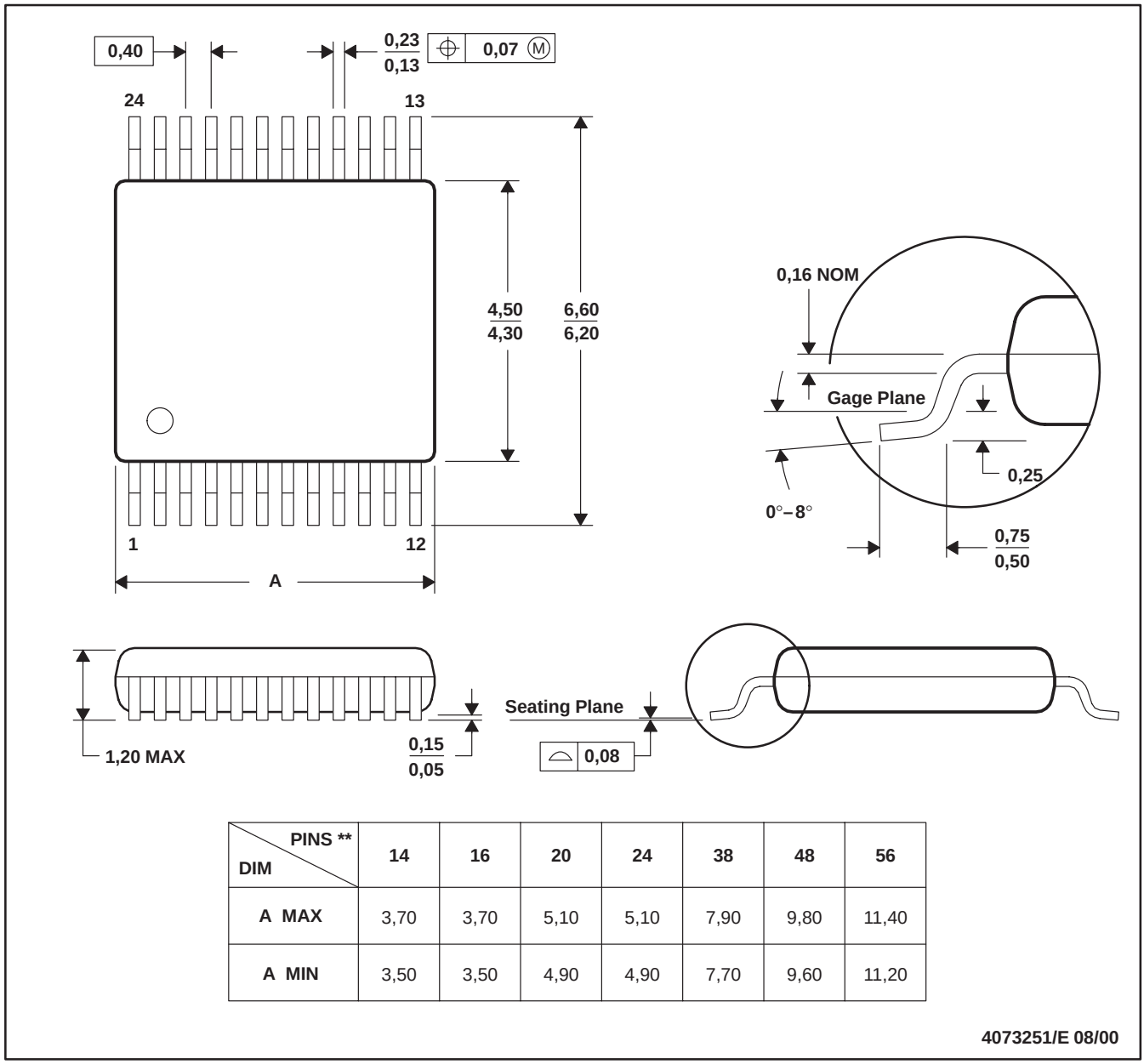
W (R–GDFP–F14) CERAMIC DUAL FLATPACK



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

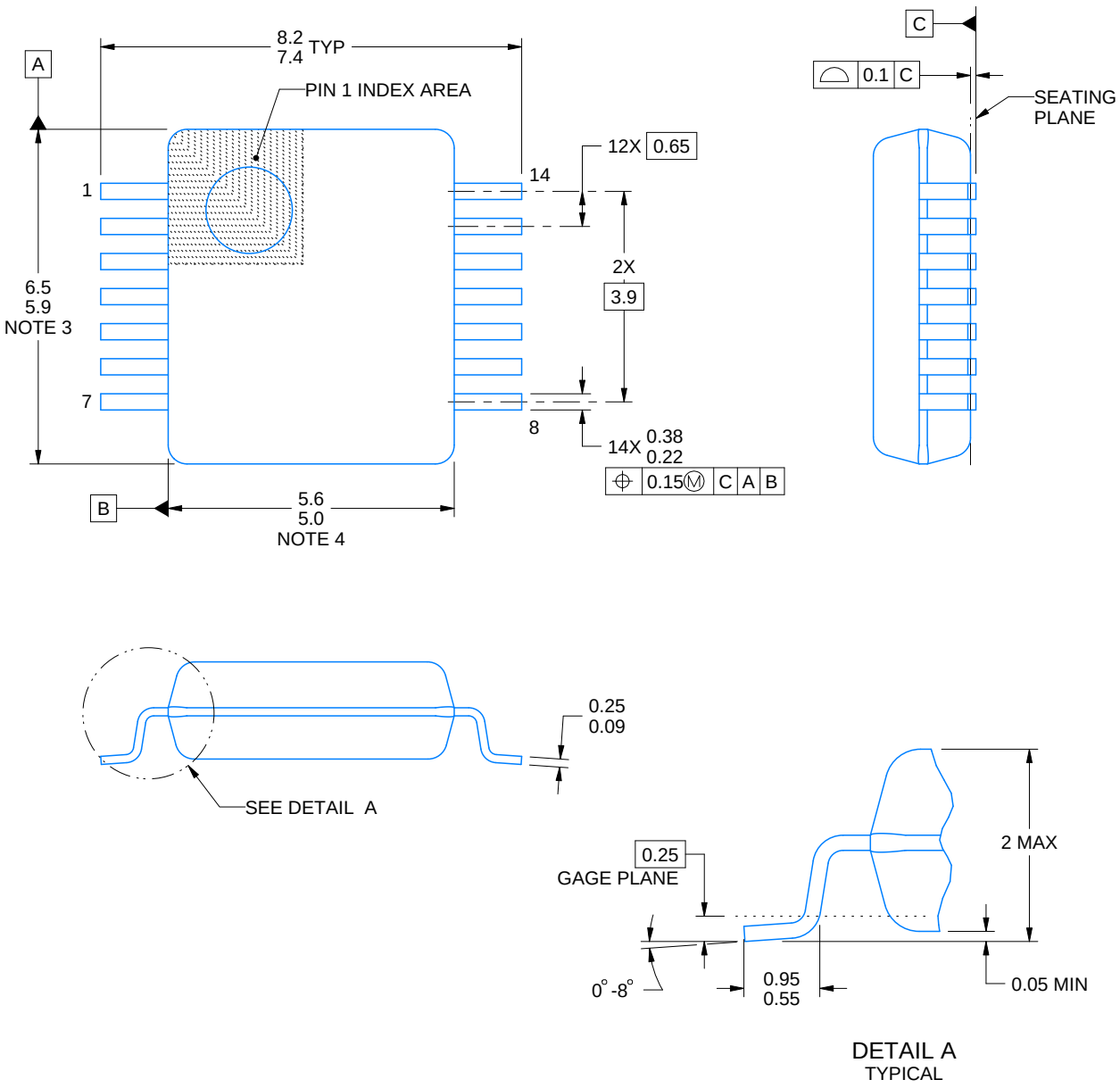
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

PACKAGE OUTLINE

DB0014A

SSOP - 2 mm max height

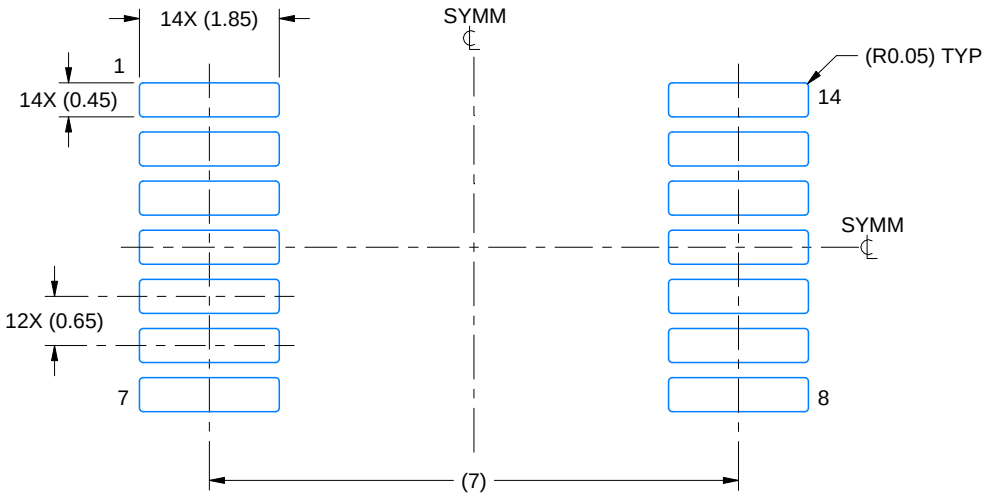
SMALL OUTLINE PACKAGE



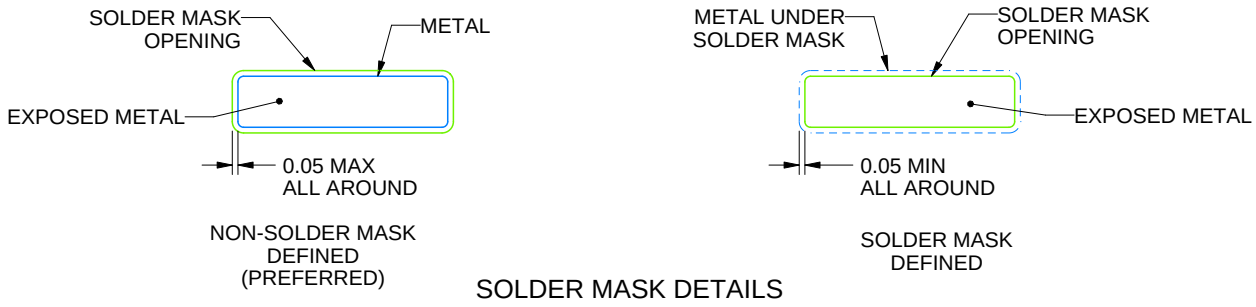
4220762/A 05/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

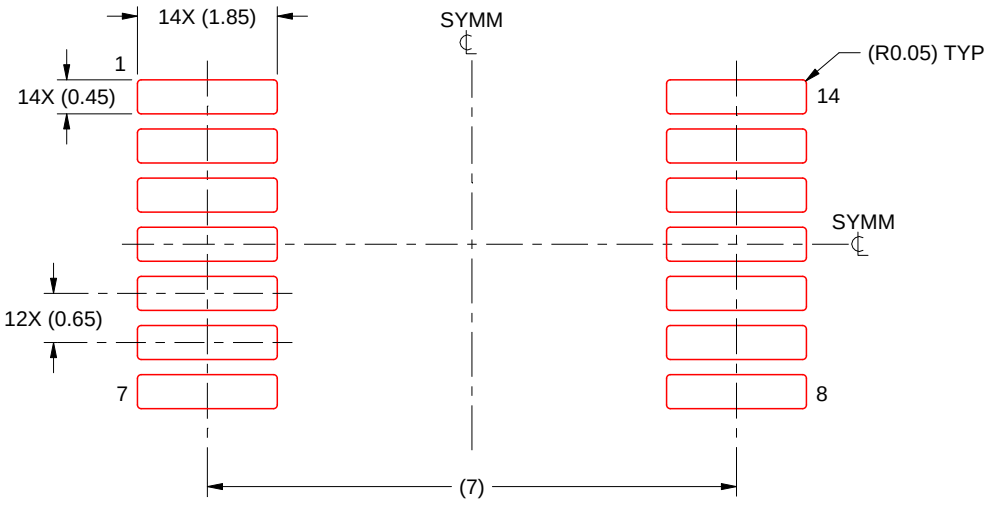


SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

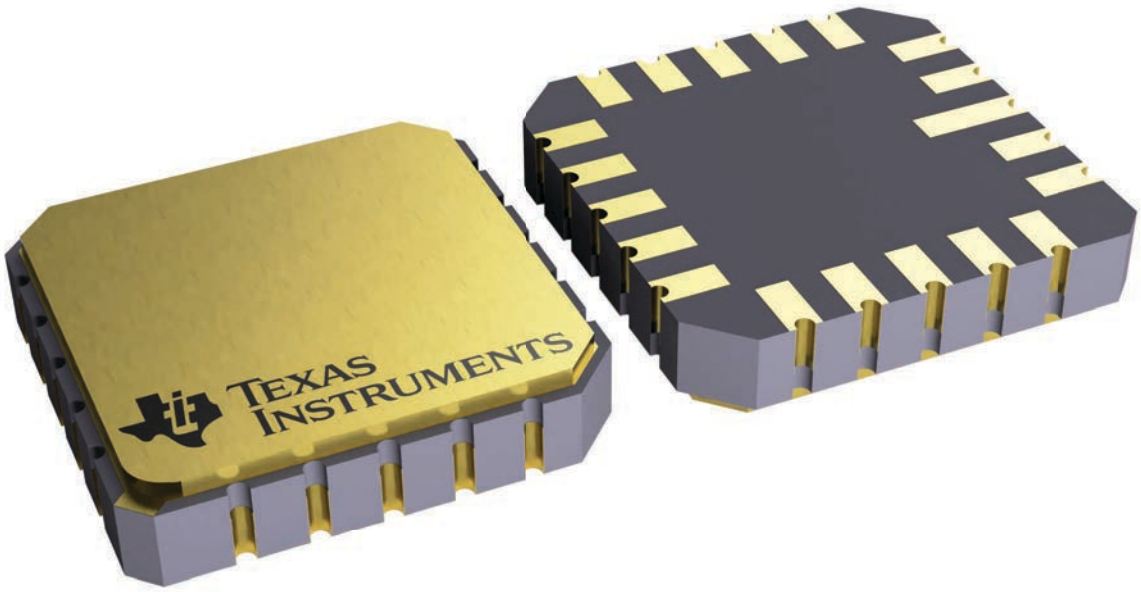
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

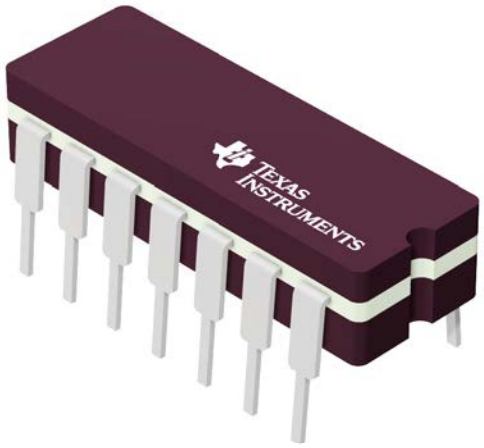


4229370VA\

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

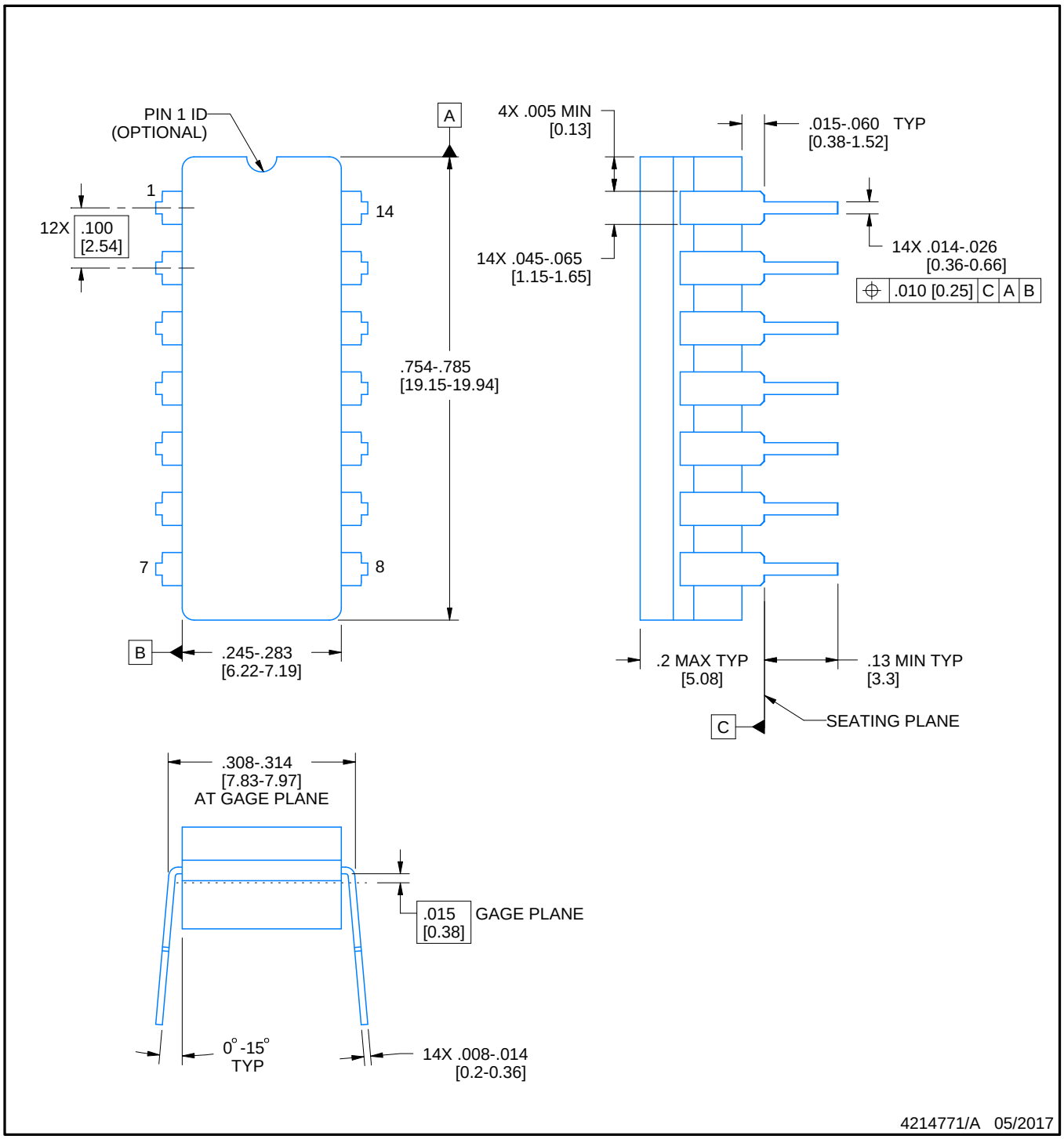
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

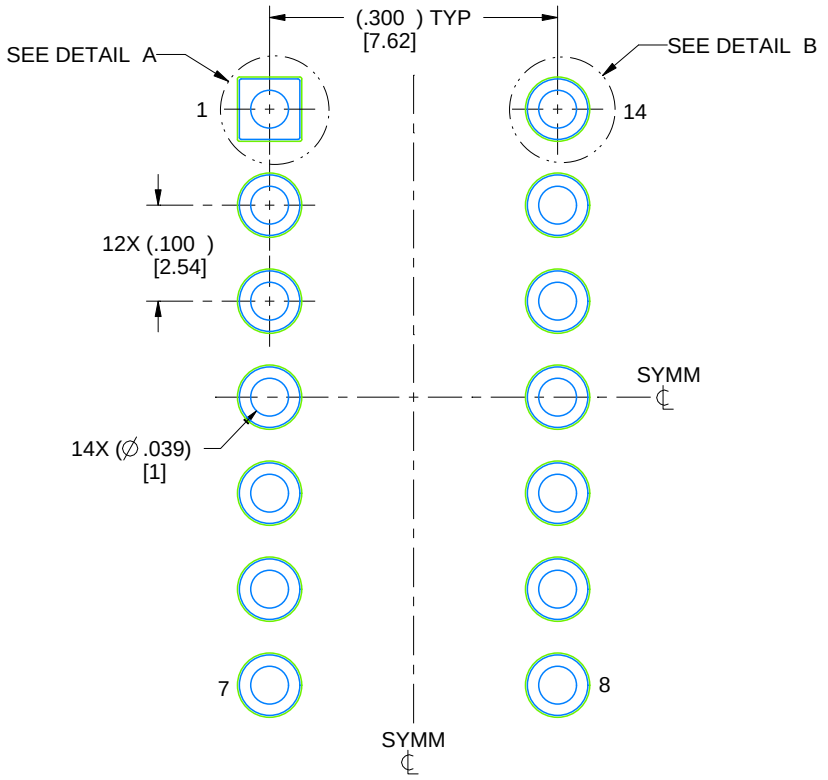
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

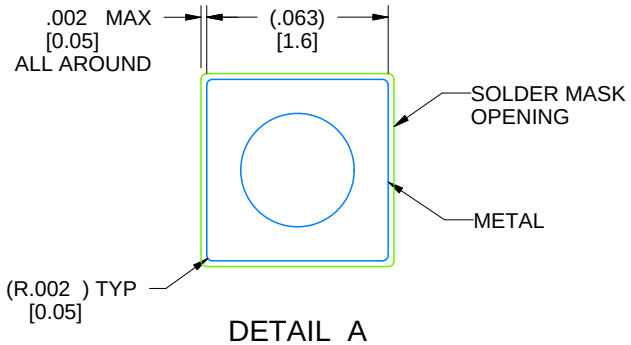
J0014A

CDIP - 5.08 mm max height

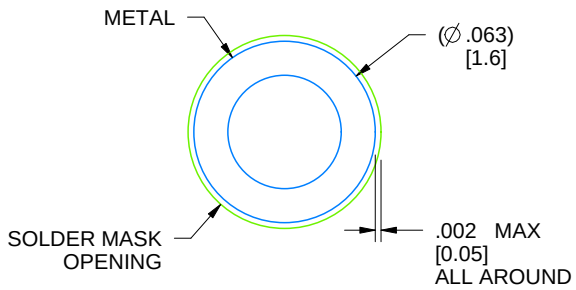
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



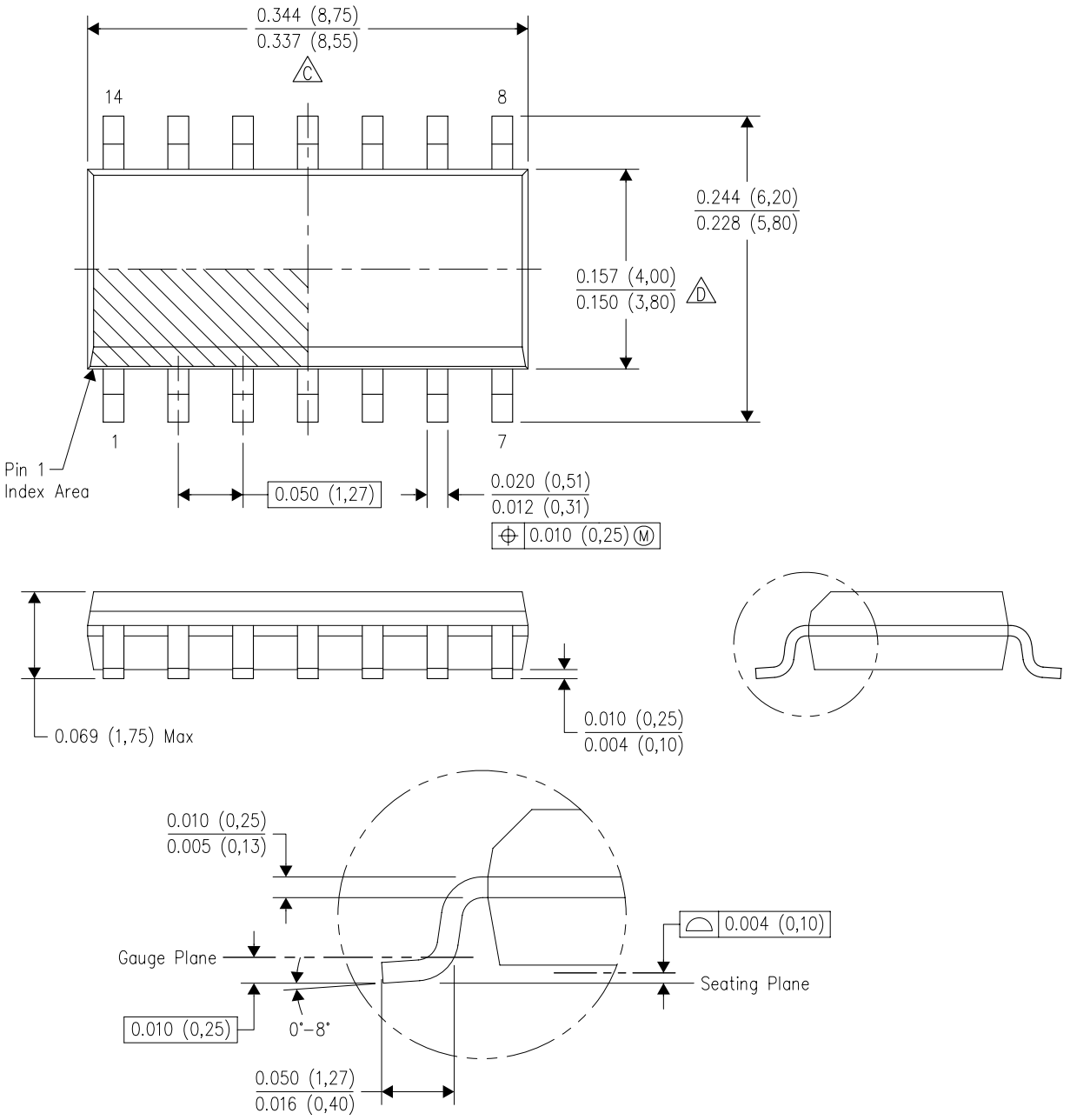
DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

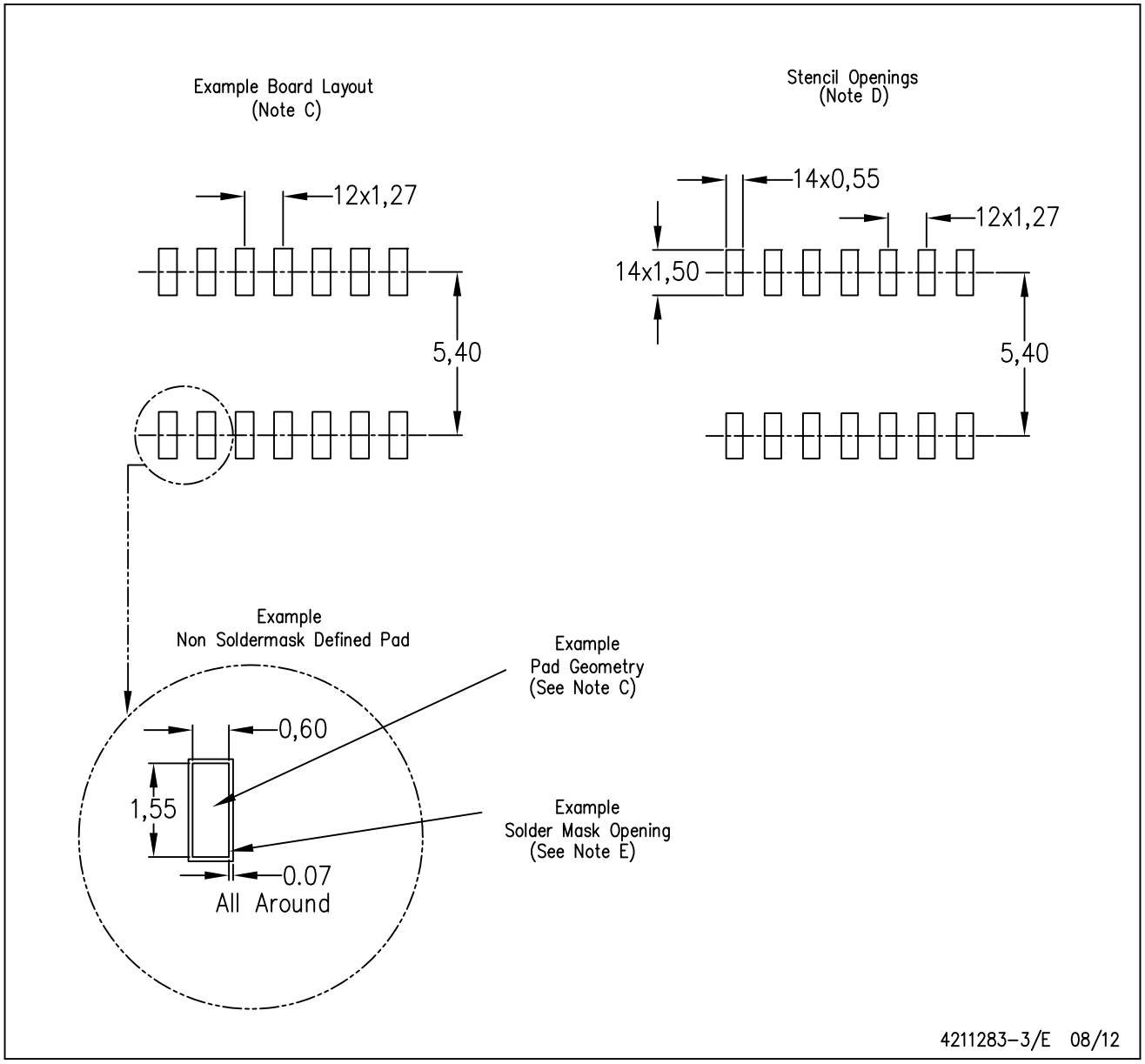
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

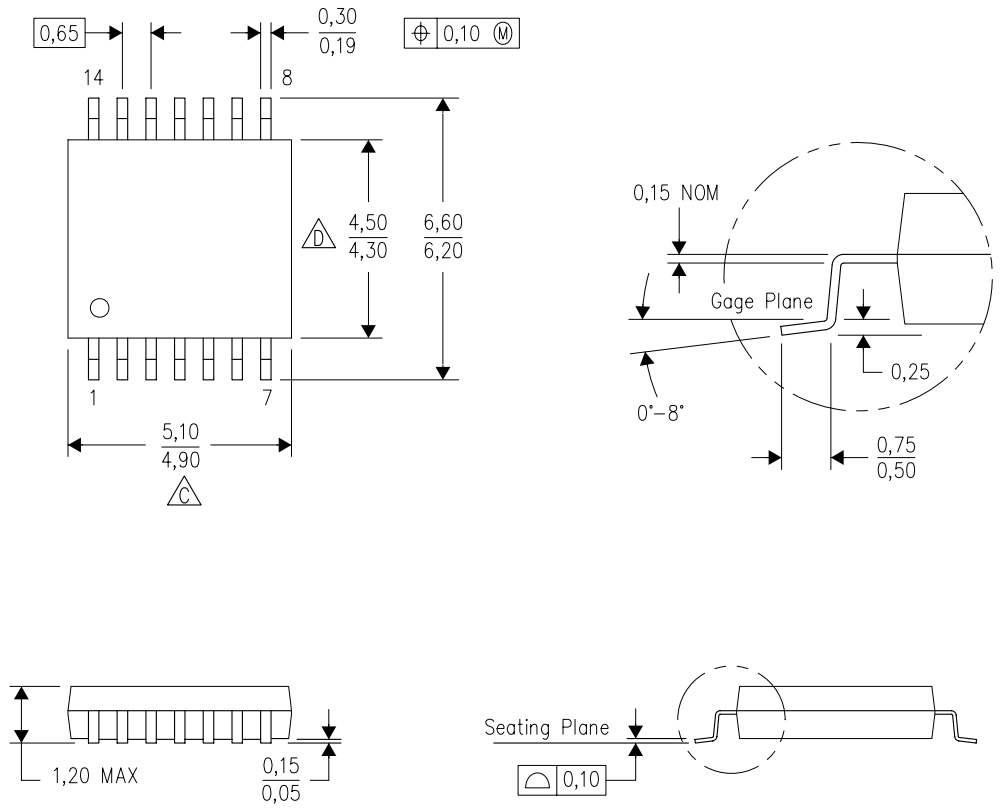
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



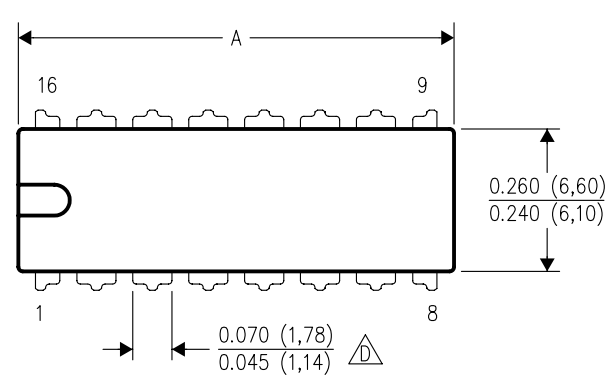
4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

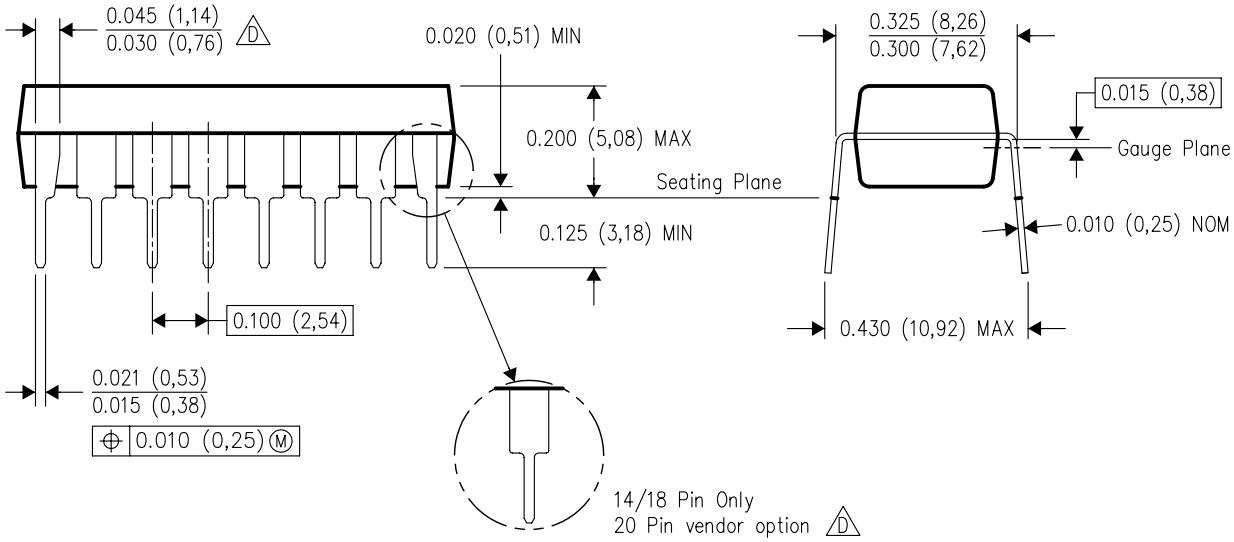
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265