TEXAS INSTRUMENTS
SN74AHC1G32
ZHCSW35Q – MARCH 1996 – REVISED APRIL 2024

# SN74AHC1G32 单路双输入正或门

## 1 特性

- 工作电压范围为 2V 至 5.5V
- 电压为 5V 时，$t_{pd}$ 最大值为 6.5ns
- 低功耗，$I_{CC}$ 最大值为 10 µ A
- 电压为 5V 时，输出驱动为 ±8mA
- 所有输入端均采用施密特触发器，使得电路能够承受较慢的输入上升和下降时间
- 闩锁性能超过 250mA，符合 JESD 17 规范

## 2 应用

- AV 接收器
- 便携式音频底座
- 蓝光播放器和家庭影院
- MP3 播放器和录像机
- 个人数字助理 (PDA)
- 电源：
  - 电信和服务器交流/直流电源
  - 单个控制器
    - 模拟
    - 数字
- 客户端和企业级固态硬盘 (SSD)
- LCD 电视、数字电视和高清电视 (HDTV)
- 企业级平板电脑
- 视频分析服务器
- 无线耳机、键盘和鼠标

## 3 说明

SN74AHC1G32 器件是一个单路 2 输入正或门。该器件以正逻辑执行布尔函数 $Y = A + B$ or $Y = \overline{A \bullet B}$ 。

**封装信息**

| 器件型号 | 封装(1) | 封装尺寸(2) | 本体尺寸(3) |
|---|---|---|---|
| SN74AHC1G32 | DBV ( SOT-23，5 ) | 2.90mm x 2.8mm | 2.90mm x 1.60mm |
| | DCK ( SC70，5 ) | 2.00mm x 2.1mm | 2.00mm x 1.25mm |
| | DRL ( SOT，5 ) | 1.60mm x 1.6mm | 1.60mm x 1.20mm |

(1) 如需了解更多信息，请参阅第 11 节。
(2) 封装尺寸 ( 长 × 宽 ) 为标称值，并包括引脚 ( 如适用 ) 。
(3) 本体尺寸 ( 长 × 宽 ) 为标称值，不包括引脚。


简化原理图

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# 4 Pin Configuration and Functions

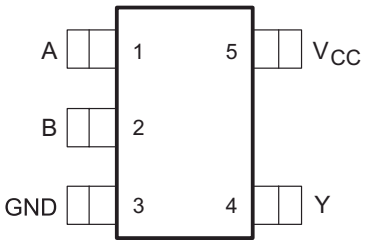



**图 4-1. DBV Package 5-Pin SOT-23 Top View**

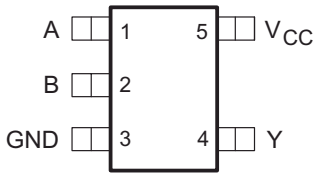
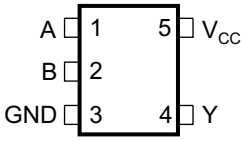



**图 4-2. DCK Package 5-Pin SC70 Top View**




See mechanical drawings for dimensions.

**图 4-3. DRL Package 5-Pin SOT Top View**

**表 4-1. Pin Functions**

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | A | I | Input A |
| 2 | B | I | Input B |
| 3 | GND | — | Ground Pin |
| 4 | Y | O | Output Y |
| 5 | $V_{CC}$ | — | Power Pin |

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | – 0.5 | 7 | V |
| $V_I$ | Input voltage (2) | | – 0.5 | 7 | V |
| $V_O$ | Output voltage (2) | | – 0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | ($V_I$ < 0) | | – 20 | mA |
| $I_{OK}$ | Output clamp current | ($V_O$ < 0 or $V_O$ > $V_{CC}$) | | ±20 | mA |
| $I_O$ | Continuous output current | ($V_O$ = 0 to $V_{CC}$) | | ±25 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±50 | mA |
| $T_J$ | Maximum junction temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature | | – 60 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±1500 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | – 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | – 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | – 8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise and fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | |

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $T_A$ | Operating free-air temperature | –40 | 125 | °C |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*, SCBA004.

## 5.4 Thermal Information

| THERMAL METRIC(1) | | SN74AHC1G32 | | | UNIT |
|---|---|---|---|---|---|
| | | DBV (SOT-23) | DCK (SC70) | DRL (SOT) | |
| | | 5 PINS | 5 PINS | 5 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 278 | 293.4 | 328.7 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 180.5 | 208.8 | 105.1 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 184.4 | 180.6 | 150.3 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 115.4 | 120.6 | 6.9 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 183.4 | 179.5 | 148.4 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | $T_A$ = 25°C | | | –40 TO +80°C | | –40 TO +125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | High level output voltage | $I_{OH}$ = –50 µA | | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | | V |
| | | | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | | $I_{OH}$ = –4 mA | | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | | $I_{OH}$ = –8 mA | | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | Low level output voltage | $I_{OL}$ = 50 µA | | 2 V | | | 0.1 | | 0.1 | | 0.1 | v |
| | | | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 4 mA | | 3 V | | | 0.36 | | 0.44 | | 0.44 | |
| | | $I_{OL}$ = 8 mA | | 4.5 V | | | 0.36 | | 0.44 | | 0.44 | |
| $I_I$ | Input leakage current | $V_I$ = 5.5 V or GND | | 0 V to 5.5 V | | | ±0.1 | | ±1 | | ±1 | µA |
| $I_{CC}$ | Supply current | $V_I$ = $V_{CC}$ or GND, | $I_O$ = 0 | 5.5 V | | | 1 | | 10 | | 10 | µA |
| $C_i$ | Input Capacitance | $V_I$ = $V_{CC}$ or GND | | 5 V | | 2 | 10 | | 10 | | 10 | pF |

## 5.6 Switching Characteristics, $V_{CC}$ = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit And Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | –40°C to +85°C | | | –40°C to +125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 5.5 | 7.9 | 1 | | 9.5 | 1 | | 10 | ns |
| $t_{PHL}$ | | | | | 5.5 | 7.9 | 1 | | 9.5 | 1 | | 10 | |

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit And Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | −40°C to +85°C | | | −40°C to +125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 8 | 11.4 | 1 | | 13 | 1 | | 14 | ns |
| $t_{PHL}$ | | | | | 8 | 11.4 | 1 | | 13 | 1 | | 14 | |

## 5.7 Switching Characteristics, $V_{CC}$ = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit And Voltage Waveforms)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | −40°C to +85°C | | | −40°C to +125°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 15 pF | | 3.8 | 5.5 | 1 | | 6.5 | 1 | | 7 | ns |
| $t_{PHL}$ | | | | | 3.8 | 5.5 | 1 | | 6.5 | 1 | | 7 | |
| $t_{PLH}$ | A or B | Y | $C_L$ = 50 pF | | 5.3 | 7.5 | 1 | | 8.5 | 1 | | 9.5 | ns |
| $t_{PHL}$ | | | | | 5.3 | 7.5 | 1 | | 8.5 | 1 | | 9.5 | |

## 5.8 Operating Characteristics

$V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 14 | pF |

## 5.9 Typical Characteristics

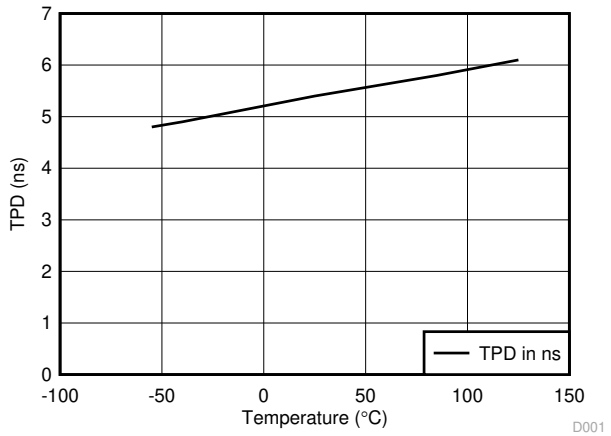



图 5-1. TPD vs Temperature

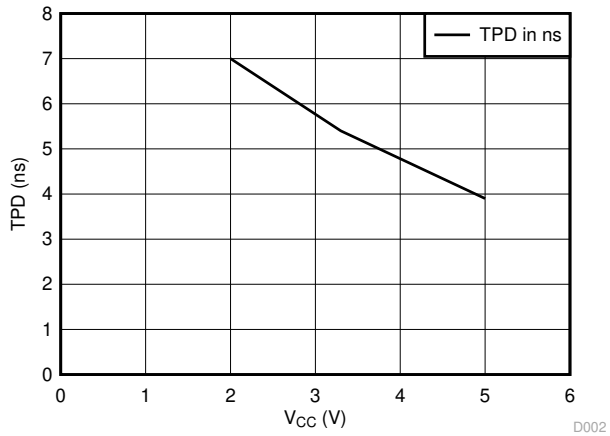
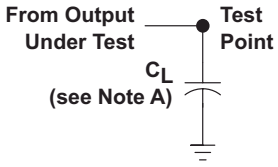
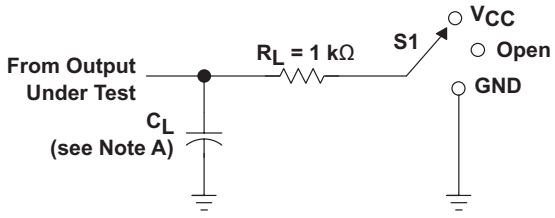



图 5-2. TPD vs $V_{CC}$

## 6 Parameter Measurement Information

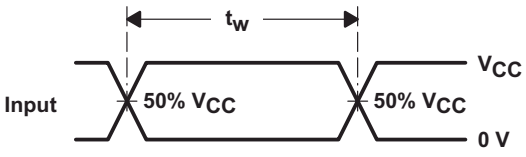



LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

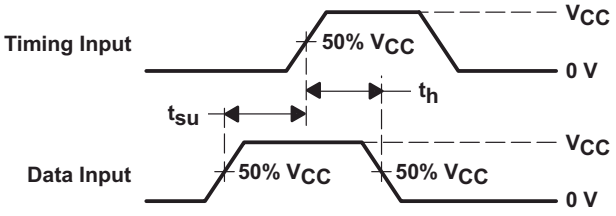



| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |
| Open Drain | $V_{CC}$ |

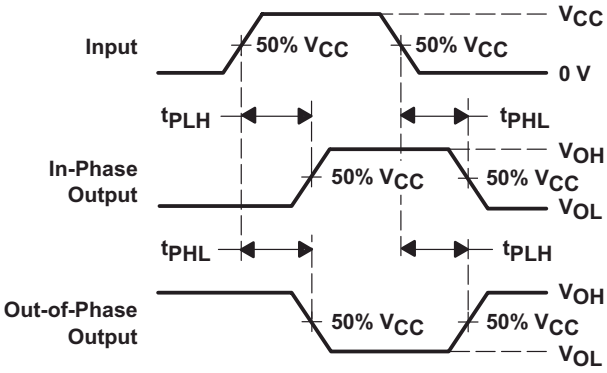
LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS



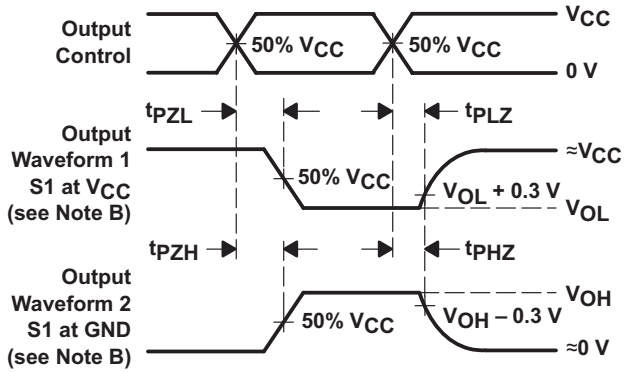

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

**图 6-1. Load Circuit and Voltage Waveforms**

# 7 Detailed Description

## 7.1 Overview

The SN74AHC1G32 device is a single 2-input positive OR gate with low drive that produces slow rise and fall times. This reduces ringing on the output signal. The device also has Schmitt-trigger action that will allow for slower or noisier inputs. The input signals are high impedance when $V_{CC}$ = 0 V.

## 7.2 Functional Block Diagram


## 7.3 Feature Description

- Wide operating voltage
  - Operates from 2 V to 5.5 V
- Allows down voltage translation
  - Accepts input voltages to 5.5 V

## 7.4 Device Functional Modes

表 7-1 shows the functional modes of the SN74AHC1G32 device.

**表 7-1. Function Table**

| INPUTS(1) | | OUTPUT(2) |
|---|---|---|
| A | B | Y |
| H | X | H |
| X | H | H |
| L | L | L |

(1) H = High Voltage Level, L = Low Voltage Level, X = Don’t Care
(2) H = Driving High, L = Driving Low, Z = High Impedance State

# 8 Application and Implementation

**备注**

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

## 8.1 Application Information

The SN74AHC1G32 is a low-drive CMOS device that can be used for a multitude of bus-interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs can except voltages to 5.5 V at any valid $V_{CC}$ making it ideal for down translation.

## 8.2 Typical Application

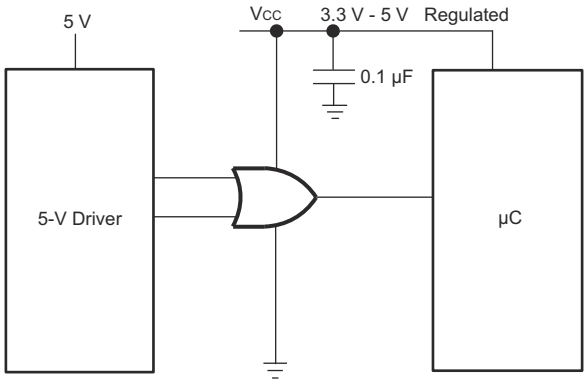



**图 8-1. Specific Application Schematic**

### 8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

### 8.2.2 Detailed Design Procedure

- Recommended input conditions
  - Specified high and low levels. See ($V_{IH}$ and $V_{IL}$) in the *节 5.3* table.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid $V_{CC}$
- Recommended output conditions
  - Load currents should not exceed 25 mA per output and 50 mA total for the part
  - Outputs should not be pulled above $V_{CC}$

### 8.2.3 Application Curve

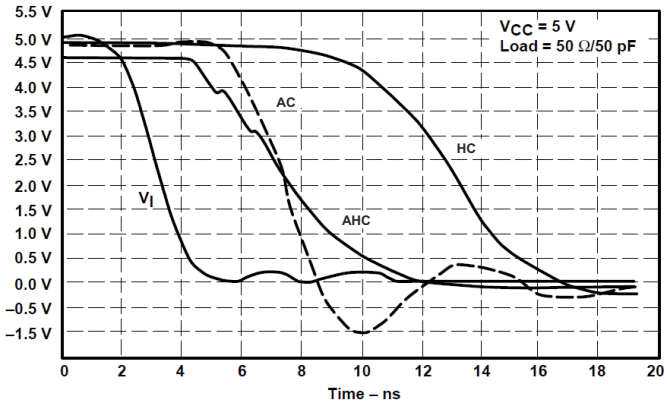



图 8-2. Switching Characteristics Comparison

## 8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the 节 5.3 table.

Each $V_{CC}$ pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μf is recommended; if there are multiple $V_{CC}$ pins, then 0.01 μf or 0.022 μf is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μf and a 1 μf are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 8.4 Layout

### 8.4.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. 图 8-3 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or $V_{CC}$, whichever makes more sense or is most convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.

### 8.4.2 Layout Example

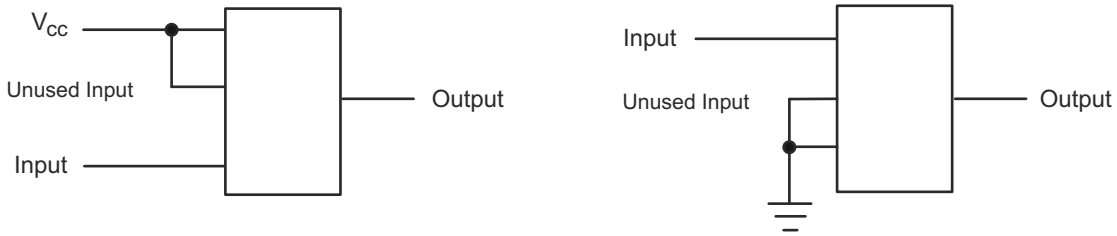



图 8-3. Layout Diagram

# 9 Device and Documentation Support

## 9.1 Documentation Support (Analog)

### 9.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**表 9-1. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| SN74AHC1G32 | Click here | Click here | Click here | Click here | Click here |

## 9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

## 9.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

## 9.4 Trademarks

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## 9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 9.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

# 10 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision P (February 2017) to Revision Q (April 2024) | Page |
|---|---|
| • 更新了整个文档中的编号、格式、表格、图和交叉参考，以反映现代数据表标准 | 1 |
| • Updated R θ JA values: DBV = 231.3 to 278, DCK = 287.6 to 293.4; Updated DBV and DCK packages for R θ JC(top), R θ JB, ΨJT, ΨJB, and R θ JC(bot), all values in °C/W | 5 |

| Changes from Revision O (July 2014) to Revision P (February 2017) | Page |
|---|---|
| • Changed *Handling Ratings* table to *ESD Ratings* table | 4 |
| • Added MAX values for $T_A$ = 25°C in both *Switching Characteristics* tables. | 5 |

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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