DGG OR DL PACKAGE

/TOD VIEW



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FEATURES

- Member of the Texas Instruments Widebus™
 Family
- Operates From 1.65 V to 3.6 V
- Max t_{nd} of 4.2 ns at 3.3 V
- ±12-mA Output Drive at 3.3 V
- All Outputs Have Equivalent 26- Ω Series Resistors, So No External Resistors Are Required
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

DESCRIPTION/ORDERING INFORMATION

This 16-bit (dual-octal) noninverting bus transceiver is designed for 1.65-V to 3.6-V $V_{\rm CC}$ operation.

The SN74ALVCHR16245 is designed for asynchronous communication between data buses. The control-function implementation minimizes external timing requirements.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated.

(TOP VIEW)									
1DIR [1 U	48 1 0E							
1B1 [2	47 1A1							
1B2	3	46 1A2							
GND	4								
_	· ·	45 GND							
1B3 [5	44 1 1A3							
1B4 [6	43 1A4							
V_{CC}	7	42 V _{CC}							
1B5 [8	41 🛮 1A5							
1B6 [9	40 1A6							
GND [10	39 GND							
1B7 [11	38] 1A7							
1B8 [12	37] 1A8							
2B1 [13	36 2A1							
2B2 [14	35 2A2							
GND [15	34 GND							
2B3 [16	33] 2A3							
2B4 [17	32 2A4							
V _{CC}	18	31 V _{CC}							
2B5 [19	30 2A5							
2B6 [20	29] 2A6							
GND [21	28 GND							
2B7 [22	27 2A7							
2B8 [23	26 2A8							
2DIR [24	25 2 0E							

All outputs, which are designed to sink up to 12 mA, include equivalent 26- Ω series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹)	ORDERABLE PART NUMBER	TOP-SIDE MARKING	
	SSOP - DL	Tape and reel	SN74ALVCHR16245LR	ALVCHR16245	
40°C to 95°C	TSSOP - DGG	Tape and reel	SN74ALVCHR16245GR	ALVCHR16245	
-40°C to 85°C	VFBGA - GQL	Tana and real	SN74ALVCHR16245KR	VD245	
	VFBGA - ZQL (Pb-free)		74ALVCHR16245ZQLR	- VR245	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

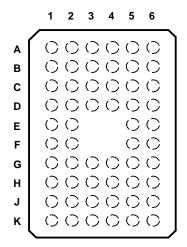


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Widebus is a trademark of Texas Instruments.



GQL OR ZQL PACKAGE (TOP VIEW)



TERMINAL ASSIGNMENTS(1)

	1	2	3	4	5	6
Α	1DIR	NC	NC	NC	NC	1 OE
В	1B2	1B1	GND	GND	1A1	1A2
С	1B4	1B3	V _{CC}	V _{CC}	1A3	1A4
D	1B6	1B5	GND	GND	1A5	1A6
E	1B8	1B7			1A7	1A8
F	2B1	2B2			2A2	2A1
G	2B3	2B4	GND	GND	2A4	2A3
Н	2B5	2B6	V _{CC}	V _{CC}	2A6	2A5
J	2B7	2B8	GND	GND	2A8	2A7
K	2DIR	NC	NC	NC	NC	2 OE

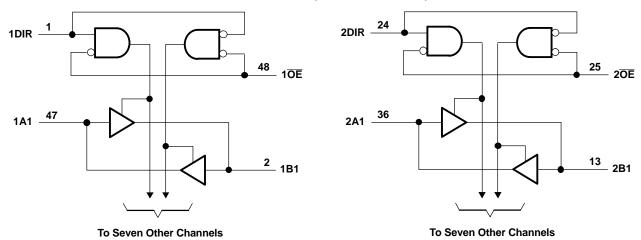
(1) NC - No internal connection

FUNCTION TABLE (each 8-bit section)

INP	UTS	OPERATION
ŌĒ	DIR	OPERATION
L	L	B data to A bus
L	Н	A data to B bus
Н	Χ	Isolation



LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the DGG and DL packages.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	4.6	V
\/	lanut valtaga ranga	Except I/O ports (2)	-0.5	4.6	V
VI	Input voltage range	I/O ports ⁽²⁾⁽³⁾	-0.5	V _{CC} + 0.5	V
Vo	Output voltage range ⁽²⁾⁽³⁾		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
Io	Continuous output current			±50	mA
	Continuous current through each V _{CC} o	or GND		±100	mA
		DGG package		70	
θ_{JA}	Package thermal impedance (4)	DL package		63	°C/W
		GQL/ZQL package		42	
T _{stg}	Storage temperature range		-65	150	°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

⁽²⁾ The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

³⁾ This value is limited to 4.6 V maximum.

⁽⁴⁾ The package thermal impedance is calculated in accordance with JESD 51-7.

SN74ALVCHR16245 16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS





RECOMMENDED OPERATING CONDITIONS(1)

			MIN	MAX	UNIT
V _{CC}	Supply voltage		1.65	3.6	V
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		
V_{IH}	High-level input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7		V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		V _{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$	
V_{IL}	Low-level input voltage	V _{CC} = 2.3 V to 2.7 V		0.7	V
		V _{CC} = 2.7 V to 3.6 V		0.8	
VI	Input voltage		0	V _{CC}	V
Vo	Output voltage		0	V _{CC}	V
	V _{CC} = 1.65 V			-2	
	High level output outront	V _{CC} = 2.3 V		-6	mA
I _{OH}	High-level output current	V _{CC} = 2.7 V		-8	MA
		V _{CC} = 3 V		-12	
		V _{CC} = 1.65 V		2	
	Low lovel output ourrent	V _{CC} = 2.3 V		6	
I _{OL}	Low-level output current	V _{CC} = 2.7 V	8		mA
		V _{CC} = 3 V		12	
Δt/Δν	Input transition rise or fall rate			10	ns/V
T _A	Operating free-air temperature		-40	85	°C

⁽¹⁾ All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74ALVCHR16245

16-BIT BUS TRANSCEIVER



ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TEST CONDITIONS	V _{cc}	MIN	TYP ⁽¹⁾	MAX	UNIT		
		I _{OH} = -100 μA	1.65 V to 3.6 V	V _{CC} - 0.2					
		I _{OH} = -2 mA	1.65 V	1.2					
		I _{OH} = -4 mA	2.3 V	1.9					
V_{OH}	V _{OH}	L C A	2.3 V	1.7			V		
		I _{OH} = -6 mA	3 V	2.4					
		I _{OH} = -8 mA	2.7 V	2					
	/ _{OL} I I(hold) OZ (3) CC	I _{OH} = -12 mA	3 V	2					
		I _{OL} = 100 μA	1.65 V to 3.6 V			0.2			
		I _{OL} = 2 mA	1.65 V			0.45			
		I _{OL} = 4 mA	2.3 V			0.4			
V_{OL}		L C A	2.3 V			0.55	V		
		I _{OL} = 6 mA	3 V			0.55			
		I _{OL} = 8 mA	2.7 V			0.6			
		I _{OL} = 12 mA	3 V			0.8			
I _I		V _I = V _{CC} or GND	3.6 V			±5	μΑ		
		V _I = 0.58 V	1.65.\/	25					
		V _I = 1.07 V	1.65 V	-25					
		V _I = 0.7 V	221/	45					
I _{I(hold)}		V _I = 1.7 V	2.3 V	-45			μΑ		
		V _I = 0.8 V	2.1/	75					
		V _I = 2 V	3 V	-75					
		V _I = 0 to 3.6 V ⁽²⁾	3.6 V			±500			
I _{OZ} (3)		$V_O = V_{CC}$ or GND	3.6 V			±10	μΑ		
I _{CC}		$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			40	μΑ		
ΔI_{CC}		One input at V_{CC} - 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V			750	μΑ		
Ci	Control inputs	V _I = V _{CC} or GND	3.3 V		4		pF		
C _{io}	A or B ports	$V_O = V_{CC}$ or GND	3.3 V		9		pF		

⁽¹⁾ All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V	V _{CC} = 1 ± 0.2	2.5 V 2 V	V _{CC} =	2.7 V	V _{CC} = ± 0.3	3.3 V 3 V	UNIT
	(INPUT)	(001F01)	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	B or A	(1)	1	4.9		4.7	1	4.2	ns
t _{en}	ŌĒ	B or A	(1)	1	6.8		6.7	1	5.6	ns
t _{dis}	ŌĒ	B or A	(1)	1	6.3		5.7	1	5.5	ns

⁽¹⁾ This information was not available at the time of publication.

⁽²⁾ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

⁽³⁾ For I/O ports, the parameter I_{OZ} includes the input leakage current.

SN74ALVCHR16245 16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

SCES064G-DECEMBER 1995-REVISED OCTOBER 2004



OPERATING CHARACTERISTICS

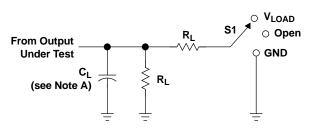
T_A = 25°C

	PARAMET	ΓER	TEST CONDITIONS	V _{CC} = 1.8 V TYP	V _{CC} = 2.5 V TYP	V _{CC} = 3.3 V TYP	UNIT
C	Power dissipation	Outputs enabled	C ₁ = 50 pF. f = 10 MHz	(1)	24	32	»E
Cpd	capacitance	Outputs disabled	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	(1)	4	5	p⊦

(1) This information was not available at the time of publication.



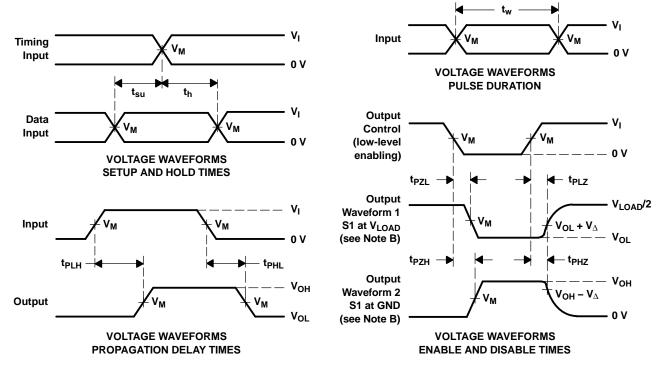
PARAMETER MEASUREMENT INFORMATION



TEST	S1
t _{pd}	Open
t _{PLZ} /t _{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

LOAD CIRCUIT

v	IN	PUT	V	v		6	v
V _{CC}	VI	t _r /t _f	V _M	V _{LOAD}	CL	R _L	$oldsymbol{V}_\Delta$
1.8 V	V _{CC}	≤ 2 ns	V _{CC} /2	2×V _{CC}	30 pF	1 k Ω	0.15 V
2.5 V \pm 0.2 V	V _{CC}	≤2 ns	V _{CC} /2	2×V _{CC}	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V \pm 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_{\Omega} = 50 \Omega$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

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PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
74ALVCHR16245GRG4	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCHR16245
74ALVCHR16245GRG4.B	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCHR16245
74ALVCHR16245LR1G4	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCHR16245
74ALVCHR16245LR1G4.B	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCHR16245
SN74ALVCHR16245GR	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCHR16245
SN74ALVCHR16245GR.B	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCHR16245
SN74ALVCHR16245LR	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCHR16245
SN74ALVCHR16245LR.B	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALVCHR16245

⁽¹⁾ Status: For more details on status, see our product life cycle.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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⁽²⁾ Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

PACKAGE OPTION ADDENDUM

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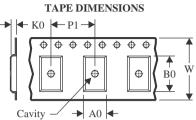
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

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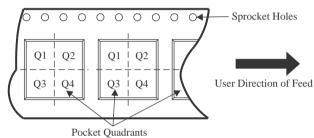
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74ALVCHR16245GRG4	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
74ALVCHR16245LR1G4	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
SN74ALVCHR16245GR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74ALVCHR16245LR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1



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*All dimensions are nominal

7 iii diiriorio die rierimidi										
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)			
74ALVCHR16245GRG4	TSSOP	DGG	48	2000	356.0	356.0	45.0			
74ALVCHR16245LR1G4	SSOP	DL	48	1000	356.0	356.0	53.0			
SN74ALVCHR16245GR	TSSOP	DGG	48	2000	356.0	356.0	45.0			
SN74ALVCHR16245LR	SSOP	DL	48	1000	356.0	356.0	53.0			

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.





SMALL OUTLINE PACKAGE



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
 4. Reference JEDEC registration MO-153.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 8. Board assembly site may have different recommendations for stencil design.



DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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