

## SN74HC4851-Q1 具有注入电流效应控制功能的汽车级 8 通道模拟多路复用器/多路解复用器

### 1 特性

- 符合汽车应用要求
- 注入电流交叉耦合  $<1\text{mV}/\text{mA}$   
( 请参阅应用信息 中的节 8.1 )
- 低开关间串扰
- 端子与 CD74HC4051、SN74LV4051A 和 CD4051B 器件兼容
- 2V 至 5.5V  $V_{\text{CC}}$  运行
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范的要求

### 2 应用

- 模拟和数字多路复用和多路信号分离
- 诊断和监控
- 区域架构
- 车身控制模块
- 电池管理系统 (BMS)
- HVAC 控制模块
- 汽车音响主机
- 远程信息处理
- 车载充电器 (OBC) 和无线充电

### 3 说明

这款八通道 CMOS 模拟多路复用器/多路解复用器的端子与 '4051 器件的功能兼容，并具有注入电流效应控制功能，此控制功能在电压通常超过正常电源电压的汽车应用中具有出色的价值。

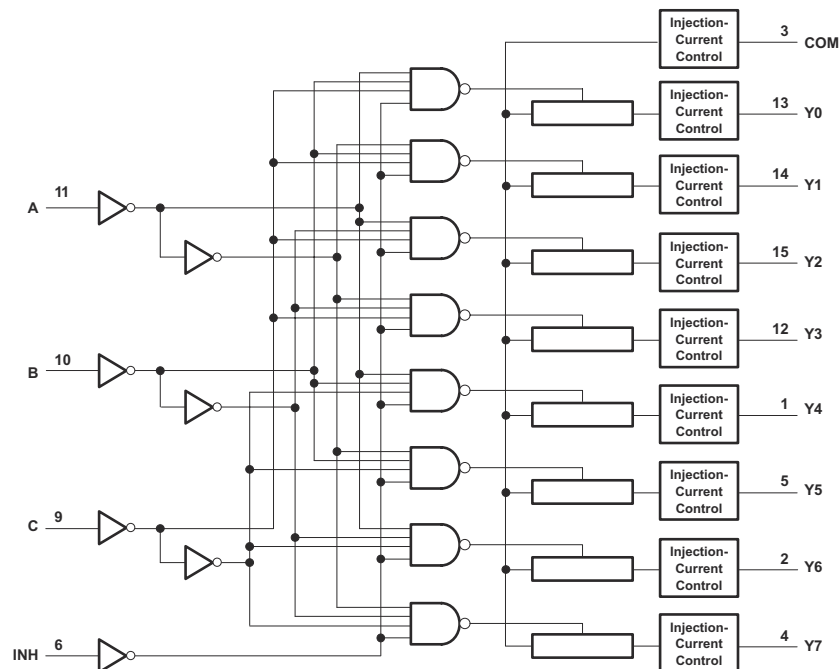
注入电流效应控制功能允许已禁用的模拟输入通道上的信号超过电源电压，而不会影响已启用的模拟通道的信号。由于具备这一特性，不再需要通常使用的外部二极管/电阻器网络将模拟通道信号保持在电源电压范围内。

#### 封装信息

器件型号	封装 <sup>(1)</sup>	封装尺寸 <sup>(2)</sup>
SN74HC4851-Q1	PW ( TSSOP , 16 )	5mm × 6.4mm

(1) 有关更多信息，请参阅节 11

(2) 封装尺寸 ( 长 × 宽 ) 为标称值，并包括引脚 ( 如适用 )。



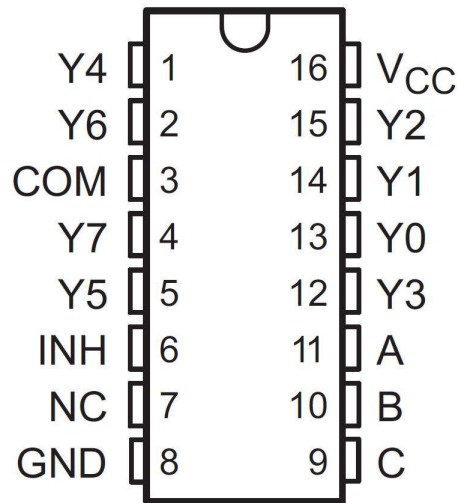
逻辑图 ( 正逻辑 )



## Table of Contents

<b>1 特性</b> .....	1	7.1 Functional Block Diagram.....	9
<b>2 应用</b> .....	1	<b>8 Application and Implementation</b> .....	10
<b>3 说明</b> .....	1	8.1 Application Information.....	10
<b>4 Pin Configuration and Functions</b> .....	2	<b>9 Device and Documentation Support</b> .....	12
<b>5 Specifications</b> .....	3	9.1 接收文档更新通知.....	12
5.1 Absolute Maximum Ratings.....	3	9.2 支持资源.....	12
5.2 Thermal Information: SN74HC485x-Q1.....	3	9.3 Trademarks.....	12
5.3 Recommended Operating Conditions.....	4	9.4 静电放电警告.....	12
5.4 Electrical Characteristics.....	5	9.5 术语表.....	12
5.5 Timing Characteristics.....	6	<b>10 Revision History</b> .....	12
5.6 Injection Current Coupling.....	6	<b>11 Mechanical, Packaging, and Orderable Information</b> .....	12
<b>6 Parameter Measurement Information</b> .....	7		
<b>7 Detailed Description</b> .....	9		

## 4 Pin Configuration and Functions



NC – No internal connection

图 4-1. SN74HC4851-Q1 PW Package, 16-Pin TSSOP (Top View)

表 4-1. Function Table

Inputs				On Channel
INH	C	B	A	Yx
L	L	L	L	Y0
L	L	L	H	Y1
L	L	H	L	Y2
L	L	H	H	Y3
L	H	L	L	Y4
L	H	L	H	Y5
L	H	H	L	Y6
L	H	H	H	Y7
H	X	X	X	None

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	- 0.5	6	V
V <sub>SEL</sub> or V <sub>EN</sub>	Logic control input pin voltage ( $\overline{EN}$ , A0, A1, A2)	- 0.5	V <sub>CC</sub> +0.5V	V
V <sub>S</sub> or V <sub>D</sub>	Source or drain voltage (Sx, D)	- 0.5	V <sub>CC</sub> +0.5V	V
I <sub>IK</sub>	Input clamp current (V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub> )	- 20	20	mA
I <sub>IOK</sub>	I/O diode current (V <sub>IO</sub> < 0 or V <sub>IO</sub> > V <sub>CC</sub> )	- 20	20	mA
I <sub>T</sub>	Switch through current (V <sub>IO</sub> = 0 to V <sub>CC</sub> )	- 25	25	mA
I <sub>GND</sub>	Continuous current through V <sub>CC</sub> or GND	- 50	50	mA
T <sub>stg</sub>	Storage temperature	- 65	150	°C
T <sub>J</sub>	Junction temperature		150	

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 Thermal Information: SN74HC485x-Q1

THERMAL METRIC <sup>(1)</sup>		SN74HC485x-Q1	
		PW (TSSOP)	
		PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	139.6	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2		5.5	V
V <sub>IH</sub>	Input logic high	2V	1.5			V
		2.5V	2.1			
		3.3V	2.3			
		4.5V	3.15			
		5.5V	4.2			
V <sub>IL</sub>	Input logic low	2V	0		0.5	V
		2.5V	0		0.7	
		3.3V	0		0.8	
		4.5V	0		0.95	
		5.5V	0		1.05	
V <sub>SEL</sub> or V <sub>EN</sub>	Logic control input pin voltage ( $\overline{EN}$ , A0, A1, A2)		0		V <sub>CC</sub>	V
V <sub>S</sub> or V <sub>D</sub>	Signal path input/output voltage (source or drain pin) (Sx, D)		0		V <sub>CC</sub>	V
$\Delta t / \Delta v$	Input transition rise or fall time	V <sub>CC</sub> = 2V			1000	ns
		V <sub>CC</sub> = 3V			800	
		V <sub>CC</sub> = 3.3V			700	
		V <sub>CC</sub> = 4.5V			500	
		V <sub>CC</sub> = 5.5V			400	
T <sub>A</sub>	Ambient temperature		- 40		125	°C

## 5.4 Electrical Characteristics

 At specified  $V_{CC} \pm 10\%$ 

 Typical values measured at nominal  $V_{CC}$ .

PARAMETER		TEST CONDITIONS	$V_{CC}$	Operating free-air temperature ( $T_A$ )									UNIT
				25°C			- 40°C to 85°C			- 40°C to 125°C			
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$R_{ON}$	On-state switch resistance	$V_S = 0V$ to $V_{CC}$ $I_{SD} = 0.5mA$	2V	500	650		670		700		$\Omega$		
			3V	215	280		320		360				
			3.3V	210	270		305		345				
			4.5V	160	210		240		270				
$\Delta R_{ON}$	On-state switch resistance matching between inputs	$V_S = V_{CC} / 2$ $I_{SD} = 0.5mA$	2V	4	13		18		23		$\Omega$		
			3V	2	10		12		16				
			3.3V	2	9		12		16				
			4.5V	2	9		12		16				
$I_I$	Control input current	$V_I = V_{CC}$ or GND	5V		$\pm 0.1$		$\pm 0.1$		$\pm 1$	$\mu A$			
$I_{S(OFF)}$	Off-state switch leakage current (any one channel)	Switch Off $V_{INH} = V_{IH}$ $V_D = V_{CC} / GND$ $V_S = GND / V_{CC}$	5V		$\pm 0.1$		$\pm 0.5$		$\pm 1$	$\mu A$			
	Off-state switch leakage current (common channel)				$\pm 0.2$		$\pm 2$		$\pm 4$	$\mu A$			
$I_{S(ON)}$	Channel on-state leakage current	Switch Off $V_{INH} = V_{IL}$ $V_D = V_{CC} / GND$ $V_S = GND / V_{CC}$	5V		$\pm 0.1$		$\pm 0.5$		$\pm 1$	$\mu A$			
$I_{DD}$	$V_{CC}$ supply current	Logic inputs = 0V or $V_{CC}$	5V		2		20		40	$\mu A$			
$C_{IC}$	Control input capacitance	A, B, C, INH		3.5	10		10		10	pF			
$C_{IS}$	Common terminal capacitance	Switch off		22	40		40		40	pF			
$C_{OS}$	Switch terminal capacitance	Switch off		6.7	15		15		15	pF			
$C_{PD}$	Power Dissipation Capacitance	No Load $t_r = t_f = 1ns$ $f = 1MHz$	3.3V	32						pF			
			5V	37									

## 5.5 Timing Characteristics

At specified  $V_{CC} \pm 10\%$

Typical values measured at nominal  $V_{CC}$ .

PARAMETER	TEST CONDITIONS	$V_{CC}$	Operating free-air temperature ( $T_A$ )									UNIT
			25°C			- 40°C to 85°C			- 40°C to 125°C			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS <sup>(1)</sup>												
$t_{PD}$	Propagation delay	$C_L = 50\text{pF}$ Sx to D, D to Sx	2V	19.5	30		34		37	ns		
			3V	12	17.5		19.5		21.5			
			3.3V	11	16.5		18.5		20.5			
			5.5V	8.6	14		15		16			
$t_{TRAN}$	Transition-time between inputs	$R_L = 10\text{k}\Omega$ , $C_L = 50\text{pF}$ Ax to D, Ax to Sx	2V	44	94		103		103	ns		
			3V	30	63		67		67			
			3.3V	23	51		54		54			
			5.5V	18	43		46		46			
$t_{ON(EN)}$	Turnon-time from enable	$R_L = 10\text{k}\Omega$ , $C_L = 50\text{pF}$ EN to D, EN to Sx	2V		95		105		115	ns		
			3V		90		100		110			
			3.3V		85		95		105			
			5V		80		90		100			
$t_{OFF(EN)}$	Turnoff time from enable	$R_L = 10\text{k}\Omega$ , $C_L = 50\text{pF}$ EN to D, EN to Sx	2V		95		105		115	ns		
			3V		90		100		110			
			3.3V		85		95		105			
			5.5V		80		90		100			

(1)  $t_{PLH}/t_{PHL} = t_{PD}$  propagation delay time,  $t_{PZH}/t_{PZL} = t_{ON(EN)}$  enable delay time,  $t_{PHZ}/t_{PLZ} = t_{OFF(EN)}$  disable delay time,  $t_{PLH}/t_{PHL}$  Channel select =  $t_{TRAN}$

## 5.6 Injection Current Coupling

At specified  $V_{CC} \pm 10\%$

Typical values measured at nominal  $V_{CC}$  and  $T_A = 25^\circ\text{C}$ .

PARAMETER	$V_{CC}$	TEST CONDITIONS	-40°C to 125°C			UNIT		
			MIN	TYP	MAX			
INJECTION CURRENT COUPLING								
$\Delta V_{OUT}$	Maximum shift of output voltage of enabled analog input <sup>(1)</sup>	3.3V	$R_S \leq 3.9\text{k}\Omega$	$I_{INJ} \leq 1\text{mA}$	0.05	1	mV	
		5V			0.1	1		
		3.3V		$R_S \leq 20\text{k}\Omega$	$I_{INJ} \leq 10\text{mA}$	0.345		5
		5V				0.067		5
		3.3V	$R_S \leq 20\text{k}\Omega$	$I_{INJ} \leq 1\text{mA}$	0.05	2		
		5V			0.11	2		
		3.3V		$I_{INJ} \leq 10\text{mA}$	0.05	20		
		5V			0.024	20		

(1)  $I_{INJ}$  = total current injected into all disabled channels

## 6 Parameter Measurement Information

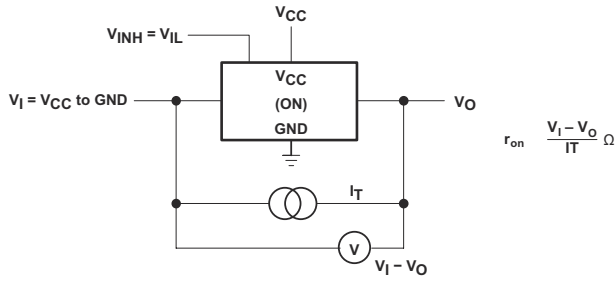


图 6-1. On-State-Resistance Test Circuit

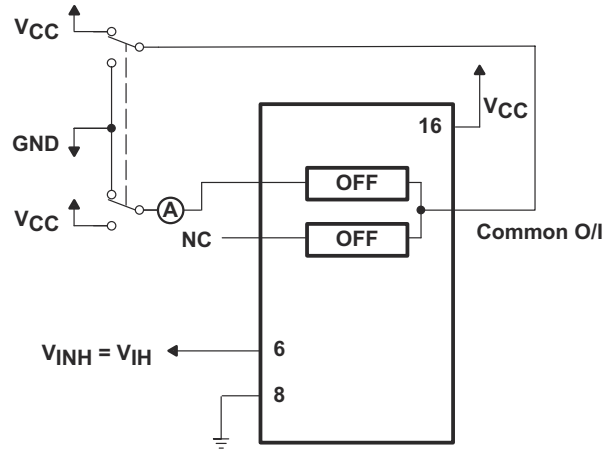


图 6-2. Maximum Off-Channel Leakage Current, Any One Channel, Test Setup

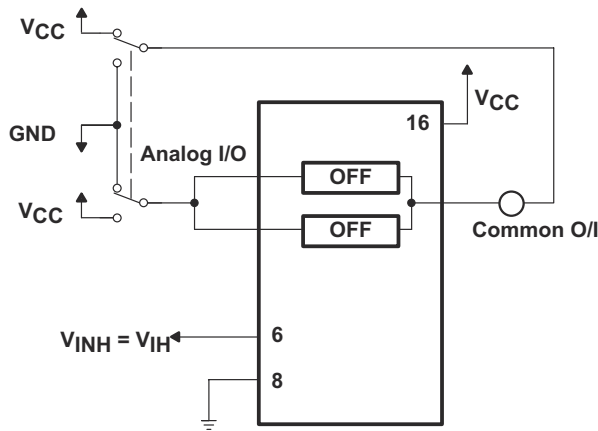


图 6-3. Maximum Off-Channel Leakage Current, Common Channel, Test Setup

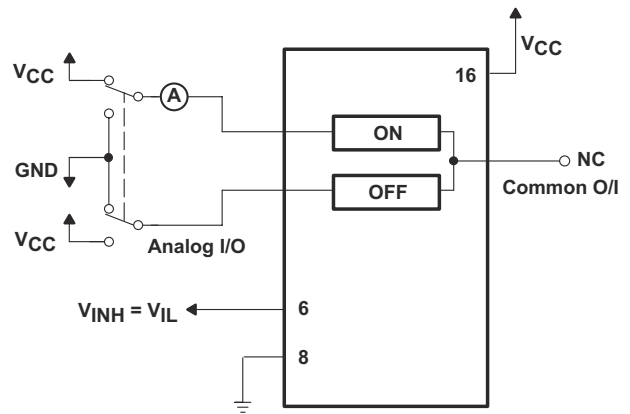


图 6-4. Maximum On-Channel Leakage Current, Channel To Channel, Test Setup

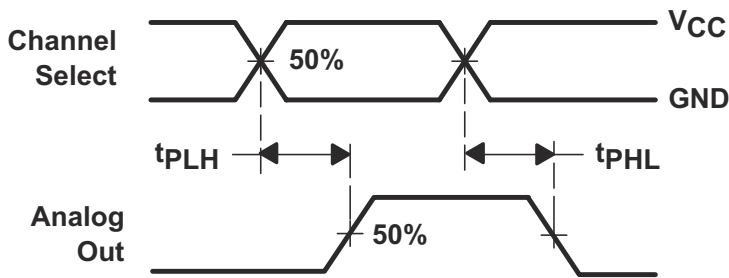
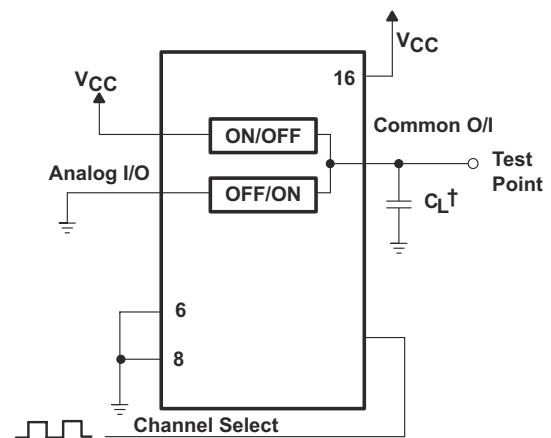


图 6-5. Propagation Delays, Channel Select to Analog Out



† Includes all probe and jig capacitance

图 6-6. Propagation-Delay Test Setup, Channel Select to Analog Out

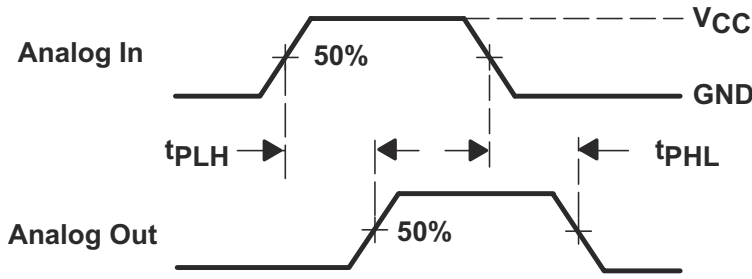
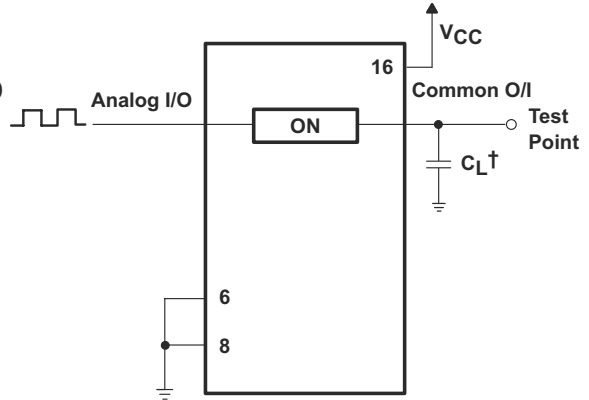


图 6-7. Propagation Delays, Analog In to Analog Out



† Includes all probe and jig capacitance

图 6-8. Propagation-Delay Test Setup, Analog In to Analog Out

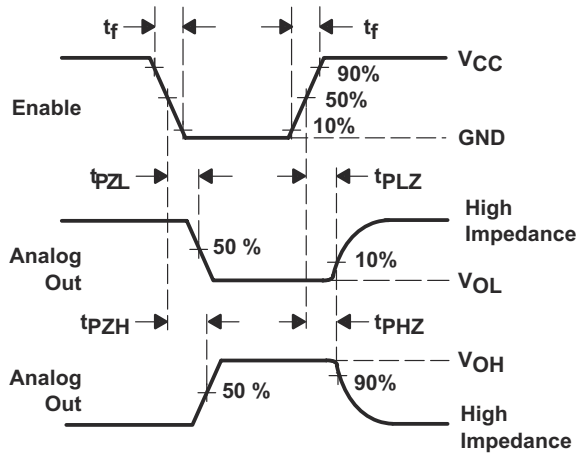


图 6-9. Propagation Delays, Enable to Analog Out

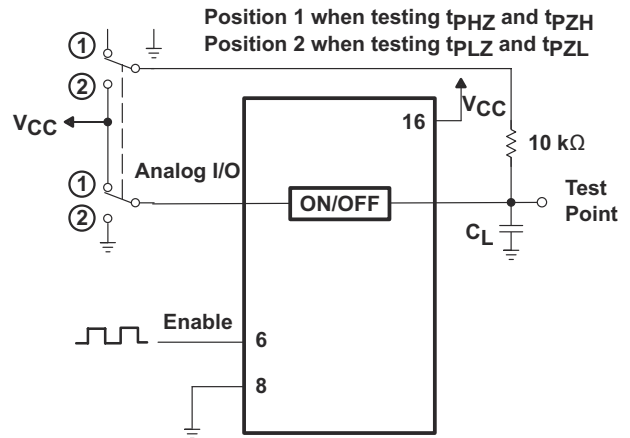


图 6-10. Propagation-Delay Test Setup, Enable to Analog Out

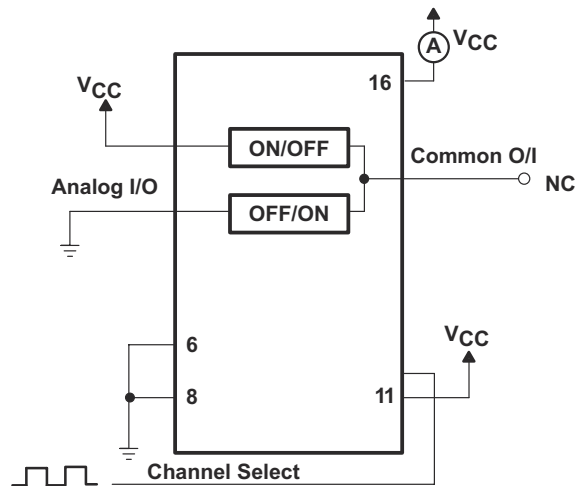


图 6-11. Power-Dissipation Capacitance Test Setup



## 7 Detailed Description

### 7.1 Functional Block Diagram

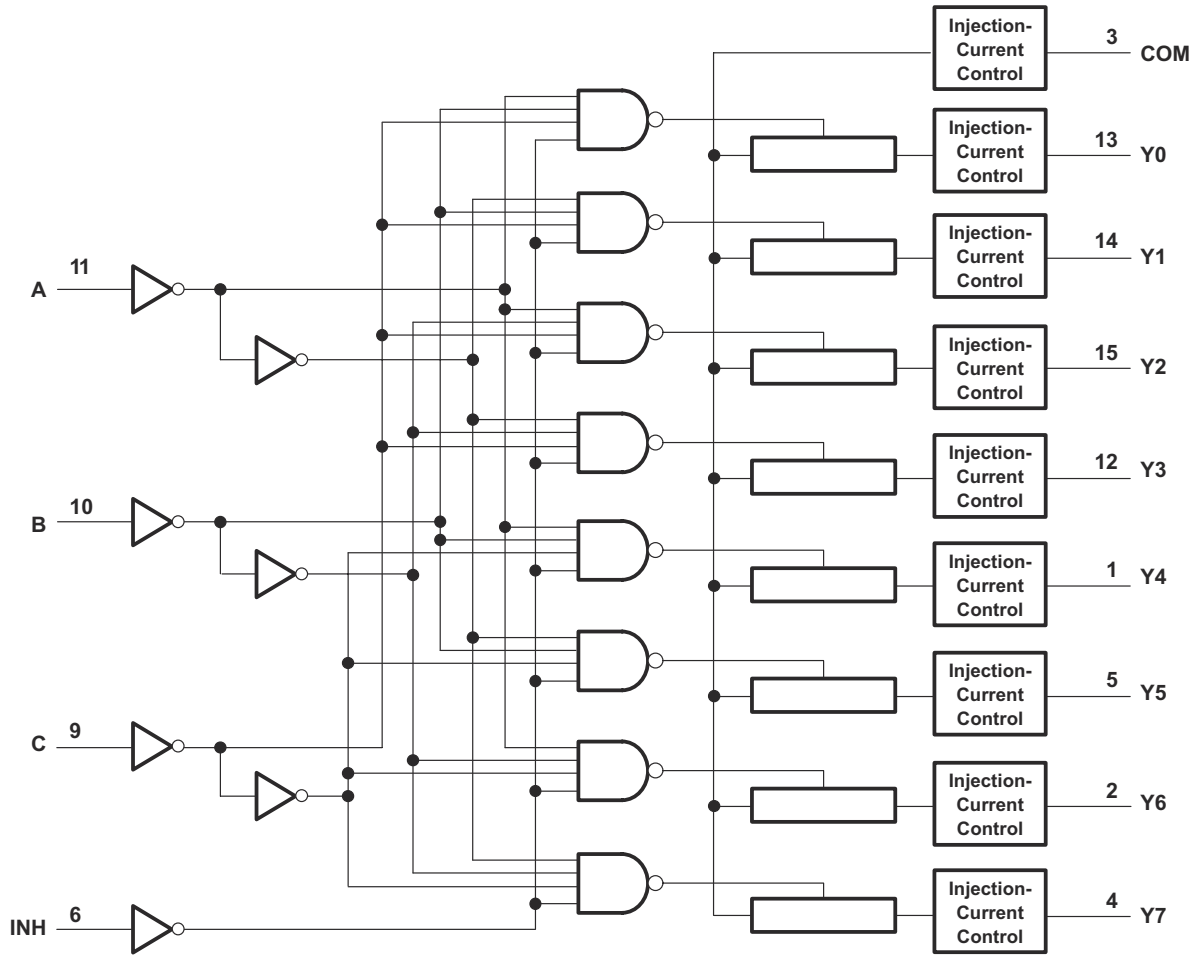


图 7-1. Logic Diagram (Positive Logic)

## 8 Application and Implementation

### 备注

以下应用部分中的信息不属于 TI 元件规格，TI 不承担其准确性和完整性。TI 的客户负责确定元件是否适合其用途，以及验证和测试其设计实现以确认系统功能。

### 8.1 Application Information

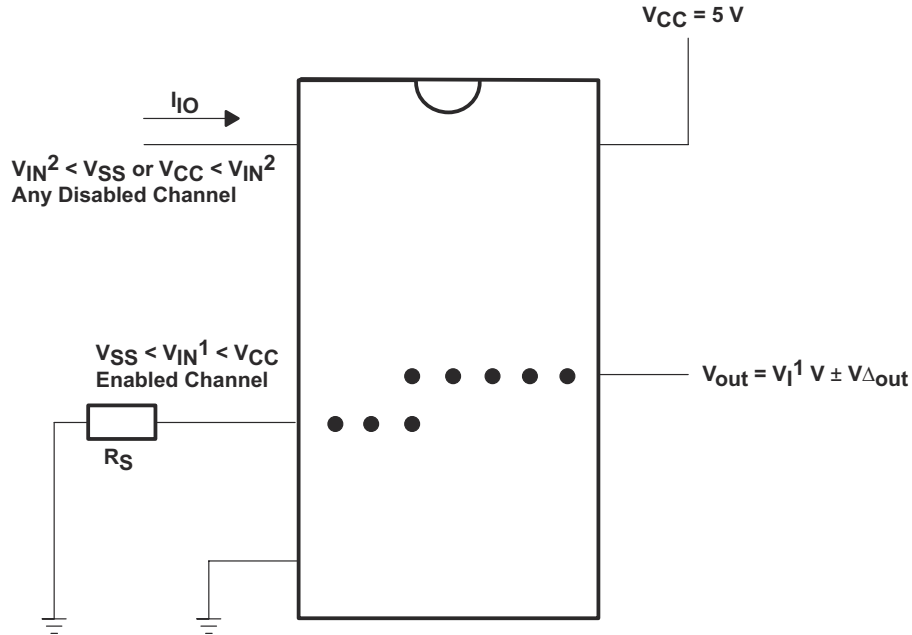


图 8-1. Injection-Current Coupling Specification

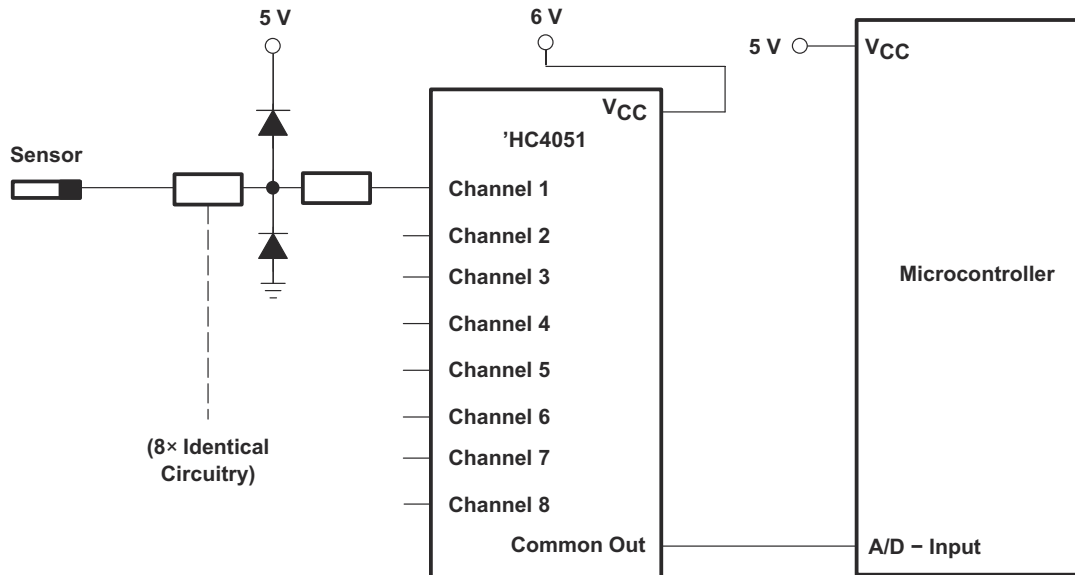


图 8-2. Alternate Solution Requires 32 Passive Components and One Extra 6-V Regulator to Suppress Injection Current Into a Standard ' HC4051 Multiplexer

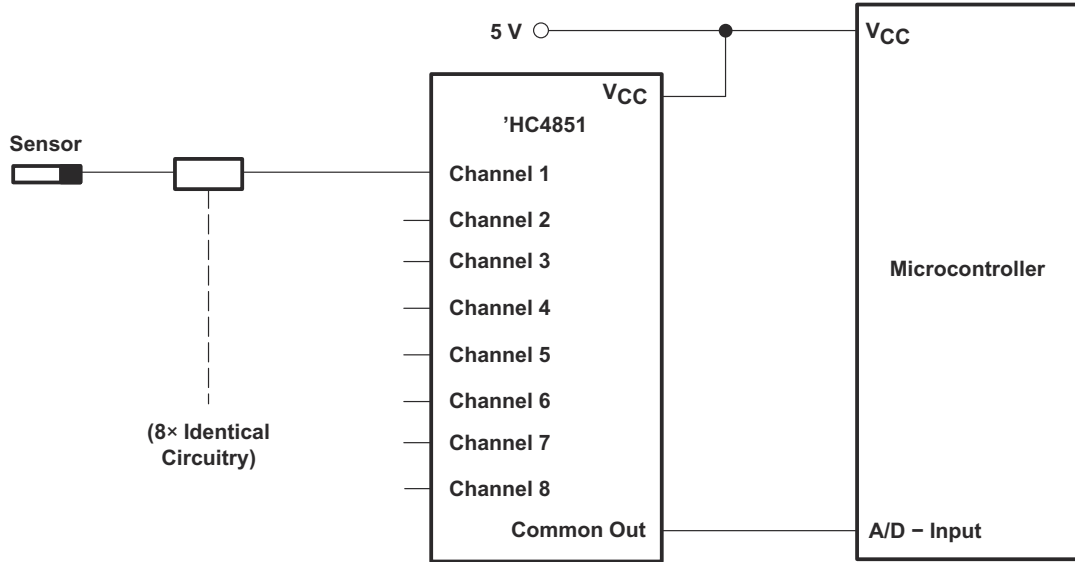


图 8-3. Solution by Applying the ' HC4851 Multiplexer

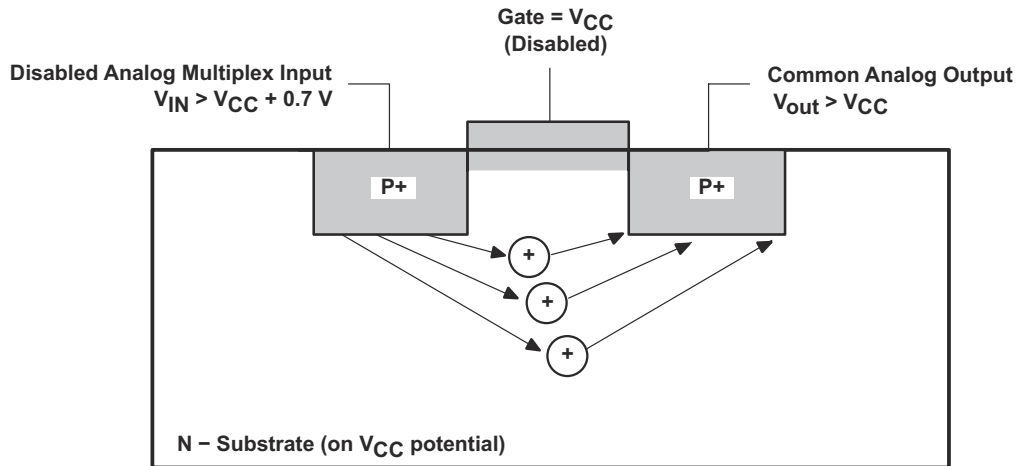


图 8-4. Diagram of Bipolar Coupling Mechanism (Appears if  $V_{IN}$  Exceeds  $V_{CC}$ , Driving Injection Current Into the Substrate)

## 9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 9.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 9.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

### 9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

### 9.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 9.5 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

## 10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (October 2012) to Revision D (June 2024)	Page
• 通篇更新了表格、图和交叉参考的编号格式.....	1
• Changed VCC ABS Max from 7V to 6V.....	3
• Changed R <sup>θ</sup> JA.....	3
• Recommended supply changed from 6V to 5.5V and all test conditions using 6V were removed.....	4
• Changed ttran, tON, tOFF parameters.....	6

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HC4851QDRG4Q1	NRND	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4851Q	
SN74HC4851QDRQ1	NRND	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4851Q	
SN74HC4851QPWRG4Q1	NRND	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4851Q	
SN74HC4851QPWRQ1	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4851Q	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN74HC4851-Q1 :**

- Catalog : [SN74HC4851](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC4851QPWRG4Q1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC4851QPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

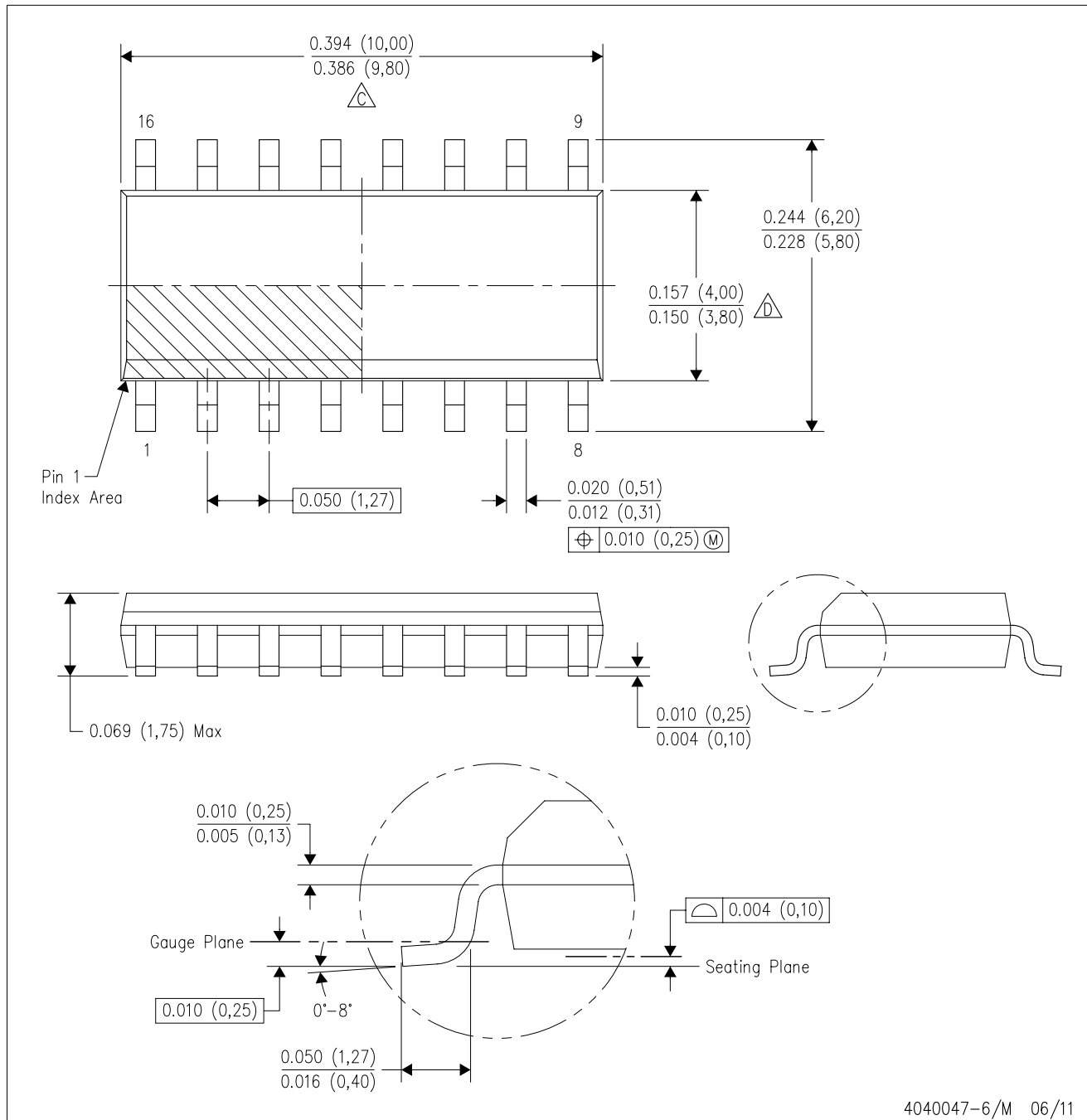

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC4851QPWRG4Q1	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74HC4851QPWRQ1	TSSOP	PW	16	2000	356.0	356.0	35.0



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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