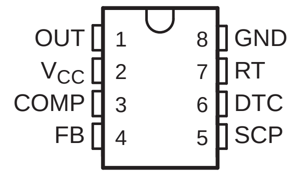
PULSE-WIDTH-MODULATION CONTROL CIRCUITS

FEATURES

- **Qualified for Automotive Applications**
- **Complete PWM Power Control**
- **3.6-V to 40-V Operation**
- **Internal Undervoltage-Lockout Circuit**
- **Internal Short-Circuit Protection**
- **Oscillator Frequency: 20 kHz to 500 kHz**
- **Variable Dead Time Provides Control Over Total Range**
- **±3% Tolerance on Reference Voltage**
- **Available in Q-Temperature Automotive**
  - **High-Reliability Automotive Applications**
  - **Configuration Control / Print Support**
  - **Qualification to Automotive Standards**

D PACKAGE
(TOP VIEW)



DESCRIPTION

The TL5001A incorporates on a single monolithic chip all the functions required for a pulse-width-modulation (PWM) control circuit. Designed primarily for power-supply control, the TL5001A contains an error amplifier, a regulator, an oscillator, a PWM comparator with a dead-time-control input, undervoltage lockout (UVLO), short-circuit protection (SCP), and an open-collector output transistor. The TL5001A has a typical reference voltage tolerance of ±3%.

The error-amplifier common-mode voltage ranges from 0 V to 1.5 V. The noninverting input of the error amplifier is connected to a 1-V reference. Dead-time control (DTC) can be set to provide 0% to 100% dead time by connecting an external resistor between DTC and GND. The oscillator frequency is set by terminating RT with an external resistor to GND. During low V_{CC} conditions, the UVLO circuit turns the output off until V_{CC} recovers to its normal operating range.

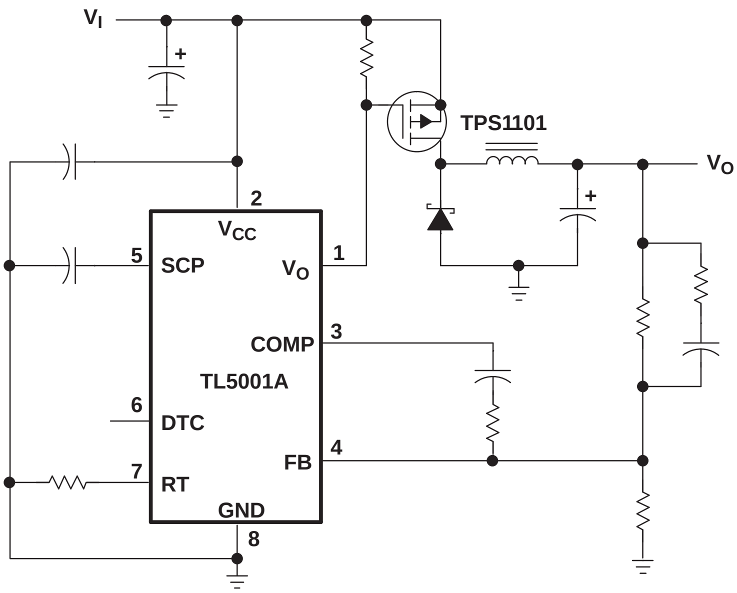
The TL5001A is characterized for operation from –40°C to 125°C.

AVAILABLE OPTIONS(1)

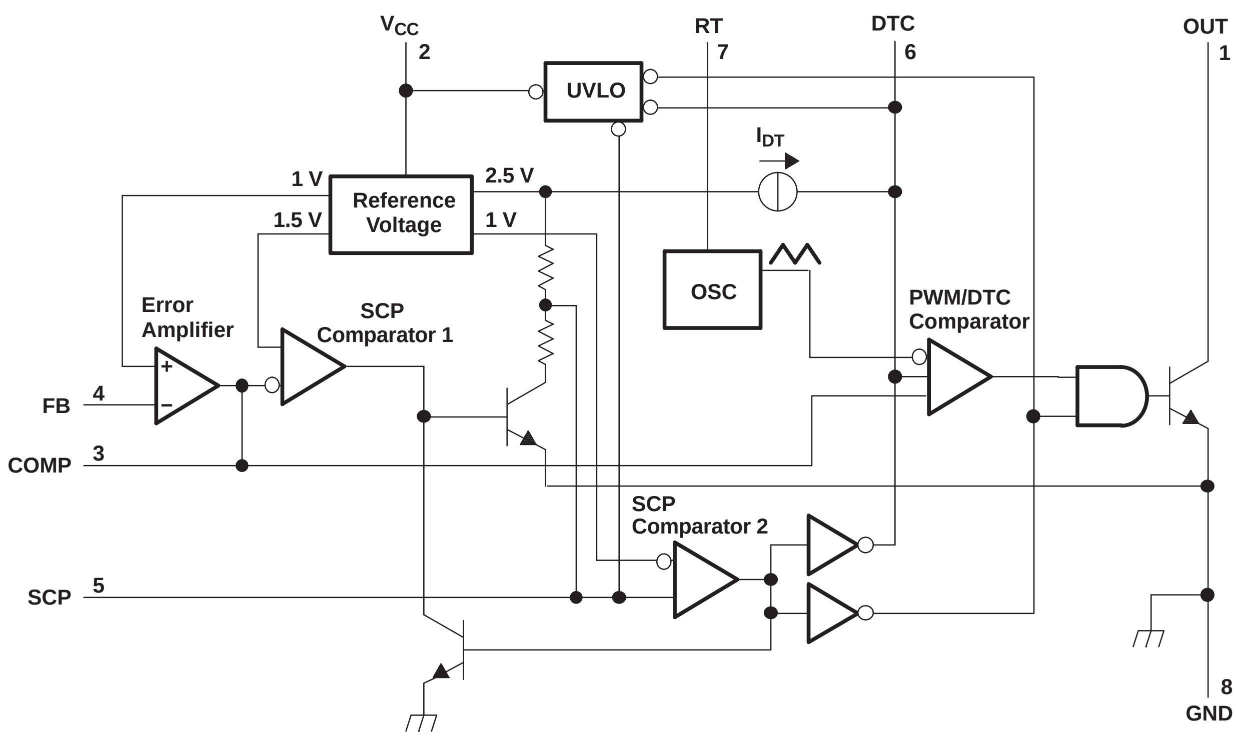
T_A	PACKAGED DEVICES(2)
	SMALL OUTLINE (D)(3)
–40°C to 125°C	TL5001AQDRQ1

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) The D package is available taped and reeled. Add the suffix R to the device type (e.g., TL5001ADR).

SCHEMATIC FOR TYPICAL APPLICATION



FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

VOLTAGE REFERENCE

A 2.5-V regulator operating from V_{CC} is used to power the internal circuitry of the TL5001A and as a reference for the error amplifier and SCP circuits. A resistive divider provides a 1-V reference for the error amplifier noninverting input which typically is within 2% of nominal over the operating temperature range.

ERROR AMPLIFIER

The error amplifier compares a sample of the dc-to-dc converter output voltage to the 1-V reference and generates an error signal for the PWM comparator. The dc-to-dc converter output voltage is set by selecting the error-amplifier gain (see Figure 1), using the following expression:

V_O = (1 + R1/R2) (1 V)

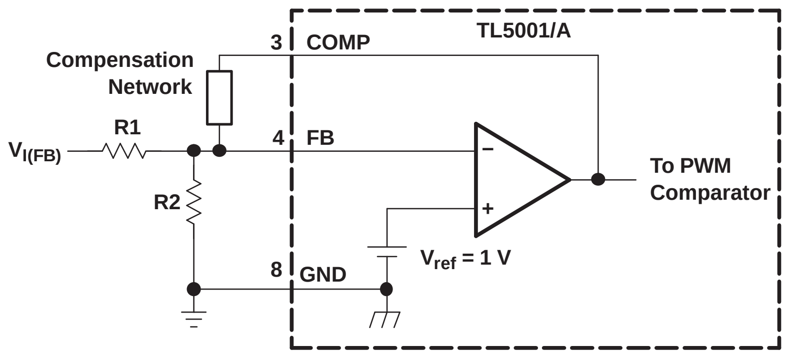


Figure 1. Error-Amplifier Gain Setting

The error-amplifier output is brought out as COMP for use in compensating the dc-to-dc converter control loop for stability. Because the amplifier can only source 45 µA, the total dc-load resistance should be 100 kΩ or more.

OSCILLATOR/PWM

The oscillator frequency (f_{osc}) can be set between 20 kHz and 500 kHz by connecting a resistor between RT and GND. Acceptable resistor values range from 15 kΩ to 250 kΩ. The oscillator frequency can be determined by using the graph shown in Figure 5.

The oscillator output is a triangular wave with a minimum value of approximately 0.7 V and a maximum value of approximately 1.3 V. The PWM comparator compares the error-amplifier output voltage and the DTC input voltage to the triangular wave and turns the output transistor off whenever the triangular wave is greater than the lesser of the two inputs.

DEAD-TIME CONTROL (DTC)

DTC provides a means of limiting the output-switch duty cycle to a value less than 100%, which is critical for boost and flyback converters. A current source generates a reference current (I_{DT}) at DTC that is nominally equal to the current at the oscillator timing terminal (RT). Connecting a resistor between DTC and GND generates a dead-time reference voltage (V_{DT}), which the PWM/DTC comparator compares to the oscillator triangle wave as described in the previous section. Nominally, the maximum duty cycle is 0% when VDT is 0.7 V or less and 100% when V_{DT} is 1.3 V or greater. Because the triangle wave amplitude is a function of frequency and the source impedance of RT is relatively high (1250 Ω), choosing R_{DT} for a specific maximum duty cycle (D) is accomplished using the following equation and the voltage limits for the frequency in question as found in Figure 11 (V_{osc}max and V_{osc}min are the maximum and minimum oscillator levels):

$$R_{DT} = \frac{(R_t + 1250)\,[D(V_{osc}\,max - V_{osc}\,min) + V_{osc}\,min]}{V_{RT}} \quad ; \quad V_{RT} = 1\ V \tag{1}$$

Where

R_{DT} and R_t are in Ω, D is in decimal

Soft start can be implemented by paralleling the DTC resistor with a capacitor (C_{DT}) as shown in Figure 2. During soft start, the voltage at DTC is derived by the following equation:

$$V_{DT} \approx I_{DT} R_{DT} \left(1 - e^{-\frac{t}{R_{DT} C_{DT}}} \right) \quad (2)$$

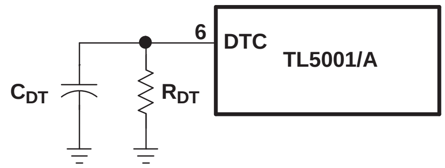


Figure 2. Soft-Start Circuit

If the dc-to-dc converter must be in regulation within a specified period of time, the time constant ($R_{DT}C_{DT}$) should be $t_0/3$ to $t_0/5$. The TL5001A remains off until $V_{DT} \approx 0.7$ V, the minimum ramp value. C_{DT} is discharged every time UVLO or SCP becomes active.

UNDERVOLTAGE-LOCKOUT (UVLO) PROTECTION

The undervoltage-lockout circuit turns the output transistor off and resets the SCP latch whenever the supply voltage drops too low (approximately 3 V at 25°C) for proper operation. A hysteresis voltage of 200 mV eliminates false triggering on noise and chattering.

SHORT-CIRCUIT PROTECTION (SCP)

The TL5001A includes short-circuit protection (see Figure 3), which turns the power switch off to prevent damage when the converter output is shorted. When activated, the SCP prevents the switch from being turned on until the internal latching circuit is reset. The circuit is reset by reducing the input voltage until UVLO becomes active or until the SCP terminal is pulled to ground externally.

When a short circuit occurs, the error-amplifier output at COMP rises to increase the power-switch duty cycle in an attempt to maintain the output voltage. SCP comparator 1 starts an RC timing circuit when COMP exceeds 1.5 V. If the short is removed and the error-amplifier output drops below 1.5 V before time out, normal converter operation continues. If the fault is still present at the end of the time-out period, the timer sets the latching circuit and turns off the TL5001/A output transistor.

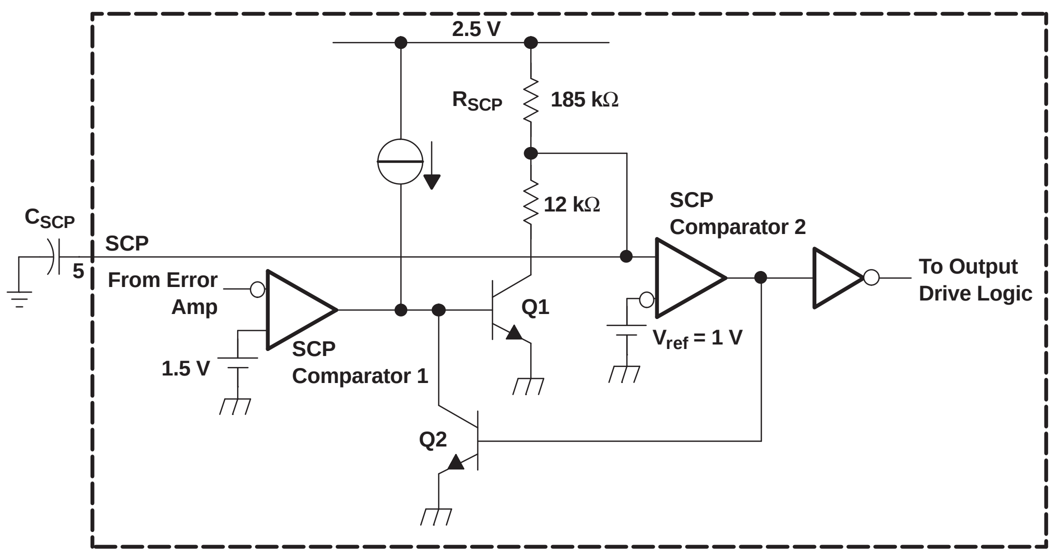


Figure 3. SCP Circuit

The timer operates by charging an external capacitor (C_{SCP}) connected between the SCP terminal and ground, towards 2.5 V through a 185-kΩ resistor (R_{SCP}). The circuit begins charging from an initial voltage of approximately 185 mV and times out when the capacitor voltage reaches 1 V. The output of SCP comparator 2 then goes high, turns on Q2, and latches the timer circuit. The expression for setting the SCP time period is derived from Equation 3:

$$V_{SCP} = (2.5 - 0.185)\,(1 - e^{-t/\tau}) + 0.185 \tag{3}$$

Where

$\tau = R_{SCP}C_{SCP}$

The end of the time-out period (t_{SCP}) occurs when V_{SCP} = 1 V. Solving for C_{SCP} yields Equation 4:

$$C_{SCP} = 12.46 \times t_{SCP} \tag{4}$$

Where

t is in seconds, C is in µF

t_{SCP} must be much longer (generally 10 to 15 times) than the converter start-up period, or the converter will not start.

OUTPUT TRANSISTOR

The output of the TL5001A is an open-collector transistor with a maximum collector current rating of 21 mA and a voltage rating of 51 V. The output is turned on under the following conditions: the oscillator triangle wave is lower than both the DTC voltage and the error-amplifier output voltage, the UVLO circuit is inactive, and the short-circuit protection circuit is inactive.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

V_{CC}	Supply voltage (2)	41 V
$V_{I(FB)}$	Amplifier input voltage	20 V
V_O	Output voltage, OUT	51 V
I_O	Output current, OUT	21 mA
$I_{O(peak)}$	Output peak current, OUT	100 mA
	Continuous total power dissipation	See *Dissipation Rating*
T_A	Operating ambient temperature range, TL5001AQDRQ1	–40°C to 125°C
T_{stg}	Storage temperature range	–65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

DISSIPATION RATINGS

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	145 mW

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3.6	40	V
$V_{I(FB)}$	Amplifier input voltage		0	1.5	V
V_O	Output voltage, OUT			50	V
I_O	Output current, OUT			20	mA
	COMP source current			45	µA
	COMP dc load resistance		100		kΩ
R_t	Oscillator timing resistor		15	250	kΩ
f_{OSC}	Oscillator frequency		20	500	kHz
T_A	Operating ambient temperature	TL5001AQDRQ1	–40	125	°C

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 6 V, f_{osc} = 100 kHz (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TL5001AQ MIN	TL5001AQ TYP(1)	TL5001AQ MAX	UNIT
REFERENCE						
Output voltage	T_A = 25°C	COMP connected to FB	0.97	1	1.03	V
	T_A = MIN to MAX		0.94	0.98	1.06	
Input regulation	T_A = MIN to MAX,	VCC = 3.6 V to 40 V		2	12.5	mV
Output voltage change with temperature	T_A = MIN to MAX		–6%(2)	2%	6%(2)	
UNDERVOLTAGE LOCKOUT						
Upper threshold voltage	T_A = MIN, 25°C			3		V
	T_A = MAX			2.55		
Lower threshold voltage	T_A = MIN, 25°C			2.8		V
	T_A = MAX			2.0		
Hysteresis	T_A = MIN to MAX		80	200		mV
Reset threshold voltage	T_A = MIN, 25°C		2.1	2.55		V
	T_A = MAX		0.35	0.63		
SHORT-CIRCUIT PROTECTION						
SCP threshold voltage	T_A = MIN, 25°C		0.97	1	1.03	V
	T_A = MAX		0.94	0.98	1.06	
SCP voltage, latched	T_A = MIN to MAX	No pullup	140	185	230	mV
SCP voltage, UVLO standby	T_A = MIN to MAX	No pullup		60	120	mV
Equivalent timing resistance	T_A = MIN to MAX			185		kΩ
SCP comparator 1 threshold voltage	T_A = MIN to MAX			1.5		V
OSCILLATOR						
Frequency	T_A = MIN to MAX	R_t = 100 kΩ		100		kHz
Standard deviation of frequency	T_A = MIN to MAX			2		kHz
Frequency change with voltage	T_A = MIN to MAX	V_{CC} = 3.6 V to 40 V		1		kHz
Frequency change with temperature	T_A = MIN to MAX	Q suffix	–9(2)	5	9(2)	kHz
		M suffix	–9(2)	5	9(2)	
Voltage at RT	T_A = MIN to MAX			1		V
DEAD-TIME CONTROL						
Output (source) current	T_A = MIN to MAX	$V_{(DT)}$ = 1.5 V	0.9 × I_{RT}(3)		1.1 × I_{RT}(3)	µA
Input threshold voltage	T_A = 25°C	Duty cycle 0%	0.5	0.7		V
		Duty cycle 100%		1.3	1.5	
	T_A = MIN to MAX	Duty cycle 0%	0.4	0.7		
		Duty cycle 100%		1.3	1.7	

(1) All typical values are at T_A = 25°C.
(2) Not production tested.
(3) Output source current at RT

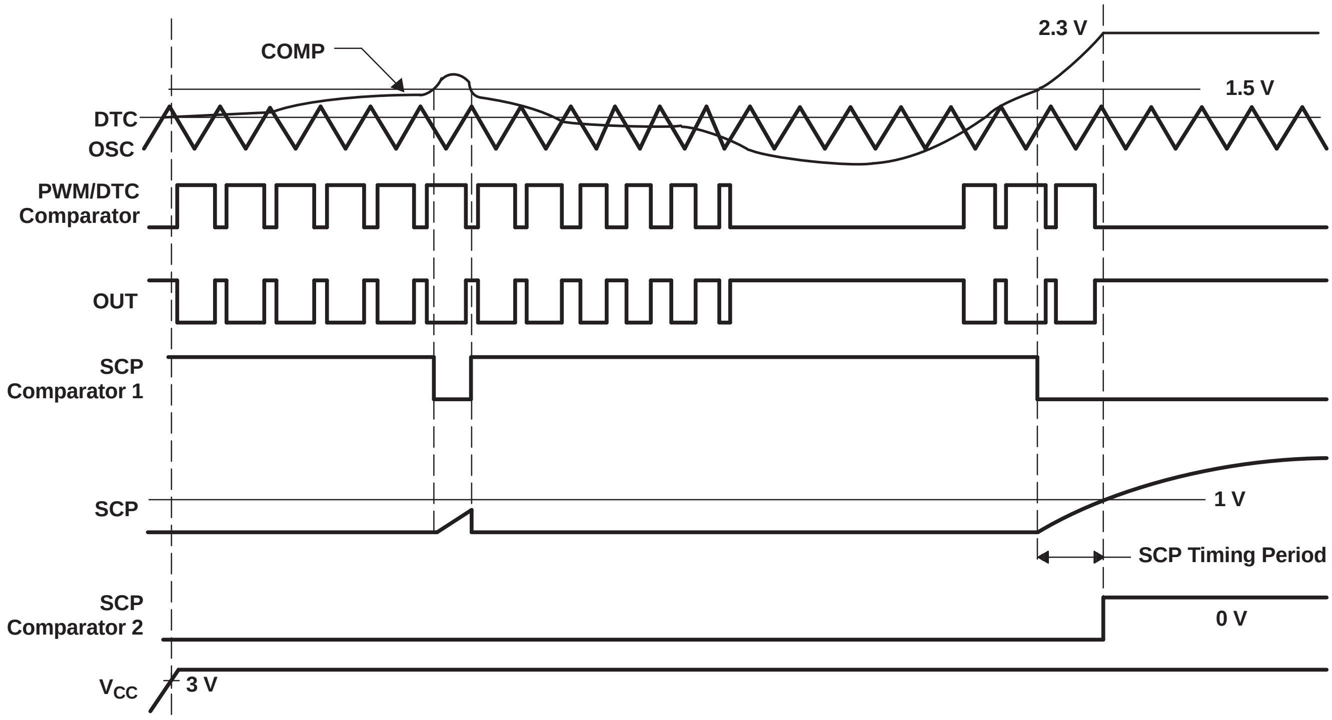
ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 6 V, f_{osc} = 100 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TL5001AQ MIN	TYP(1)	MAX	UNIT
ERROR AMPLIFIER							
Input bias current		T_A = MIN to MAX			–160	–500	nA
Output voltage swing	Positive	T_A = MIN to MAX		1.5	2.3		V
	Negative				0.3	0.4	V
Open-loop voltage amplification		T_A = MIN to MAX			80		dB
Unity gain bandwidth		T_A = MIN to MAX			1.5		MHz
Output (sink) current		T_A = MIN to MAX	$V_{I(FB)}$ = 1.2 V, COMP = 1 V	100	600		µA
Output (source) current		T_A = MIN, 25°C	$V_{I(FB)}$ = 0 V, COMP = 1 V	–45	–70		µA
		T_A = MAX		–30	–45		
OUTPUT							
Output saturation voltage		T_A = MIN to MAX	I_O = 10 mA		1.5	2	V
Off-state current		T_A = MIN to MAX	V_O = 50 V, V_{CC} = 0			10	µA
			V_O = 50 V			10	
Short-circuit output current		T_A = MIN to MAX	V_O = 6 V		40		mA
TOTAL DEVICE							
Standby supply current	Off state	T_A = MIN to MAX			1	1.5	mA
Average supply current		T_A = MIN to MAX	R_L = 100 kΩ		1.4	2.1	mA

(1) All typical values are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



A. The waveforms show timing characteristics for an intermittent short circuit and a longer short circuit that is sufficient to activate SCP.

Figure 4. PWM Timing Diagram

TYPICAL CHARACTERISTICS

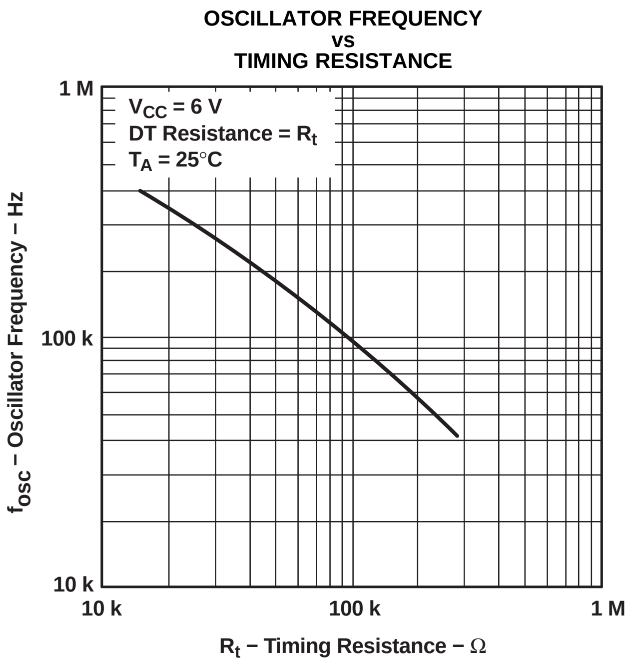


Figure 5.

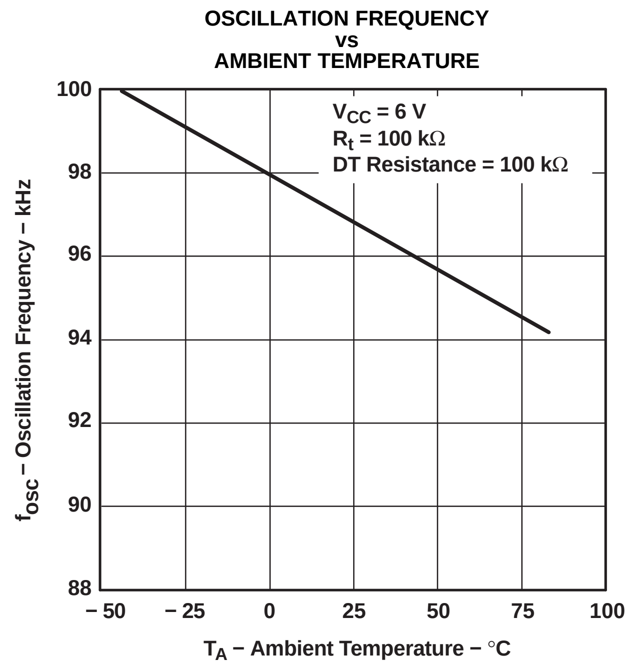


Figure 6.

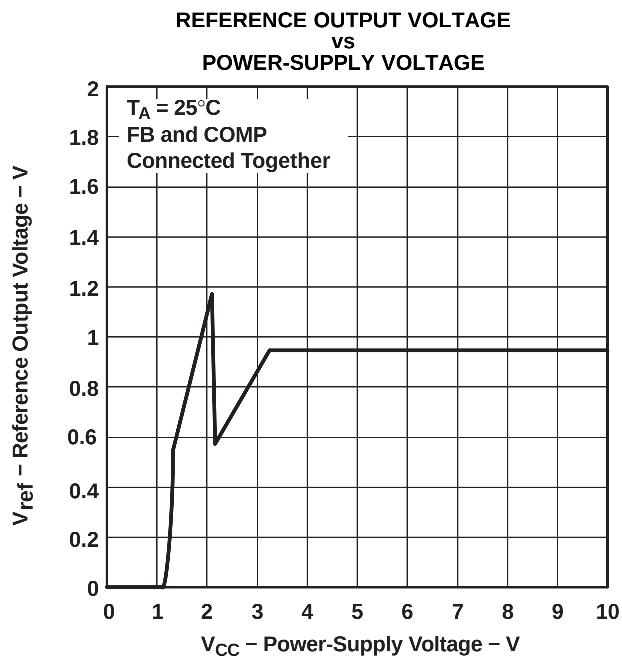


Figure 7.

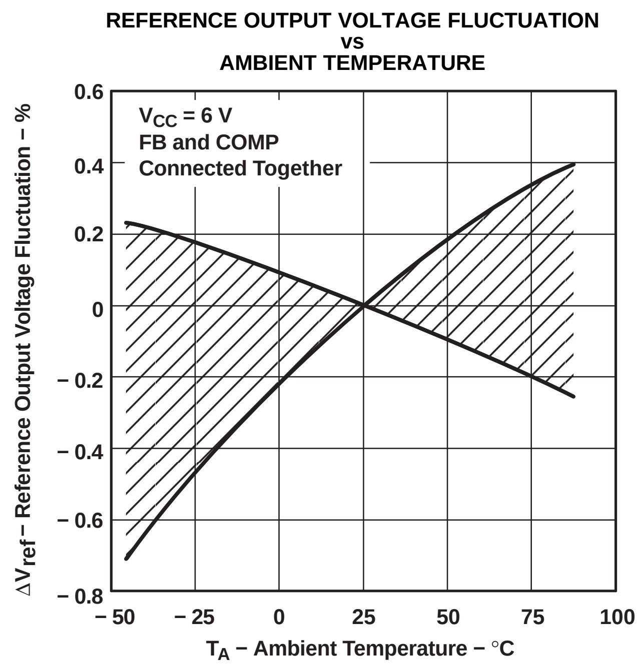


Figure 8.

TYPICAL CHARACTERISTICS (continued)

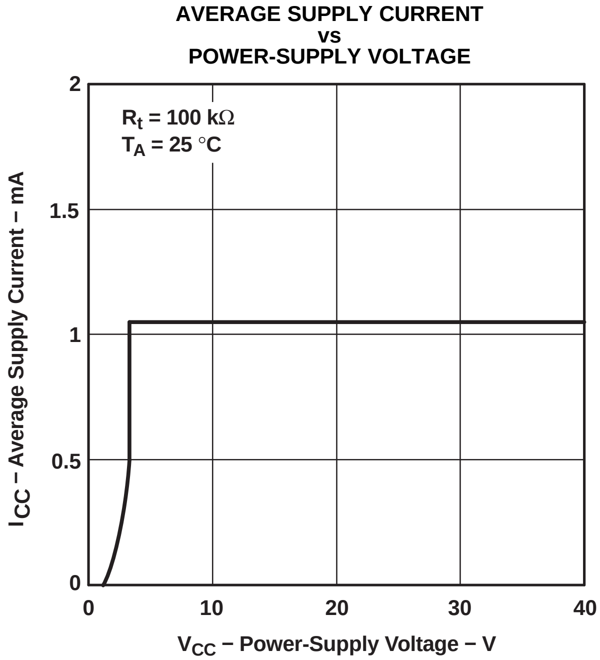


Figure 9.

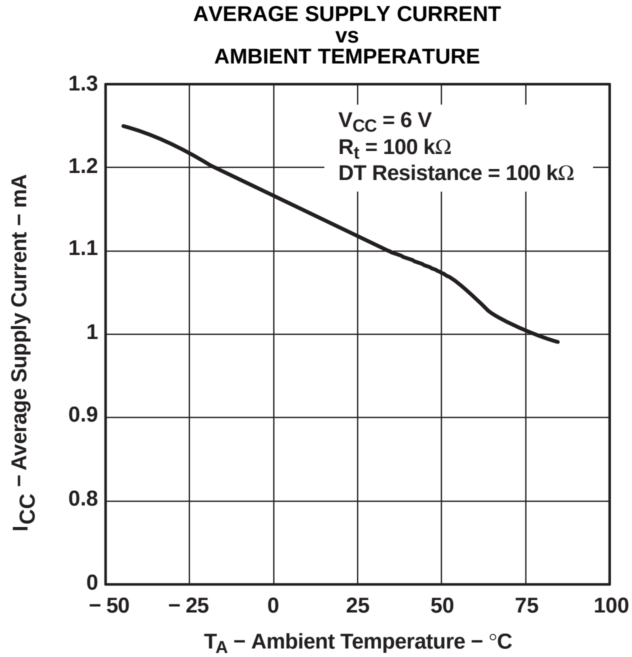


Figure 10.

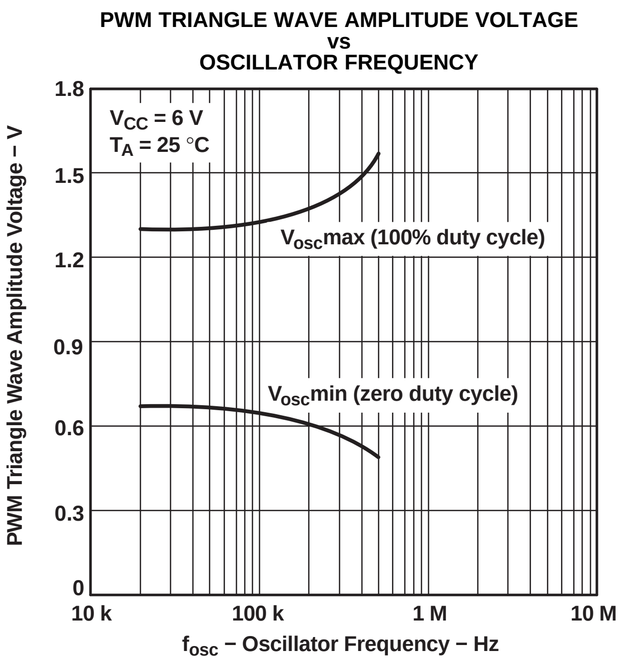


Figure 11.

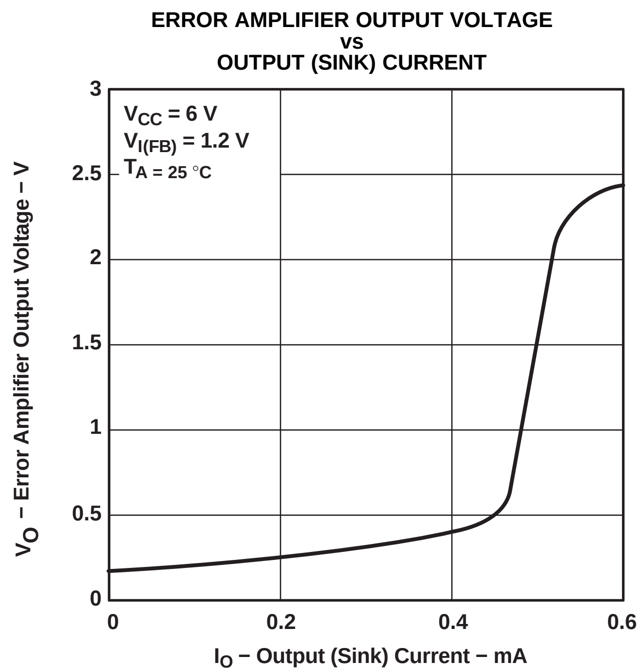
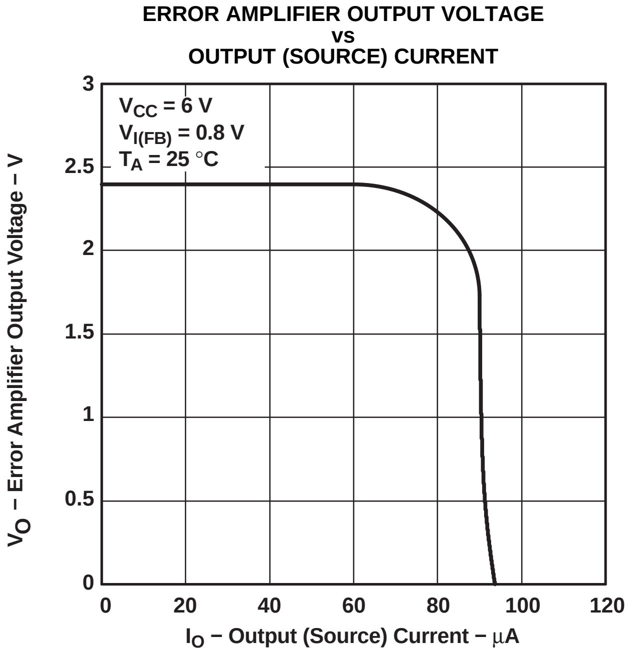


Figure 12.

TYPICAL CHARACTERISTICS (continued)



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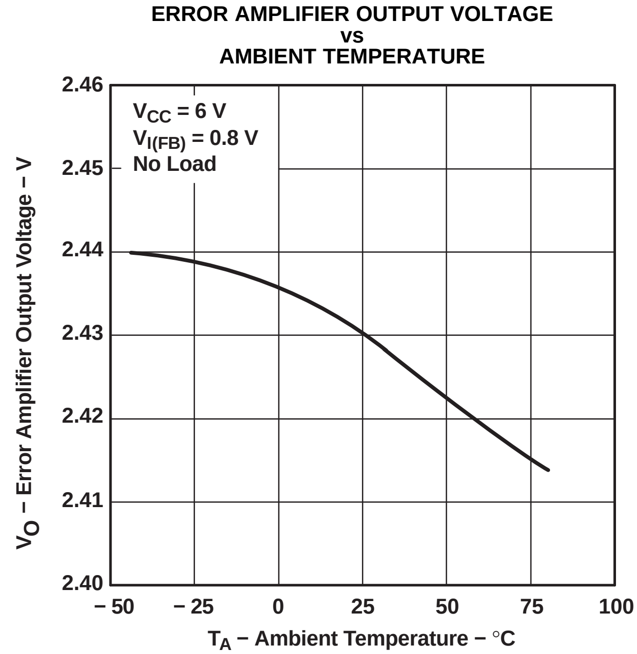

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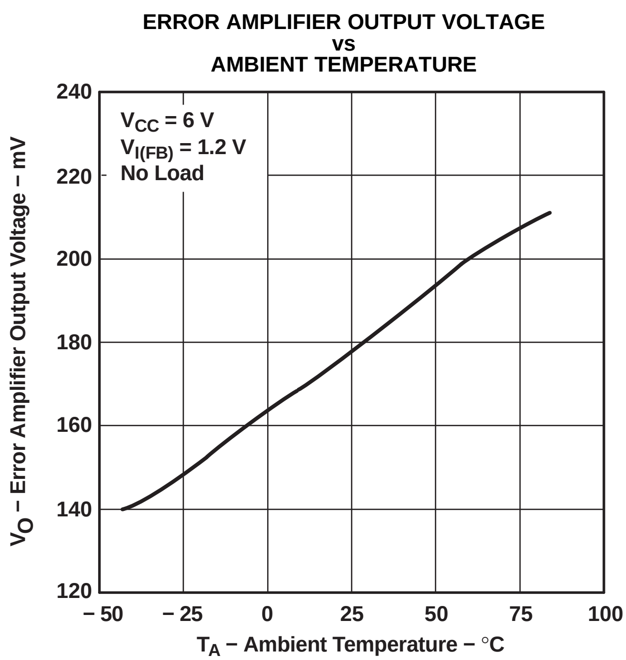


Figure 15.

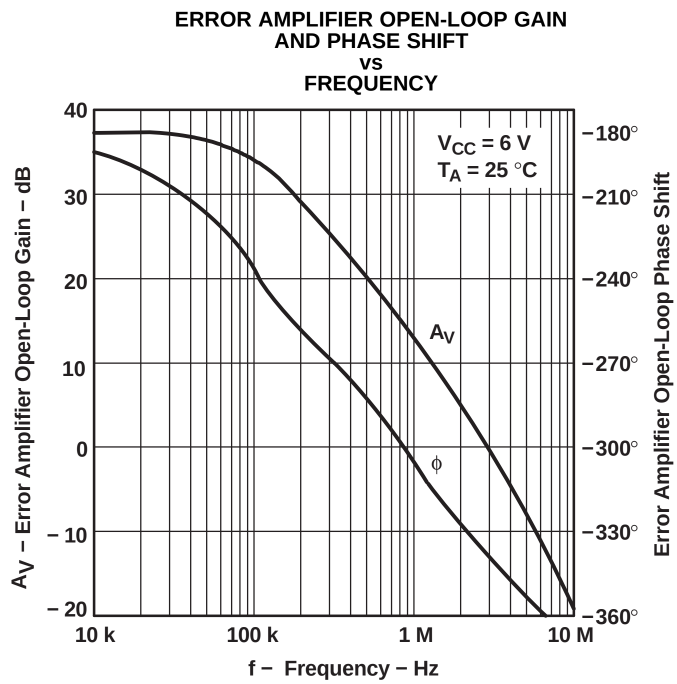


Figure 16.

TYPICAL CHARACTERISTICS (continued)

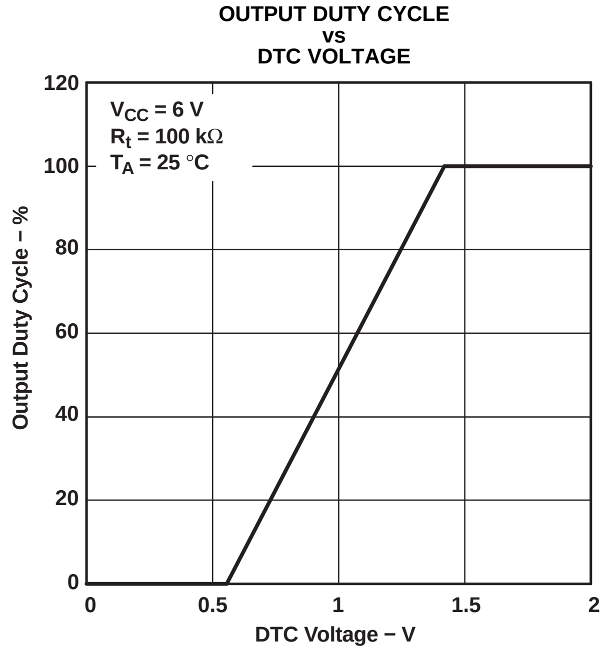


Figure 17.

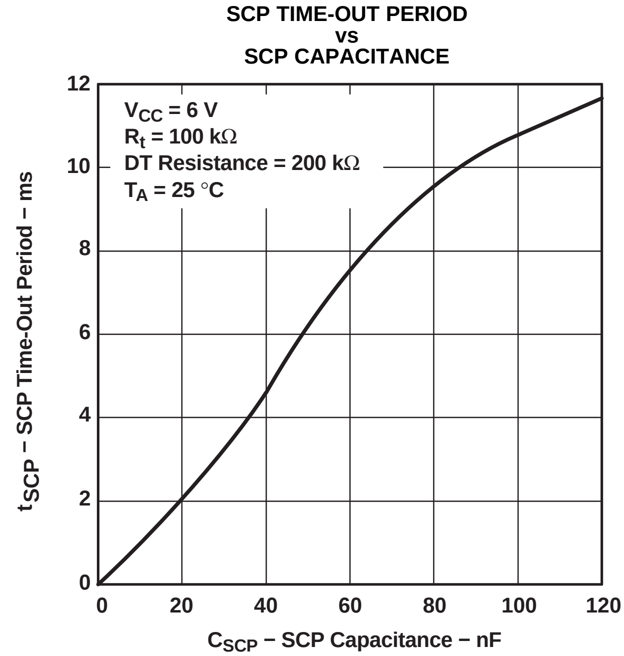


Figure 18.

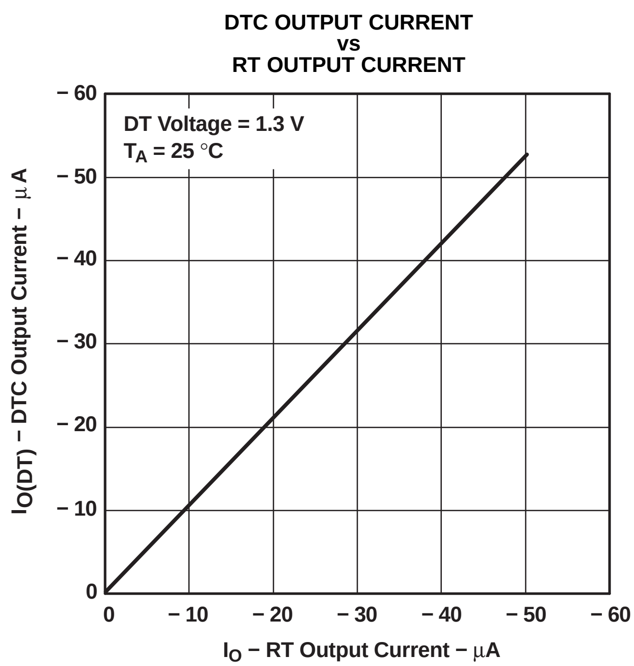


Figure 19.

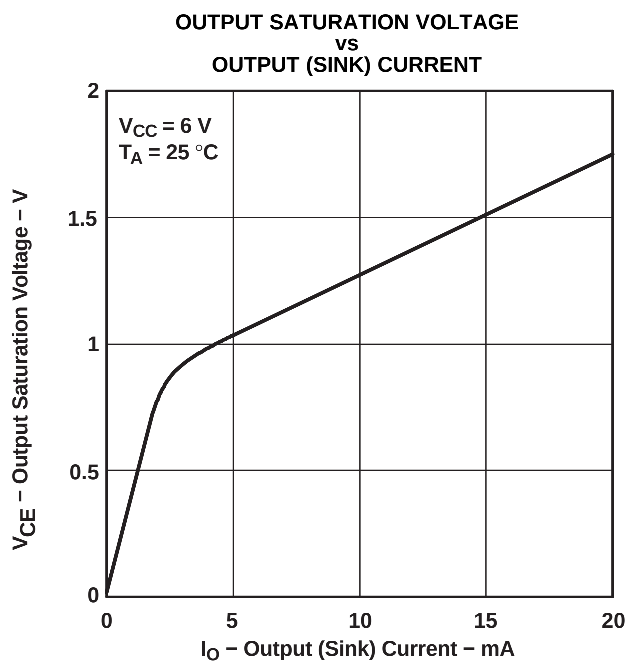
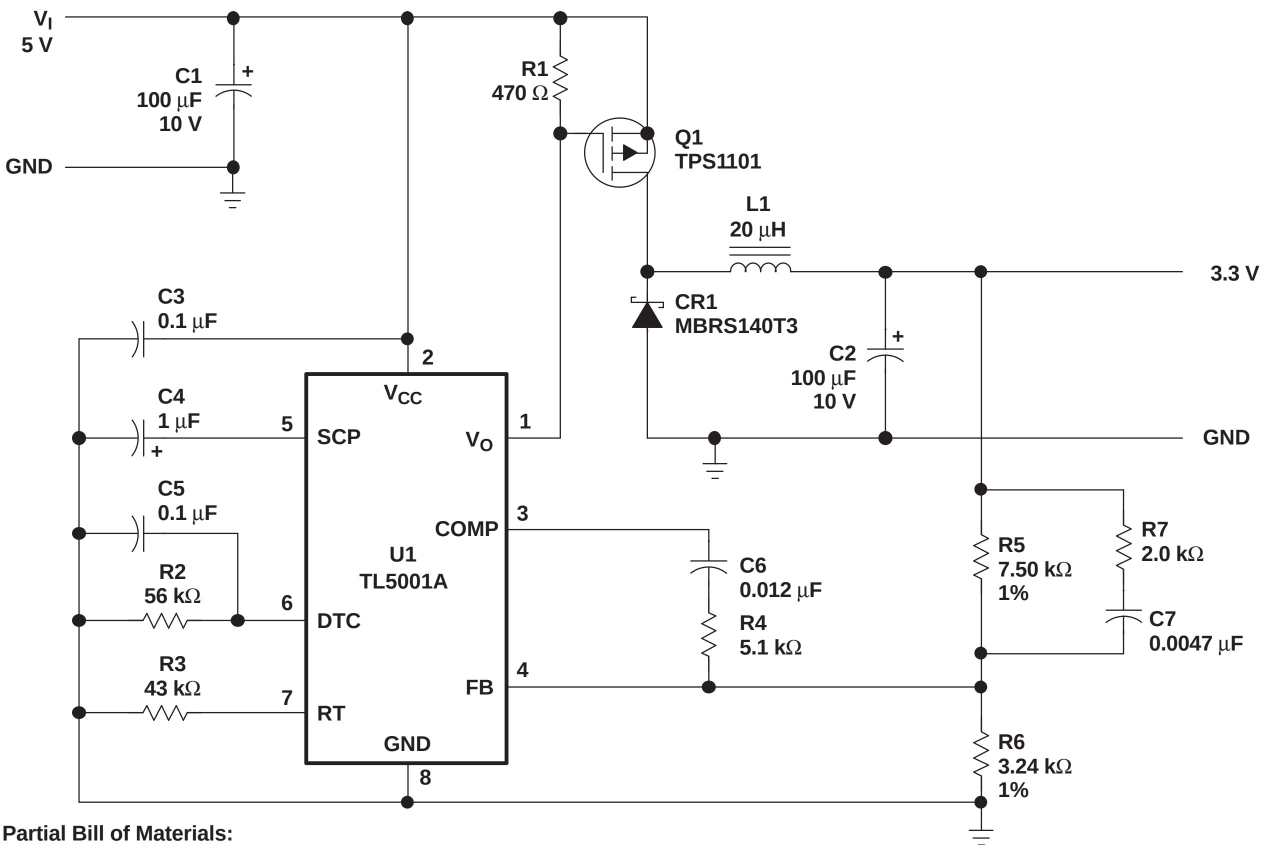


Figure 20.

APPLICATION INFORMATION



Partial Bill of Materials:

U1	**TL5001A**	**Texas Instruments**
Q1	**TPS1101**	**Texas Instruments**
LI	**CTX20-1 or 23 turns of #28 wire on Micrometals No. T50-26B core**	**Coiltronics**
C1	**TPSD107M010R0100**	**AVX**
C2	**TPSD107M010R0100**	**AVX**
CR1	**MBRS140T3**	**Motorola**

A. Frequency = 200 kHz

B. Duty cycle = 90% max

C. Soft-start time constant (TC) = 5.6 ms

D. SCP TC = 70 ms

Figure 21. Step Down Converter

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TL5001AQDRG4Q1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	501AQ1
TL5001AQDRG4Q1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	501AQ1
TL5001AQDRQ1	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	501AQ1
TL5001AQDRQ1.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	501AQ1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TL5001A-Q1 :

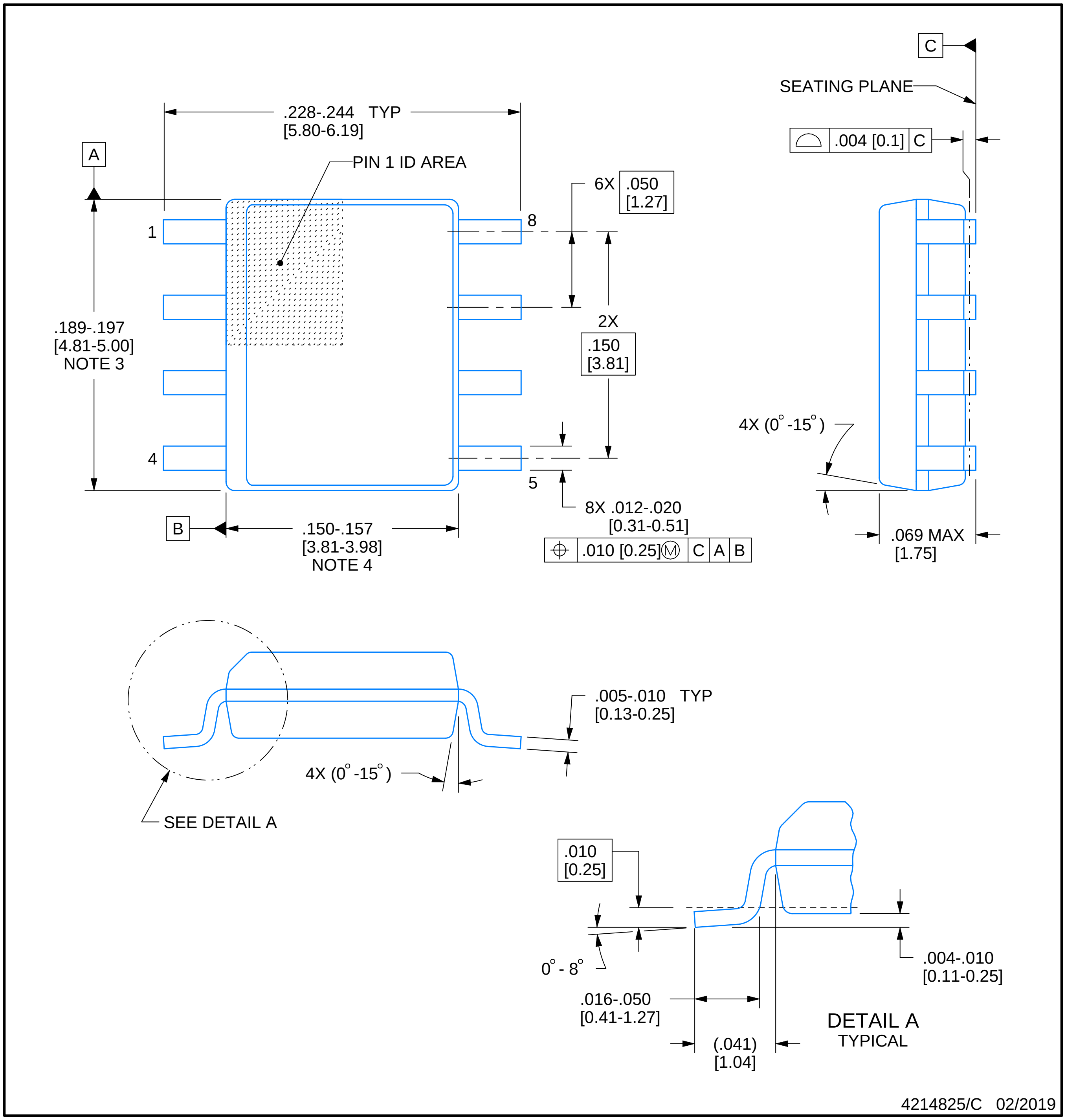
- Catalog : TL5001A

- Military : TL5001AM

NOTE: Qualified Version Definitions:

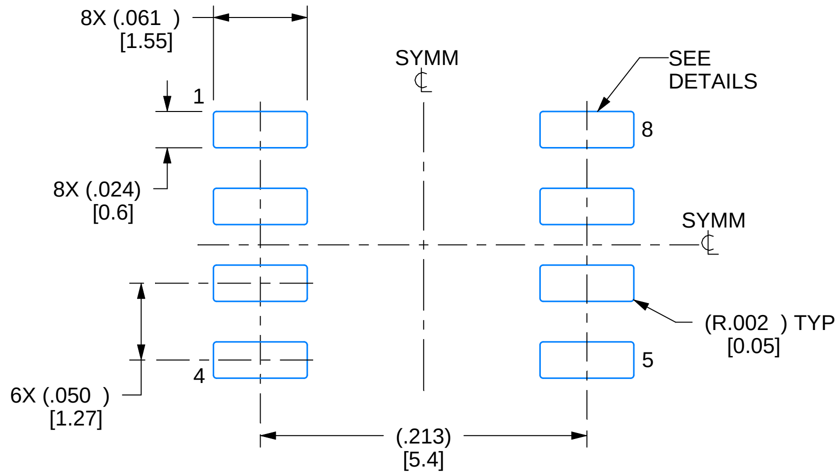
- Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

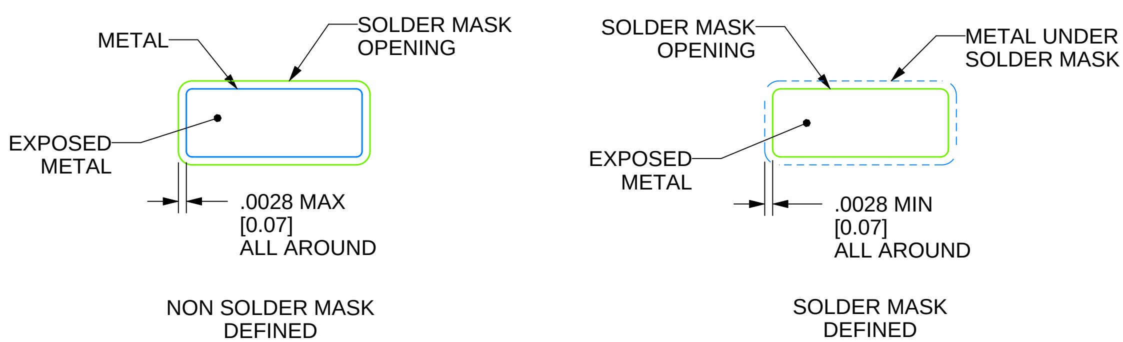


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

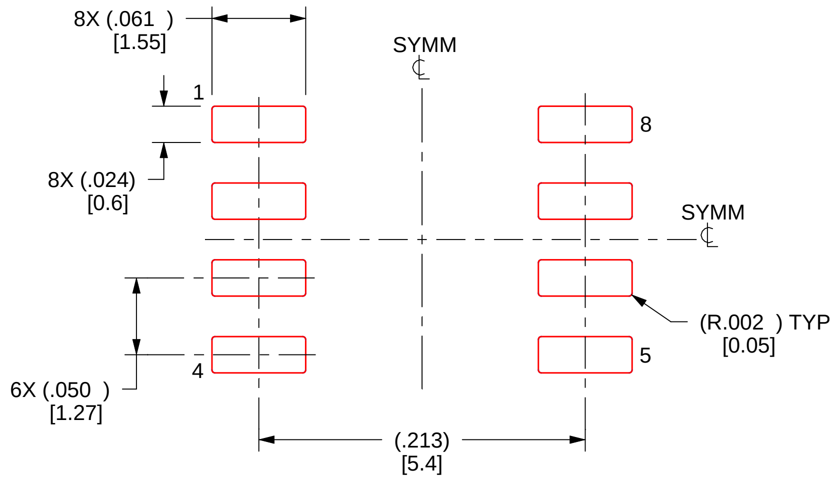


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.