TEXAS INSTRUMENTS
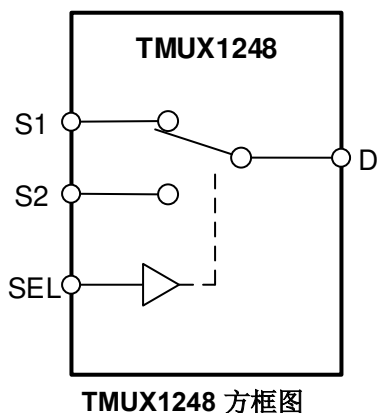
TMUX1248 采用 1.8V 逻辑的 3Ω 低 R$_{ON}$、5V、2:1 (SPDT) 通用开关

1 特性

- 轨至轨运行
- 双向信号路径
- 兼容 1.8V 逻辑电平
- 失效防护逻辑
- 控制输入过压容差：5.5V
- 低导通电阻：3Ω
- 宽电源电压范围：1.08V 至 5.5V
- 工作温度范围：-40°C 至 +125°C
- 低电源电流：7nA
- 先断后合开关

2 应用

- 模拟和数字开关
- I^{2}C 和 SPI 总线多路复用
- 机架式服务器
- 网络接口卡 (NIC)
- 条形码扫描仪
- 楼宇自动化
- 模拟输入模块
- 电机驱动器
- 视频监控
- 电子销售终端
- 台式机
- 电器

3 说明

TMUX1248 是一种通用 2:1 单极双投 (SPDT) 开关，支持 1.08V 至 5.5V 的宽工作范围。此器件在源极 (Sx) 和漏极 (D) 引脚上支持从 GND 到 V$_{DD}$ 的双向模拟和数字信号。选择引脚 (SEL) 的状态决定连接到漏极引脚的源极引脚。此外，TMUX1248 具有 7nA 的低电源电流，这使器件能够在许多手持设备或低功耗应用中使用。
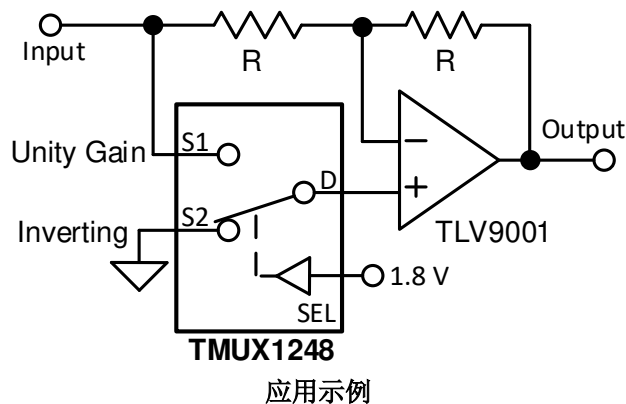
先断后合开关操作可防止同时启用两个源极引脚。此功能通过防止源极信号在开关事件期间短路，增加了系统的稳健性。

所有逻辑输入都具有兼容 1.8V 逻辑的阈值，允许使用低压逻辑信号进行操作。失效防护逻辑电路允许先在控制引脚上施加电压，然后在电源引脚上施加电压，或在电压高于电源引脚（最高为 5.5V）时施加电压，从而保护器件免受潜在的损害。

器件信息[(1)]

器件型号	封装	封装尺寸（标称值）
TMUX1248	SC70 (6)	2.00mm × 1.25mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。

TMUX1248 方框图

应用示例

English Data Sheet: SCDS447

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
July 2021	*	Initial Release

5 Pin Configuration and Functions
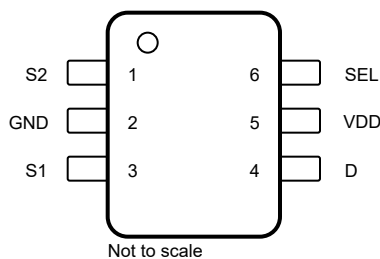
图 5-1. DCK Package 6-Pin SC70 Top View

表 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION[2]
NAME	NO.		
D	4	I/O	Drain pin. Can be an input or output.
GND	2	P	Ground (0 V) reference.
S1	3	I/O	Source pin 1. Can be an input or output.
S2	1	I/O	Source pin 2. Can be an input or output.
SEL	6	I	Select pin: controls state of the switch according to 表 8-1.
V_{DD}	5	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND.

(1)   I = input, O = output, I/O = input and output, P = power.
(2)   Refer to 节 8.4 for what to do with unused pins.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1] [2] [3]

		MIN	MAX	UNIT
V_{DD}	Supply voltage	-0.5	6	V
V_{SEL} or V_{EN}	Logic control input pin voltage (SEL)	-0.5	6	V
I_{SEL} or I_{EN}	Logic control input pin current (SEL)	-30	30	mA
V_S or V_D	Source or drain voltage (Sx, D)	-0.5	V_{DD}+0.5	V
I_S or $I_{D\,(CONT)}$	Source or drain continuous current (Sx, D)	-50	50	mA
I_K	Diode clamp current[4]	-30	30	mA
T_{stg}	Storage temperature	-65	150	°C
T_J	Junction temperature		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.
(4) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	1.08		5.5	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (Sx, D)	0		V_{DD}	V
V_{SEL}	Logic control input pin voltage (SEL)	0		5.5	V
T_A	Ambient temperature	-40		125	°C
t_r, t_f	Logic input pin rise and fall time			70	ns/V

6.4 Thermal Information

		TMUX1248	UNIT
	THERMAL METRIC[1]	**DCK (SC70)**	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	243.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	180.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	106.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	89.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	106.0	°C/W

6.4 Thermal Information (continued)

THERMAL METRIC[1]		TMUX1248	UNIT
		DCK (SC70)	
		6 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics (V_{DD} = 5 V ±10 %), GND = 0 V unless otherwise specified.

at T_A = 25°C, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to V_{DD} I_{SD} = 10 mA	25°C		3		Ω
			− 40°C to +85°C			5	Ω
			− 40°C to +125°C			6	Ω
$\triangle R_{ON}$	On-resistance matching between channels	V_S = 0 V to V_{DD} I_{SD} = 10 mA	25°C		0.15		Ω
			− 40°C to +85°C			1	Ω
			− 40°C to +125°C			1	Ω
R_{ON} FLAT	On-resistance flatness	V_S = 0 V to V_{DD} I_{SD} = 10 mA	25°C		1.5		Ω
			− 40°C to +85°C			2	Ω
			− 40°C to +125°C			3	Ω
$I_{S(OFF)}$	Source off leakage current[1]	V_{DD} = 5 V Switch Off V_D = 4.5 V / 1.5 V V_S = 1.5 V / 4.5 V	25°C		±75		nA
			− 40°C to +85°C	− 150		150	nA
			− 40°C to +125°C	− 175		175	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 5 V Switch On V_D = V_S = 4.5 V / 1 V	25°C		±200		nA
			− 40°C to +85°C	− 500		500	nA
			− 40°C to +125°C	− 750		750	nA
LOGIC INPUTS							
V_{IH}	Input logic high		-40°C to 125°C	1.42		5.5	V
V_{IL}	Input logic low		-40°C to 125°C	0		0.87	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		− 40°C to +125°C			±0.05	µA
C_{IN}	Digital input capacitance		25°C		1		pF
C_{IN}	Digital input capacitance		− 40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Digital Inputs = 0 V or 5.5 V	25°C		0.007		µA
			− 40°C to +125°C			1.5	µA

6.5 Electrical Characteristics (V_{DD} = 5 V ±10 %), GND = 0 V unless otherwise specified. (continued)

at T_A = 25°C, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Switching time between channels	V_S = 3 V R_L = 200 Ω, C_L = 15 pF	25°C		12		ns
			– 40°C to +85°C			18	ns
			– 40°C to +125°C			19	ns
t_{OPEN} (BBM)	Break before make time	V_S = 3 V R_L = 200 Ω, C_L = 15 pF	25°C		8		ns
			– 40°C to +85°C	1			ns
			– 40°C to +125°C	1			ns
Q_C	Charge Injection	V_S = V_{DD} /2 R_S = 0 Ω, C_L = 1 nF	25°C		– 10		pC
O_{ISO}	Off Isolation	R_L = 50 Ω, C_L = 5 pF f = 1 MHz	25°C		– 65		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz	25°C		– 45		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF f = 1 MHz	25°C		– 65		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz	25°C		– 45		dB
BW	Bandwidth	R_L = 50 Ω, C_L = 5 pF	25°C		250		MHz
C_{SOFF}	Source off capacitance	f = 1 MHz	25°C		7		pF
C_{SON} C_{DON}	On capacitance	f = 1 MHz	25°C		23		pF

(1)   When V_S is 4.5 V, V_D is 1.5 V or when V_S is 1.5 V, V_D is 4.5 V.

Product Folder Links: *TMUX1248*

6.6 Electrical Characteristics (V_{DD} = 3.3 V ±10 %), GND = 0 V unless otherwise specified.

at T_A = 25°C, V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to V_{DD} I_{SD} = 10 mA	25°C		4.5		Ω
			− 40°C to +85°C			12.5	Ω
			− 40°C to +125°C			13	Ω
$\triangle R_{ON}$	On-resistance matching between channels	V_S = 0 V to V_{DD} I_{SD} = 10 mA	25°C		0.15		Ω
			− 40°C to +85°C			1	Ω
			− 40°C to +125°C			1	Ω
R_{ON} FLAT	On-resistance flatness	V_S = 0 V to V_{DD} I_{SD} = 10 mA	25°C		3.5		Ω
			− 40°C to +85°C		4		Ω
			− 40°C to +125°C		5		Ω
$I_{S(OFF)}$	Source off leakage current[1]	V_{DD} = 3.3 V Switch Off V_D = 3 V / 1 V V_S = 1 V / 3 V	25°C		±75		nA
			− 40°C to +85°C	− 150		150	nA
			− 40°C to +125°C	− 175		175	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 3.3 V Switch On V_D = V_S = 3 V / 1 V	25°C		±200		nA
			− 40°C to +85°C	− 500		500	nA
			− 40°C to +125°C	− 750		750	nA
LOGIC INPUTS							
V_{IH}	Input logic high		-40°C to 125°C	1.3		5.5	V
V_{IL}	Input logic low		-40°C to 125°C	0		0.8	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		μA
I_{IH} I_{IL}	Input leakage current		− 40°C to +125°C			±0.05	μA
C_{IN}	Logic input capacitance		25°C		1		pF
C_{IN}	Logic input capacitance		− 40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Digital Inputs = 0 V or 5.5 V	25°C		0.004		μA
			− 40°C to +125°C			0.8	μA

Product Folder Links: *TMUX1248*

6.6 Electrical Characteristics (V_{DD} = 3.3 V ±10 %), GND = 0 V unless otherwise specified. (continued)

at T_A = 25°C, V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Switching time between channels	V_S = 2 V R_L = 200 Ω, C_L = 15 pF	25°C		14		ns
			– 40°C to +85°C			20	ns
			– 40°C to +125°C			22	ns
t_{OPEN} (BBM)	Break before make time	V_S = 2 V R_L = 200 Ω, C_L = 15 pF	25°C		8		ns
			– 40°C to +85°C	1			ns
			– 40°C to +125°C	1			ns
Q_C	Charge Injection	V_S = V_{DD}/2 R_S = 0 Ω, C_L = 1 nF	25°C		– 6		pC
O_{ISO}	Off Isolation	R_L = 50 Ω, C_L = 5 pF f = 1 MHz	25°C		– 65		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz	25°C		– 45		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF f = 1 MHz	25°C		– 65		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz	25°C		– 45		dB
BW	Bandwidth	R_L = 50 Ω, C_L = 5 pF	25°C		250		MHz
C_{SOFF}	Source off capacitance	f = 1 MHz	25°C		7		pF
C_{SON} C_{DON}	On capacitance	f = 1 MHz	25°C		23		pF

(1)   When V_S is 3 V, V_D is 1 V or when V_S is 1 V, V_D is 3 V.

6.7 Electrical Characteristics (V_{DD} = 1.8 V ±10 %), GND = 0 V unless otherwise specified.

at T_A = 25°C, V_{DD} = 1.8 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to V_{DD} I_{SD} = 10 mA	25°C		40		Ω
			−40°C to +85°C			80	Ω
			−40°C to +125°C			80	Ω
△R_{ON}	On-resistance matching between channels	V_S = 0 V to V_{DD} I_{SD} = 10 mA	25°C		0.4		Ω
			−40°C to +85°C			1.5	Ω
			−40°C to +125°C			1.5	Ω
R_{ON} FLAT	On-resistance flatness	V_S = 0 V to V_{DD} I_{SD} = 10 mA	25°C		35		Ω
$I_{S(OFF)}$	Source off leakage current[1]	V_{DD} = 1.98 V Switch Off V_D = 1.8 V / 1 V V_S = 1 V / 1.8 V	25°C		±75		nA
			−40°C to +85°C	−150		150	nA
			−40°C to +125°C	−175		175	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 1.98 V Switch On V_D = V_S = 1.62 V / 1 V	25°C		±200		nA
			−40°C to +85°C	−500		500	nA
			−40°C to +125°C	−750		750	nA
DIGITAL INPUTS							
V_{IH}	Input logic high		−40°C to +125°C	1.07		5.5	V
V_{IL}	Input logic low		−40°C to +125°C	0		0.68	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		−40°C to +125°C			±0.05	µA
C_{IN}	Logic input capacitance		25°C		1		pF
C_{IN}	Logic input capacitance		−40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic Inputs = 0 V or 5.5 V	25°C		0.002		µA
			−40°C to +125°C			0.52	µA

Product Folder Links: *TMUX1248*

6.7 Electrical Characteristics (V_{DD} = 1.8 V ±10 %), GND = 0 V unless otherwise specified. (continued)

at T_A = 25°C, V_{DD} = 1.8 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Switching time between channels	V_S = 1 V R_L = 200 Ω, C_L = 15 pF	25°C		24		ns
			– 40°C to +85°C			44	ns
			– 40°C to +125°C			45	ns
t_{OPEN} (BBM)	Break before make time	V_S = 1 V R_L = 200 Ω, C_L = 15 pF	25°C		16		ns
			– 40°C to +85°C	1			ns
			– 40°C to +125°C	1			ns
Q_C	Charge Injection	V_S = V_{DD}/2 R_S = 0 Ω, C_L = 1 nF	25°C		– 3		pC
O_{ISO}	Off Isolation	R_L = 50 Ω, C_L = 5 pF f = 1 MHz	25°C		– 65		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz	25°C		– 45		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF f = 1 MHz	25°C		– 65		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz	25°C		– 45		dB
BW	Bandwidth	R_L = 50 Ω, C_L = 5 pF	25°C		250		MHz
C_{SOFF}	Source off capacitance	f = 1 MHz	25°C		7		pF
C_{SON} C_{DON}	On capacitance	f = 1 MHz	25°C		23		pF

(1) When V_S is 1.8 V, V_D is 1 V or when V_S is 1 V, V_D is 1.8 V.

Product Folder Links: *TMUX1248*

6.8 Electrical Characteristics (V_{DD} = 1.2 V ±10 %), GND = 0 V unless otherwise specified.

at T_A = 25°C, V_{DD} = 1.2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to V_{DD} I_{DS} = 10 mA	25°C		70		Ω
			−40°C to +85°C			105	Ω
			−40°C to +125°C			105	Ω
$\triangle R_{ON}$	On-resistance matching between channels	V_S = 0 V to V_{DD} I_{DS} = 10 mA	25°C		0.4		Ω
			−40°C to +85°C			1.5	Ω
			−40°C to +125°C			1.5	Ω
R_{ON} FLAT	On-resistance flatness	V_S = 0 V to V_{DD} I_{DS} = 10 mA	25°C		65		Ω
$I_{S(OFF)}$	Source off leakage current[1]	V_{DD} = 1.32 V Switch Off V_D = 1.2 V / 1 V V_S = 1 V / 1.2 V	25°C		±75		nA
			−40°C to +85°C	−150		150	nA
			−40°C to +125°C	−175		175	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 1.32 V Switch On V_D = V_S = 1 V / 0.8 V	25°C		±200		nA
			−40°C to +85°C	−500		500	nA
			−40°C to +125°C	−750		750	nA
DIGITAL INPUTS							
V_{IH}	Input logic high		−40°C to +125°C	0.96			V
V_{IL}	Input logic low		−40°C to +125°C			0.36	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		−40°C to +125°C			±0.10	µA
C_{IN}	Digital input capacitance		25°C		1		pF
C_{IN}	Digital input capacitance		−40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Digital Inputs = 0 V or 5.5 V	25°C		0.0015		µA
			−40°C to +125°C			0.45	µA

Product Folder Links: *TMUX1248*

6.8 Electrical Characteristics (V_{DD} = 1.2 V ±10 %), GND = 0 V unless otherwise specified. (continued)

at T_A = 25°C, V_{DD} = 1.2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Switching time between channels	V_{IN} = V_{DD} V_S = 1 V R_L = 200 Ω, C_L = 15 pF	25°C		40		ns
			– 40°C to +85°C			175	ns
			– 40°C to +125°C			175	ns
t_{OPEN} (BBM)	Break before make time	V_S = 1 V R_L = 200 Ω, C_L = 15 pF	25°C		27		ns
			– 40°C to +85°C	1			ns
			– 40°C to +125°C	1			ns
Q_C	Charge Injection	V_S = (V_{DD} + V_{SS})/2 R_S = 0 Ω, C_L = 1 nF	25°C		±5		pC
O_{ISO}	Off Isolation	R_L = 50 Ω, C_L = 5 pF f = 1 MHz	25°C		– 64		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz	25°C		– 44		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF f = 1 MHz	25°C		– 64		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz	25°C		– 44		dB
BW	Bandwidth	R_L = 50 Ω, C_L = 5 pF	25°C		250		MHz
C_{SOFF}	Source off capacitance	f = 1 MHz	25°C		7		pF
C_{SON} C_{DON}	On capacitance	f = 1 MHz	25°C		23		pF

(1)   When V_S is 1 V, V_D is 1.2 V or when V_S is 1.2 V, V_D is 1 V.

Product Folder Links: TMUX1248

6.9 Typical Characteristics

At T_A = 25°C, V_{DD} = 5 V (unless otherwise noted).

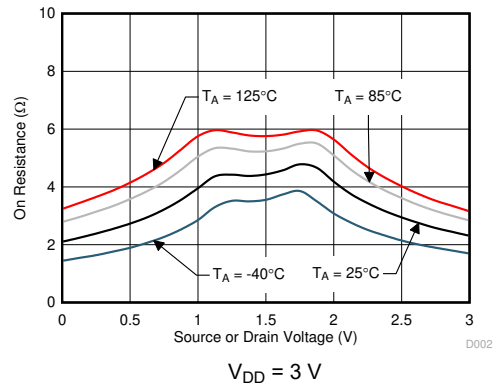T_A = 25°C
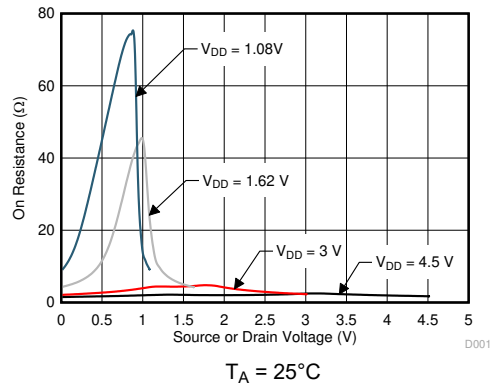
图 6-1. On-Resistance vs Source or Drain Voltage

V_{DD} = 3 V

图 6-2. On-Resistance vs Source or Drain Voltage

T_A = 25°C
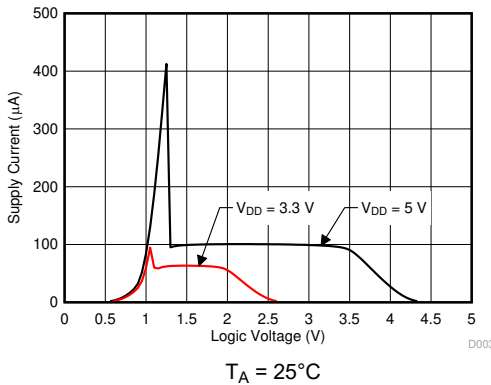
图 6-3. Supply Current vs Logic Voltage

T_A = 25°C
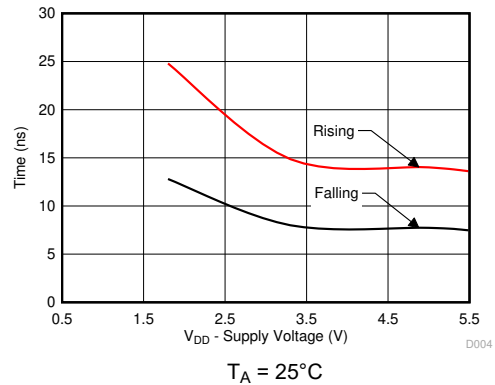
图 6-4. $T_{transition}$ vs Supply Voltage

T_A = 25°C
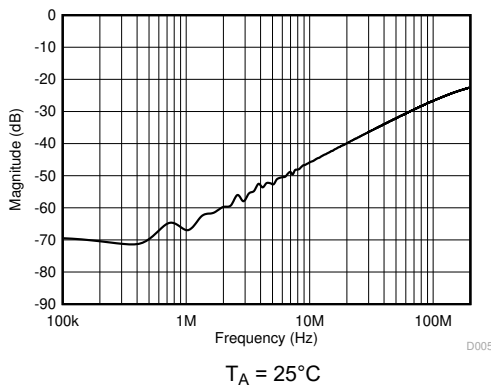
图 6-5. Crosstalk and Off-Isolation vs Frequency

T_A = 25°C

图 6-6. Frequency Response

Product Folder Links: *TMUX1248*
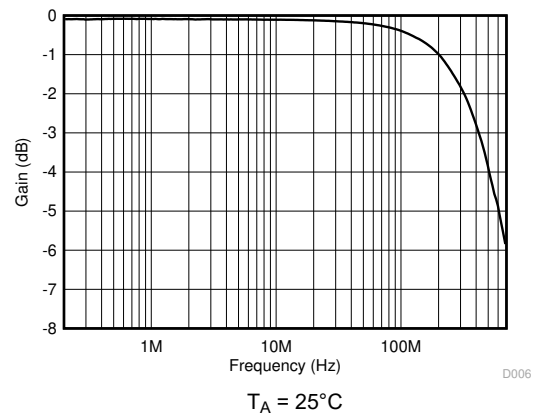
7 Parameter Measurement Information

7.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown in 图 7-1. Voltage (V) and current (I_{SD}) are measured using this setup, and R_{ON} is computed with $R_{ON} = V / I_{SD}$:
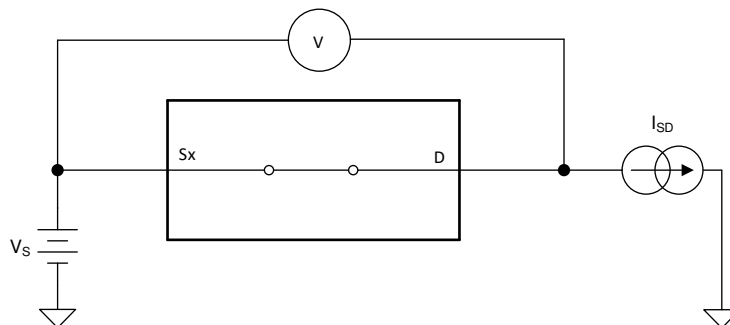

图 7-1. On-Resistance Measurement Setup

7.2 Off-Leakage Current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

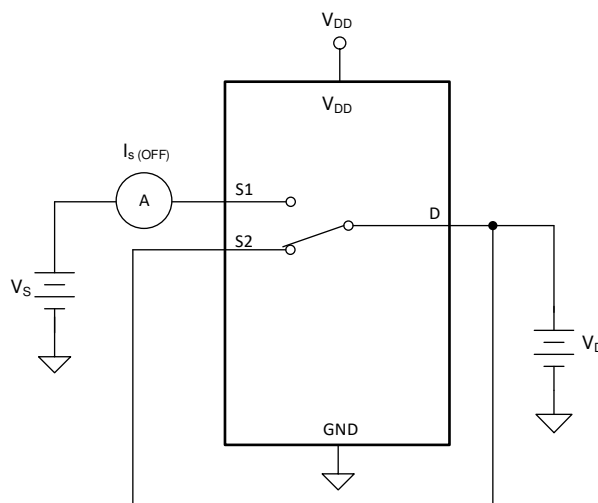The setup used to measure off-leakage current is shown in 图 7-2.

图 7-2. Off-Leakage Measurement Setup

Product Folder Links: *TMUX1248*

7.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. 图 7-3 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.
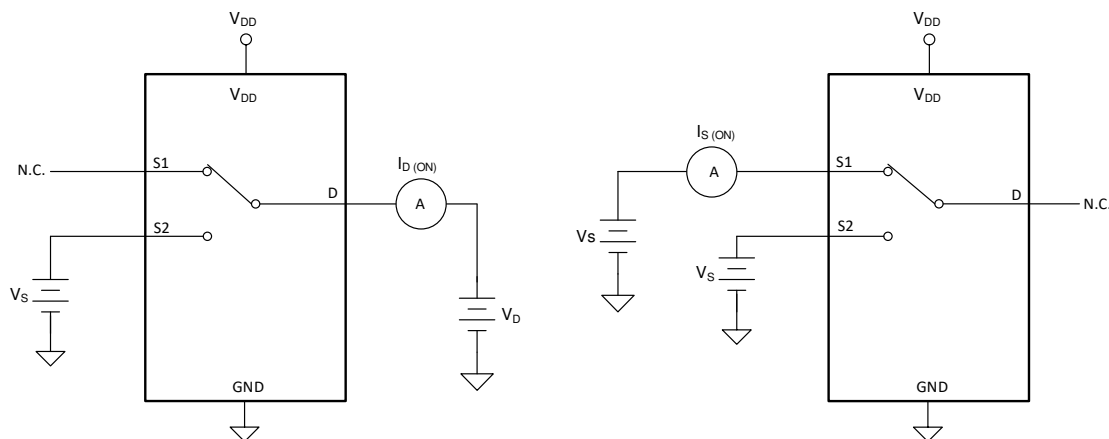

图 7-3. On-Leakage Measurement Setup

7.4 Transition Time

Transition time is defined as the time taken by the output of the device to rise or fall 10% after the logic control signal has risen or fallen past the logic threshold. The 10% transition measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. 图 7-4 shows the setup used to measure transition time, denoted by the symbol $t_{TRANSITION}$.

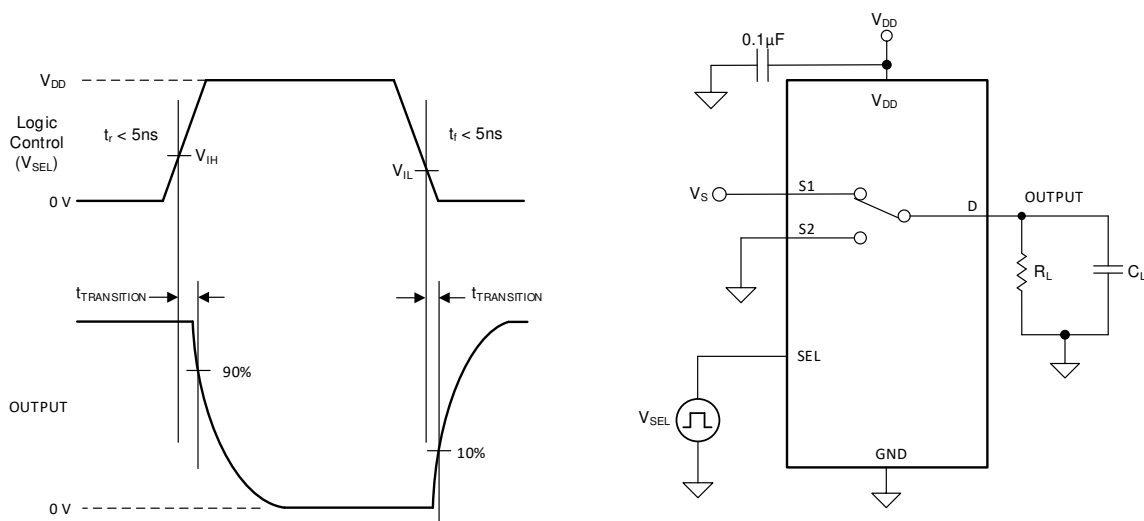图 7-4. Transition-Time Measurement Setup

Product Folder Links: *TMUX1248*

7.5 Break-Before-Make

Break-before-make delay is a safety feature that prevents two inputs from connecting when the device is switching. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. 图 7-5 shows the setup used to measure break-before-make delay, denoted by the symbol $t_{OPEN(BBM)}$.
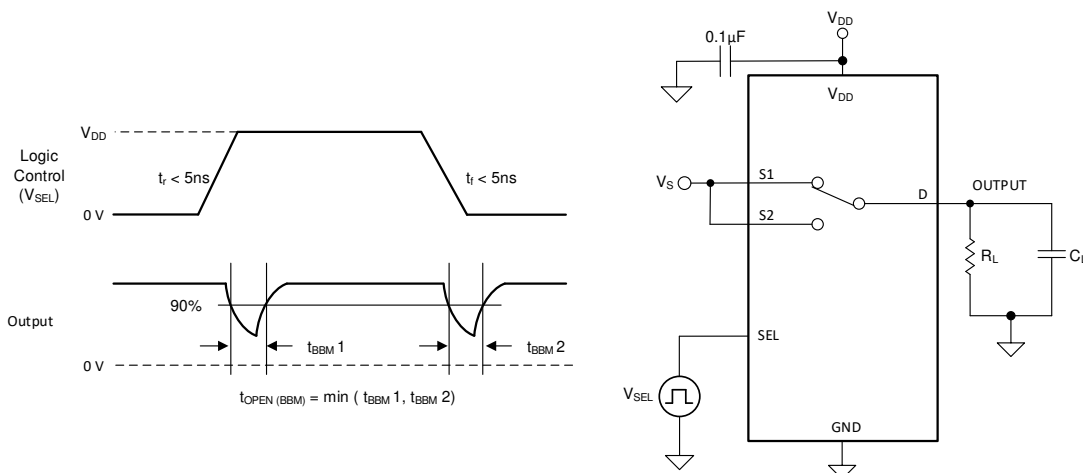

图 7-5. **Break-Before-Make Delay Measurement Setup**

7.6 Charge Injection

The TMUX1248 has a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_C. 图 7-6 shows the setup used to measure charge injection from Drain (D) to Source (Sx).
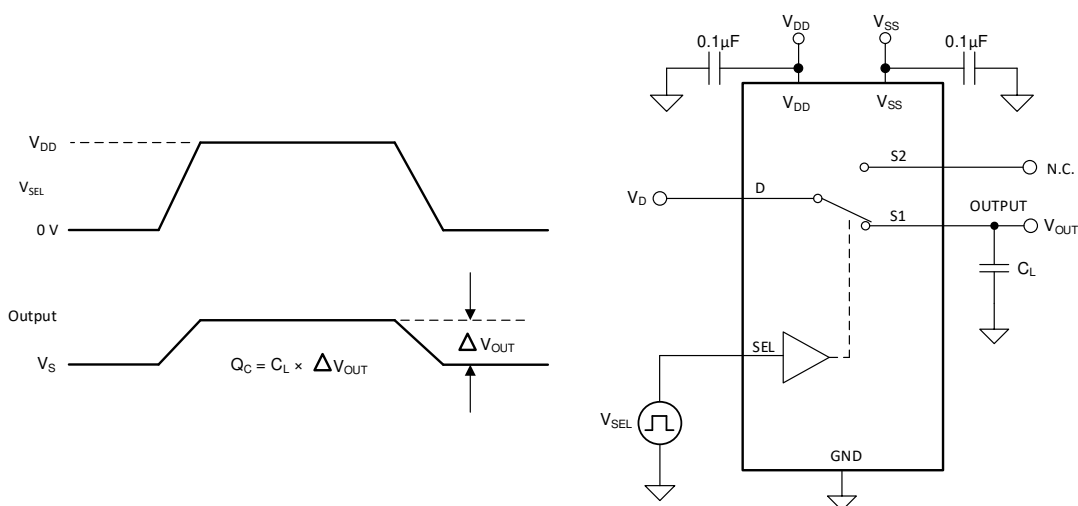

图 7-6. **Charge-Injection Measurement Setup**

Product Folder Links: *TMUX1248*

7.7 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (D) of the device when a signal is applied to the source pin (Sx) of an off-channel. 图 7-7 shows the setup used to measure, and the equation used to calculate off isolation.

图 7-7. Off Isolation Measurement Setup

$$\text{Off Isolation} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right)$$

(1)

7.8 Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (D) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. 图 7-8 shows the setup used to measure, and the equation used to calculate crosstalk.
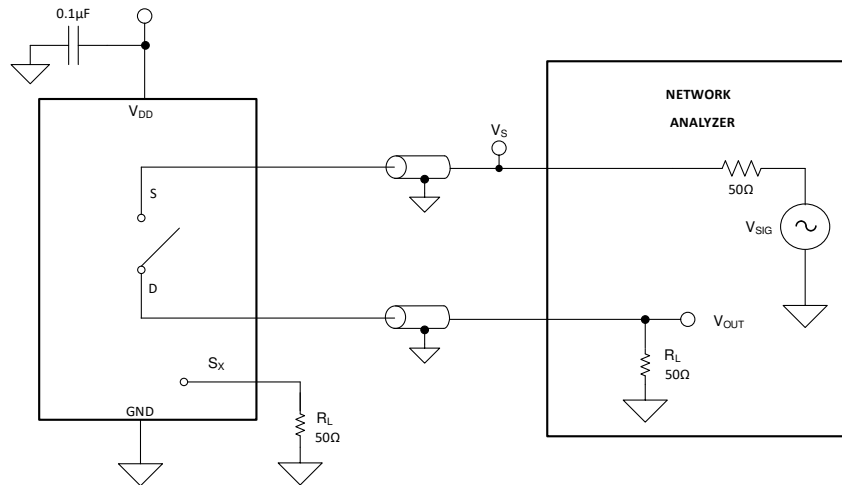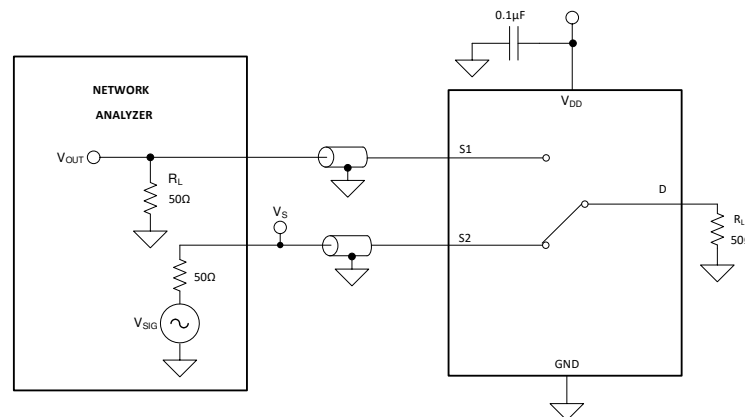

图 7-8. Crosstalk Measurement Setup

$$\text{Channel-to-Channel Crosstalk} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right)$$

(2)

7.9 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D) of the device. 图 7-9 shows the setup used to measure bandwidth.
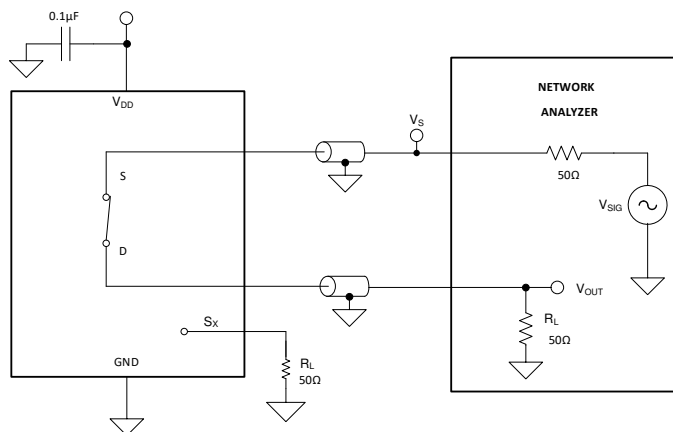
图 **7-9. Bandwidth Measurement Setup**

8 Detailed Description

8.1 Overview

The TMUX1248 is a 2:1 (SPDT), 1-channel switch where the input is controlled with a single select (SEL) control pin.

8.2 Functional Block Diagram
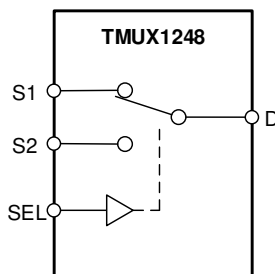
图 **8-1. TMUX1248 Functional Block Diagram**

8.3 Feature Description

8.3.1 Bidirectional Operation

The TMUX1248 conducts equally well from source (Sx) to drain (D) or from drain (D) to source (Sx). The device has very similar characteristics in both directions and supports both analog and digital signals.

8.3.2 Rail to Rail Operation

The valid signal path input/output voltage for TMUX1248 ranges from GND to V_{DD}.

Product Folder Links: *TMUX1248*

8.3.3 1.8 V Logic Compatible Inputs

The TMUX1248 has 1.8 V logic compatible control for the logic control input (SEL). The logic input threshold scales with supply but still provides 1.8 V logic control when operating at 5.5 V supply voltage. 1.8 V logic level inputs allow the TMUX1248 to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. For more information on 1.8 V logic implementations refer to *Simplifying Design with 1.8 V logic Muxes and Switches*.

8.3.4 Fail-Safe Logic

The TMUX1248 supports Fail-Safe Logic on the control input pin (SEL) allowing for operation up to 5.5 V, regardless of the state of the supply pin. This feature allows voltages on the control pin to be applied before the supply pin, or allows higher voltages on the SEL pin up to 5.5 V, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pin. For example, the Fail-Safe Logic feature allows the select pin of the TMUX1248 to be ramped to 5.5 V while V_{DD} = 0 V. Additionally, the feature enables operation of the TMUX1248 with V_{DD} = 1.2 V while allowing the select pin to interface with a logic level of another device up to 5.5 V.

8.4 Device Functional Modes

The select (SEL) pin of the TMUX1248 controls which switch is connected to the drain of the device. When a given input is not selected, that source pin is in high impedance mode (HI-Z). The control pins can be as high as 5.5 V.

The TMUX1248 can be operated without any external components except for the supply decoupling capacitors. Unused logic control pins should be tied to GND or V_{DD} in order to ensure the device does not consume additional current as highlighted in *Implications of Slow or Floating CMOS Inputs*. Unused signal path inputs (Sx or D) should be connected to GND.

8.5 Truth Tables

表 8-1. TMUX1248 Truth Table

CONTROL LOGIC (SEL)	Selected Source (Sx) Connected To Drain (D) Pin
0	S1
1	S2

Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TMUX12xx family offers good system performance across a wide operating supply (1.08 V to 5.5 V). These devices include 1.8 V logic compatible control input pins that enable operation in systems with 1.8 V I/O rails. Additionally, the control input pin supports Fail-Safe Logic which allows for operation up to 5.5 V, regardless of the state of the supply pin. This protection stops the logic pins from back-powering the supply rail. These features of the TMUX12xx, a family of general purpose multiplexers and switches, reduce system complexity, board size, and overall system cost.

9.2 Typical Application

9.2.1 Switchable Operational Amplifier Gain Setting

Another example application of the TMUX1248 is to change an Op Amp from unity gain setting to an inverting amplifier configuration. Utilizing a switch allows a system to have a configurable gain and allows the same architecture to be utilized across the board for various inputs to the system. 图 9-1 shows the TMUX1248 configured for gain setting application.
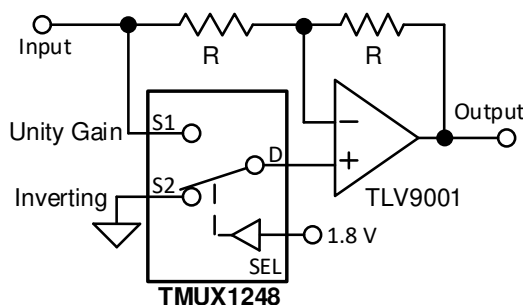
图 **9-1. Switchable Op Amp Gain Setting**

9.2.1.1 Design Requirements

This design example uses the parameters listed in 表 9-1.

表 **9-1. Design Parameters**

PARAMETERS	VALUES
Input Signal	0 V to 2.75 V
Mux Supply (V_{DD})	2.75 V
Op Amp Supply (V_+/ V_-)	±2.75 V
Mux I/O signal range	0 V to V_{DD} (Rail to Rail)
Control logic thresholds	1.8 V compatible (up to 5.5 V)

Product Folder Links: *TMUX1248*

9.2.1.2 Detailed Design Procedure

The application shown in 图 9-1 demonstrates how to use a single control input and toggle between gain settings of -1 and +1. If switching between inverting and unity gain is not required, the TMUX1248 can be utilized in the feedback path to select different feedback resistors and provide scalable gain settings for configurable signal conditioning.

The TMUX1248 can be operated without any external components except for the supply decoupling capacitors. The select pin is recommended to have a pull-down or pull-up resistor to ensure the input is in a known state if the control signal becomes disconnected. All inputs to the switch must fall within the recommend operating conditions of the TMUX1248 including signal range and continuous current. For this design with a supply of 2.75 V the signal range can be 0 V to 2.75 V and the max continuous current can be 50 mA.
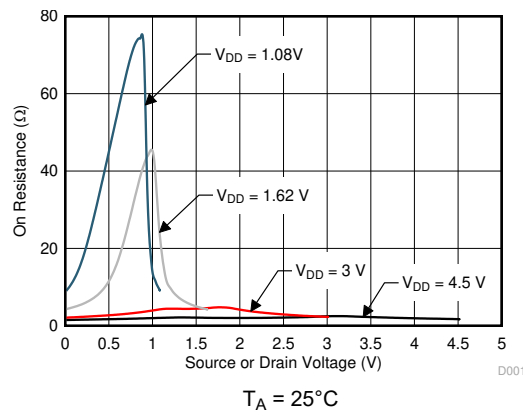
9.2.1.3 Application Curve

图 9-2. On-Resistance vs Source or Drain Voltage

9 Power Supply Recommendations

The TMUX1248 operates across a wide supply range of 1.08 V to 5.5 V. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the V_{DD} supply to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 μF to 10 μF from V_{DD} to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

Product Folder Links: *TMUX1248*

10 Layout

10.1 Layout Guidelines

10.1.1 Layout Information

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection primarily occurs because the width of the trace changes. At the apex of the turn, the trace width increases to 1.414 times its width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self‑inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. 图 10-1 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.
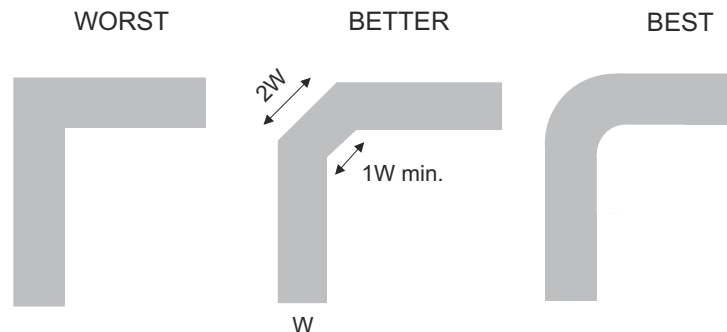
图 **10-1. Trace Example**

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

图 10-2 illustrates an example of a PCB layout with the TMUX1248. Some key considerations are:

- Decouple the V_{DD} pin with a 0.1-µF capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{DD} supply.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.
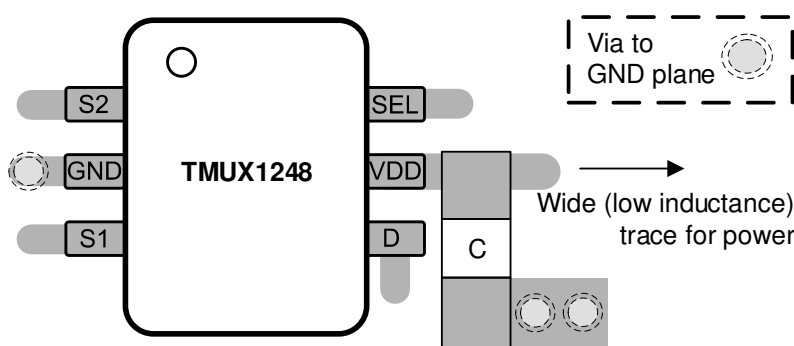
10.2 Layout Example

图 **10-2. TMUX1248 Layout Example**

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Improve Stability Issues with Low CON Multiplexers* application brief
- Texas Instruments, *Simplifying Design with 1.8 V logic Muxes and Switches* application brief
- Texas Instruments, *Eliminate Power Sequencing with Powered-off Protection Signal Switches* application brief
- Texas Instruments, *System-Level Protection for High-Voltage Analog Multiplexers* application reports

11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者"按原样"提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.4 Trademarks

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 术语表

TI 术语表   本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要声明和免责声明

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMUX1248DCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	SN	Level-1-260C-UNLIM	-40 to 125	248	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
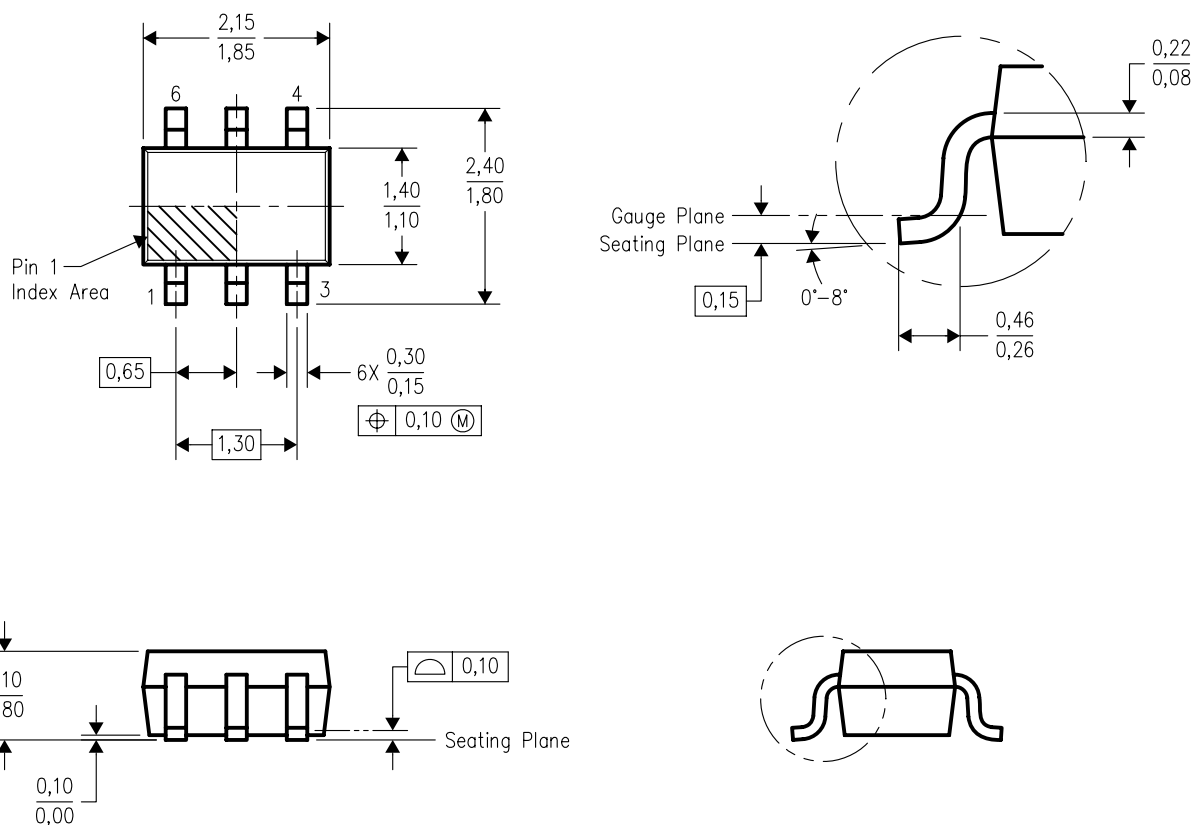
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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DCK (R−PDSO−G6) PLASTIC SMALL−OUTLINE PACKAGE

2,15
1,85

6   4

2,40
1,80

1,40
1,10

Pin 1
Index Area

1   3

0,65

6X 0,30
0,15

1,30

⊕ 0,10 Ⓜ

0,22
0,08

Gauge Plane
Seating Plane

0,15   0°−8°

0,46
0,26

1,10
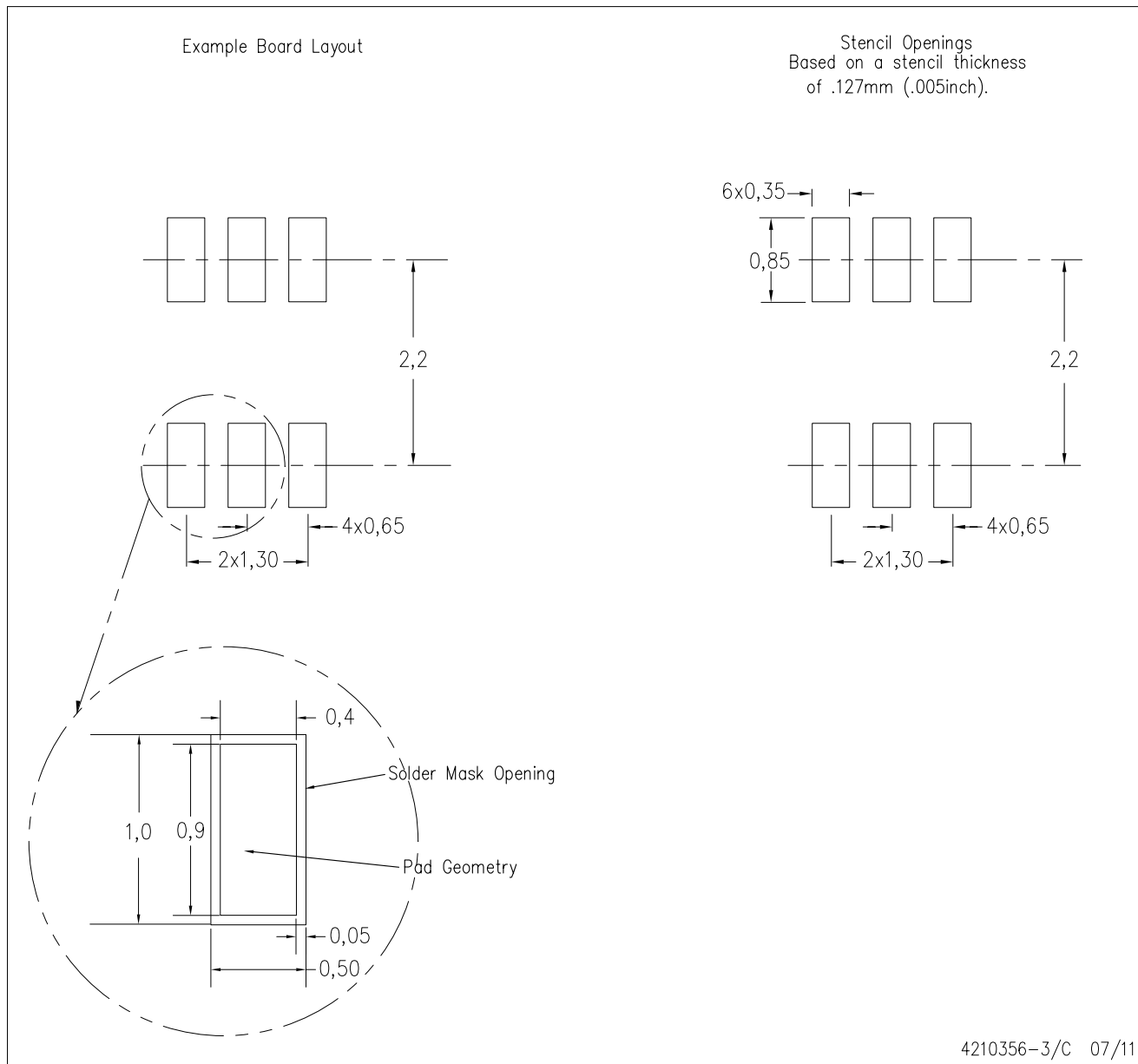0,80

0,10

Seating Plane

0,10
0,00

0,10

4093553−4/G 01/2007

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO−203 variation AB.

DCK (R−PDSO−G6)   PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

6x0,35

0,85

2,2

2,2

4x0,65

4x0,65

2x1,30

2x1,30

0,4

Solder Mask Opening

1,0   0,9

Pad Geometry

0,05

0,50

4210356−3/C 07/11

NOTES: A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.
          C.   Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
          D.   Publication IPC−7351 is recommended for alternate designs.
          E.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
               contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric
               metal load solder paste. Refer to IPC−7525 for other stencil recommendations.

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