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5 通道节省空间静电放电 (ESD) 保护器件

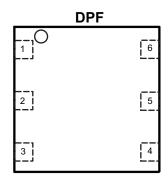
查询样品: TPD5E003

特性

- 为低压输入输出 (IO) 接口提供系统级的 ESD 保护
- IEC 61000-4-2 级别 4
 - ±15kV (接触放电)
 - ±15kV (空气间隙放电)
- 典型 IO 电容 7pF (V_{IO}=2.5V)
- 直流 (DC) 击穿电压 6V (最小值)
- 低泄漏电流 100nA (最大值)
- 低 ESD 钳位电压
- 工业温度范围: -40°C 至 125°C
- IEC 61000-4-5 (浪涌): 40W (8/20µs 脉冲)
- 小型、易于走线的 DPF 封装

应用范围

- SIM 卡
- 侧键
- 音频接口
- 存储卡



1 mm x 1 mm x 0.4mm (0.35-mm pitch)

说明

TPD5E003 是一款 5 通道 ESD 保护器件。 它提供 ±15KV IEC 接触和 ±15KV 空气间隙 ESD 保护。 它特有 5 个 完全一样的 ESD 钳位二极管,这些二极管可被用于 5 个单向(0V 至 5V)I/O 线路或 4 个双向(-5V 至 5V)I/O 线路。 较低的 IO 电容适合于广泛的应用。 典型应用领域包括音频线路(麦克风、耳机和免提电话),SD 接口和 袖珍键盘以及其他按钮。

订购信息

T _A	#	対装(1)(2)	可订购部件号	正面标记		
-40°C 至 125°C	C 至 125°C 5000 卷带		TPD5E003DPFR	9Q		

- (1) 封装图样、热数据和符号可从网站www.ti.com/packaging中获取。
- (2) 要获得最新的封装和订购信息,请见本文档末尾的封装选项附录,或者浏览 TI 网站www.ti.com。



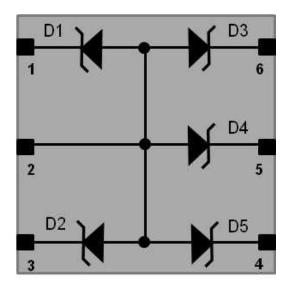
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.





These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

APPLICATION/FUNCTIONAL BLOCK DIAGRAM



PIN FUNCTIONS

PIN NAME	DPF	PIN TYPE	DESCRIPTION
I/O	1, 3, 4, 5, 6	I/O	ESD Protected channel
GND	2	GND	Ground

ABSOLUTE MAXIMUM RATINGS

	MIN	MAX	UNIT
IO voltage tolerance		5.5	V
Operating temperature range	-40	125	°C
Storage temperature	-55	150	°C
IEC 61000-4-2 contact ESD		±15	kV
IEC 61000-4-2 air-gap ESD		±15	kV
I _{PP} , peak pulse current (tp = 8/20μs)		3	Α
P _{PP} , peak pulse power (tp = 8/20µs)		40	W

ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V _{RWM}	Reverse stand-off voltage	Ι _Ι = 0.1 μΑ			5.0	V
I _{LEAK}	Leakage Current	Pin 1, 3, 4, 5, or 6 = 5V, Pin 2 = 0V		10	100	nA
\((C _{0},,)	Claren veltana with ECD strile	I _{PP} = 6A, TLP, Dx pin to GND, T _A = 25 °C		13	15.6	V
VClamp		I_{PP} = 10 A, TLP, Dx pin to GND, T_A = 25 °C		16.3	19.5	V
_	Danasia maiata	I_{TLP} = 6A to 10 A, Dx pin to GND, T_A = 25 °C		0.8	1	Ω
R _{DYN}	Dynamic resistance	I_{TLP} = 6A to 10 A, GND to Dx pin, T_A = 25 °C		0.3	0.4	Ω
_	IO conscitores	V _{IO} = 2.5V, 1 MHz, T _A = 25 °C	5.6	7	8.4	pF
C _{IO}	IO capacitance	V _{IO} = 0V, 1 MHz, T _A = 25 °C	8	10	12	рF
V_{BR}	Break-down voltage	I _{IO} = 1 mA	6.0	7	8.5	V



APPLICATION INFORMATION

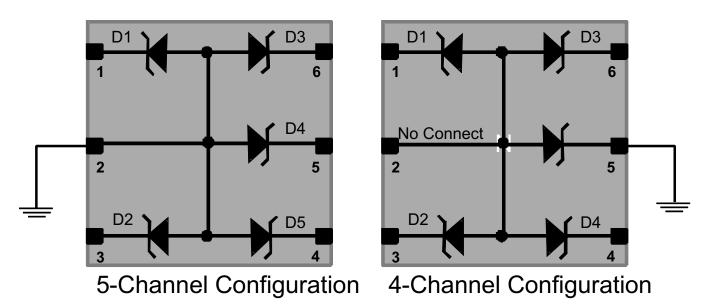


Figure 1. Application Diagram

The TPD5E003 offers 5 identical unidirectional ESD protection channels. To use all 5 channels, the recommended configuration is shown in Figure 1. The TPD5E003 can also be used as 4 identical bidirectional ESD protection channels. To do so, pin 5 would be connected to ground, with pin 1, 3, 4, and 6 connected to the I/O to be protected. In the bidirectional configuration, IO capacitance is reduced by half and the breakdown voltage is doubled.



TYPICAL CHARACTERISTICS

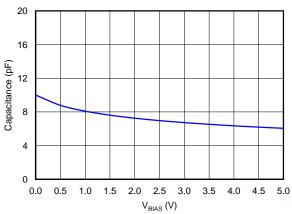


Figure 2. Capacitance vs DC Bias Voltage

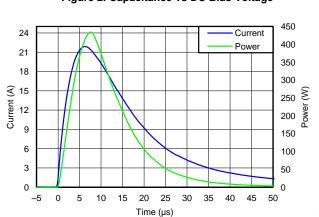


Figure 4. Surge Plot (tp = $8/20\mu$ s), Pin GND to Dx

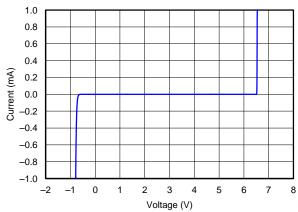


Figure 6. DC SWEEP V-I Curve

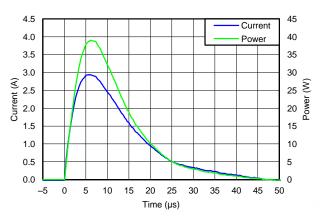


Figure 3. Surge Plot (tp = $8/20\mu s$), Pin Dx to GND

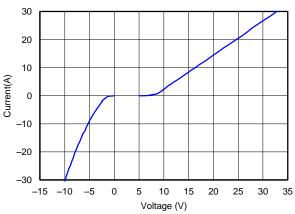


Figure 5. 30 Amps TLP Plot

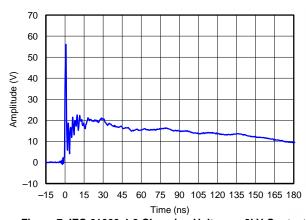


Figure 7. IEC 61000-4-2 Clamping Voltage, +8kV Contact



TYPICAL CHARACTERISTICS (continued)

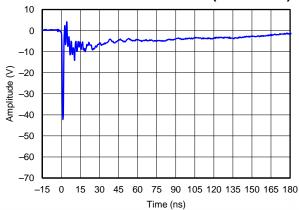


Figure 8. IEC 61000-4-2 Clamping Voltage, -8kV Contact

ZHCSAP3A - DECEMBER 2012-REVISED JANUARY 2013



REVISION HISTORY

Cł	nanges from Original (December 2012) to Revision A	Page
•	Added IO voltage tolerance to the ABSOLUTE MAXIMUM RATINGS table.	2
•	Added MAX values to parameters in the ELECTRICAL CHARACTERISTICS table.	2



PACKAGE OPTION ADDENDUM

10-Dec-2020

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead finish/ Ball material	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
TPD5E003DPFR	ACTIVE	X2SON	DPF	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	9Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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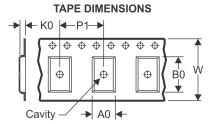
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PACKAGE MATERIALS INFORMATION

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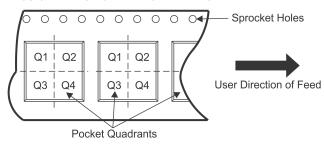
TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD5E003DPFR	X2SON	DPF	6	5000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2

PACKAGE MATERIALS INFORMATION

www.ti.com 24-Jul-2020

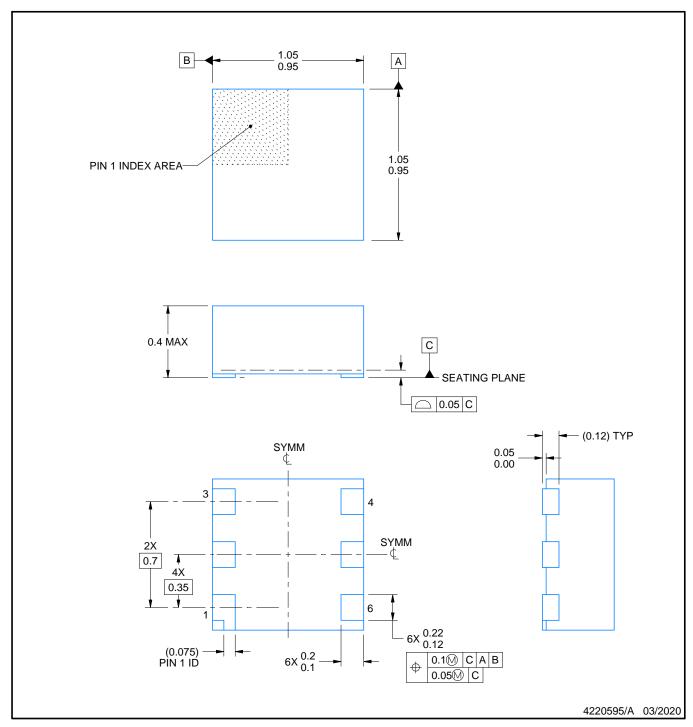


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)	
TPD5E003DPFR	X2SON	DPF	6	5000	184.0	184.0	19.0	



PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

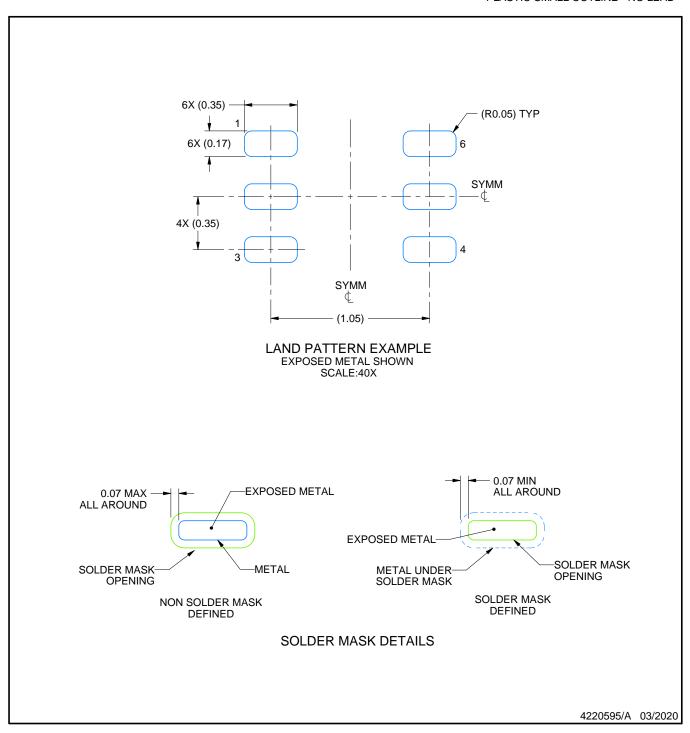
- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. Reference JEDEC registration MO-287, variation X2AAF.



PLASTIC SMALL OUTLINE - NO LEAD

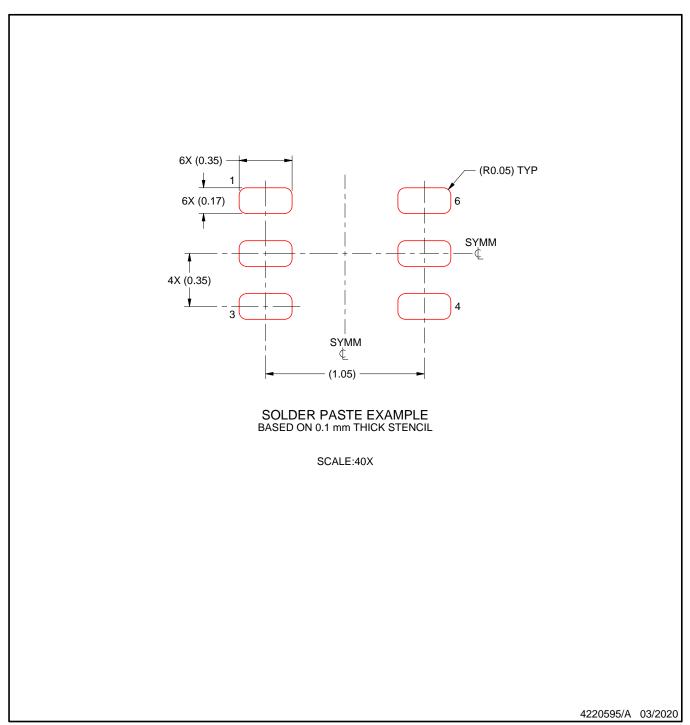


NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



PLASTIC SMALL OUTLINE - NO LEAD



4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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