TPS22965 5.7V，6A，16mΩ 导通电阻负载开关

1 特性

- 集成单通道负载开关
- 输入电压范围：0.8V 至 5.7V
- 超低导通电阻 (R_{ON})
  - $V_{输入}$ = 5V（$V_{偏置}$ = 5V）时，$R_{导通}$ = 16mΩ
  - $V_{输入}$ = 3.6V（$V_{偏置}$ = 5V）时，$R_{导通}$ = 16mΩ
  - $V_{输入}$ = 1.8V（$V_{偏置}$ = 5V）时，$R_{导通}$ = 16mΩ
- 6A 最大持续开关电流
- 低静态电流 (50μA)
- 低控制输入阀值支持使用 1.2V，1.8V，2.5V 和 3.3V 逻辑电路
- 可配置的上升时间
- 快速输出放电 (QOD)
- 带有散热垫的小外形尺寸无引线 (SON) 8 引脚封装
- 根据 JESD 22 测试得出的静电放电 (ESD) 性能
  - 2000V 人体模型 (HBM) 和 1000V 充电器件模型 (CDM)

2 应用范围

- Ultrabook™
- 笔记本电脑/上网本
- 平板电脑
- 消费类电子产品
- 机顶盒/家庭网关
- 电信系统
- 固态硬盘 (SSD)

3 说明

TPS22965 是一款单通道负载开关，可提供可配置的上升时间来尽量减小浪涌电流。 此器件包括一个 N 通道金属氧化物半导体场效应晶体管 (MOSFET)，可在 0.8V 至 5.7V 的输入电压范围内运行并可支持 6A 的最大持续电流。此开关由一个开/关输入 (ON) 控制，此输入能够直接连接低电压控制信号。 在 TPS22965 中，为了实现开关关闭时的快速输出放电，增加了一个 225Ω 的片上负载电阻器。

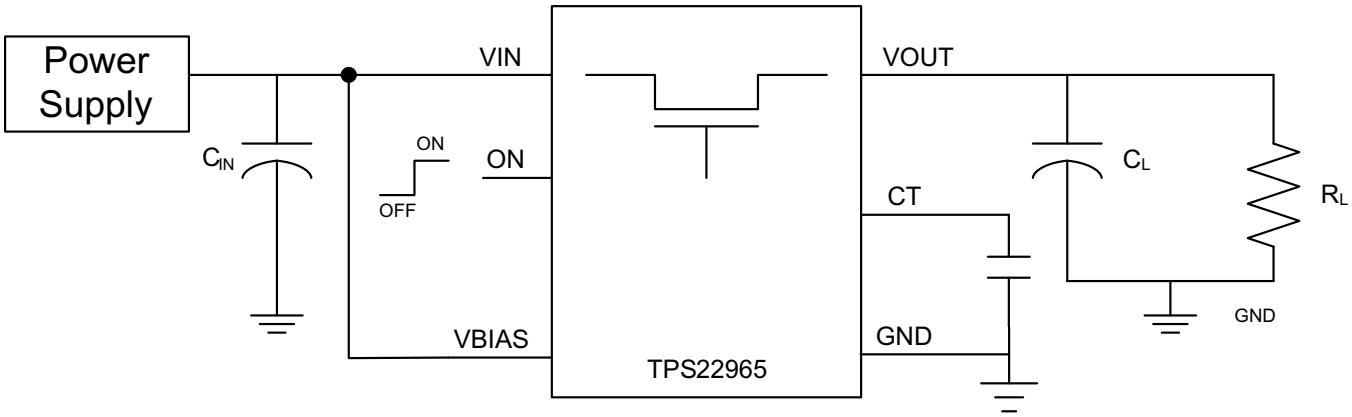
TPS22965 采用小型，节省空间的 2.00mm x 2.00mm 8 引脚 SON 封装 (DSG)，且带有集成散热焊盘，支持较高功耗。 器件在自然通风环境下的额定运行温度范围为 -40°C 至 85°C。

器件信息(1)

部件号	封装	封装尺寸（标称值）
TPS22965	DSG (8)	2.00mm x 2.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

4 简化电路原理图



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5 修订历史记录

Changes from Revision A (August 2013) to Revision B **Page**

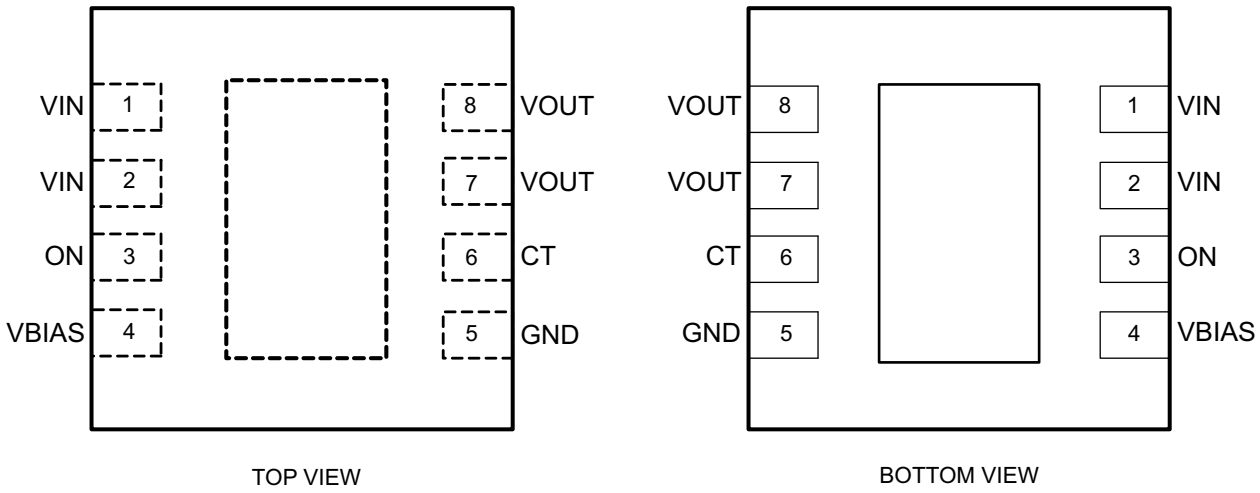
- 已更改 已将此数据表更改为新的模板布局。 ... 1
- 添加了器件信息表。 ... 1
- Added Handling Ratings table. ... 4
- Changed MAX value of "V_{IN}" from 5.5 V to 5.7 V. ... 4
- Changed MAX value of "V_{BIAS}" from 5.5 V to 5.7 V. ... 4
- Changed MAX value of "V_{ON}" from 5.5 V to 5.7 V. ... 4
- Added Thermal Information table. ... 4
- Added Detailed Description Section. ... 14
- Added Application and Implementation section. ... 16
- Added Power Supply Recommendations section. ... 19
- Added Layout section. ... 19

Changes from Original (August 2012) to Revision A **Page**

- Updated VON MAX value to fix typo that restricted operating range. Changed MAX value from "VIN" to "5.5" to align with rest of document. ... 4

6 Pin Configuration and Functions

DSG PACKAGE



Pin Functions

PIN		I/O	DESCRIPTION
NAME	DSG		
CT	6	O	Switch slew rate control. Can be left floating. See *Application Information* section for more information.
GND	5	–	Device ground.
ON	3	I	Active high switch control input. Do not leave floating.
Thermal Pad	–	–	Thermal pad (exposed center pad) to alleviate thermal stress. Tie to GND. See *Layout Example* section for layout guidelines.
VBIAS	4	I	Bias voltage. Power supply to the device. Recommended voltage range for this pin is 2.5V to 5.7V. See *Application and Implementation* section for more information.
VIN	1, 2	I	Switch input. Input bypass capacitor recommended for minimizing V_{IN} dip. Must be connected to Pin 1 and Pin 2. See *Application and Implementation* section for more information.
VOUT	7, 8	O	Switch output.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
V_{IN}	Input voltage range	–0.3	6	V
V_{OUT}	Output voltage range	–0.3	6	V
V_{BIAS}	Bias voltage range	–0.3	6	V
V_{ON}	Input voltage range	–0.3	6	V
I_{MAX}	Maximum continuous switch current		6	A
I_{PLS}	Maximum pulsed switch current, pulse <300 µs, 2% duty cycle		8	A
T_J	Maximum junction temperature		125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–2000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–1000	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{IN}	Input voltage range		0.8	V_{BIAS}	V
V_{BIAS}	Bias voltage range		2.5	5.7	V
V_{ON}	ON voltage range		0	5.7	V
V_{OUT}	Output voltage range			V_{IN}	V
V_{IH}	High-level input voltage, ON	V_{BIAS} = 2.5 V to 5.7 V	1.2	5.7	V
V_{IL}	Low-level input voltage, ON	V_{BIAS} = 2.5 V to 5.7 V	0	0.5	V
C_{IN}	Input capacitor		1(1)		µF
T_A	Operating free-air temperature range(2)		–40	85	°C

(1) Refer to *Application Information* section.
(2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [$T_{A(max)}$] is dependent on the maximum operating junction temperature [$T_{J(max)}$], the maximum power dissipation of the device in the application [$P_{D(max)}$], and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max)} – (\theta_{JA} \times P_{D(max)})$

7.4 Thermal Information

THERMAL METRIC(1)		TPS22965 DSG (8 PINS)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	74.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	35.4	
ψ_{JT}	Junction-to-top characterization parameter	2.2	
ψ_{JB}	Junction-to-board characterization parameter	36.0	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	12.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics, V_{BIAS} = 5.0 V

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature **–40 °C ≤ T_A ≤ 85 °C** (Full) and **V_{BIAS} = 5.0 V**. Typical values are for T_A = 25 °C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
$I_{IN(VBIAS-ON)}$	V_{BIAS} quiescent current	I_{OUT} = 0 mA, V_{IN} = V_{ON} = V_{BIAS} = 5.0 V		Full		50	75	µA
$I_{IN(VBIAS-OFF)}$	V_{BIAS} shutdown current	V_{ON} = GND, V_{OUT} = 0 V		Full			2	µA
$I_{IN(VIN-OFF)}$	V_{IN} off-state supply current	V_{ON} = GND, V_{OUT} = 0 V	V_{IN} = 5.0 V	Full		0.2	8	µA
			V_{IN} = 3.3 V			0.02	3	
			V_{IN} = 1.8 V			0.01	2	
			V_{IN} = 0.8 V			0.005	1	
I_{ON}	ON pin input leakage current	V_{ON} = 5.5 V		Full			0.5	µA
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance	I_{OUT} = –200 mA, V_{BIAS} = 5.0 V	V_{IN} = 5.0 V	25°C		16	23	mΩ
				Full			25	
			V_{IN} = 3.3 V	25°C		16	23	mΩ
				Full			25	
			V_{IN} = 1.8 V	25°C		16	23	mΩ
				Full			25	
			V_{IN} = 1.5 V	25°C		16	23	mΩ
				Full			25	
			V_{IN} = 1.2 V	25°C		16	23	mΩ
				Full			25	
			V_{IN} = 0.8 V	25°C		16	23	mΩ
				Full			25	
R_{PD}	Output pull-down resistance	V_{IN} = 5.0 V, V_{ON} = 0 V, I_{OUT} = 15 mA		Full		225	300	Ω

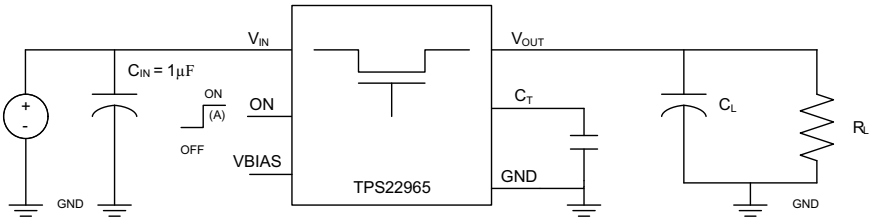
7.6 Electrical Characteristics, V_{BIAS} = 2.5 V

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature **–40 °C ≤ T_A ≤ 85 °C** (Full) and **V_{BIAS} = 2.5 V**. Typical values are for T_A = 25 °C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
$I_{IN(VBIAS-ON)}$	V_{BIAS} quiescent current	I_{OUT} = 0 mA, V_{IN} = V_{ON} = V_{BIAS} = 2.5 V		Full		20	30	µA
$I_{IN(VBIAS-OFF)}$	V_{BIAS} shutdown current	V_{ON} = GND, V_{OUT} = 0 V		Full			2	µA
$I_{IN(VIN-OFF)}$	V_{IN} off-state supply current	V_{ON} = GND, V_{OUT} = 0 V	V_{IN} = 2.5 V	Full		0.01	3	µA
			V_{IN} = 1.8 V			0.01	2	
			V_{IN} = 1.2 V			0.005	2	
			V_{IN} = 0.8 V			0.003	1	
I_{ON}	ON pin input leakage current	V_{ON} = 5.5 V		Full			0.5	µA
RESISTANCE CHARACTERISTICS								
R_{ON}	ON-state resistance	I_{OUT} = –200 mA, V_{BIAS} = 2.5 V	V_{IN} = 2.5 V	25°C		20	26	mΩ
				Full			28	
			V_{IN} = 1.8 V	25°C		19	26	mΩ
				Full			28	
			V_{IN} = 1.5 V	25°C		18	25	mΩ
				Full			27	
			V_{IN} = 1.2 V	25°C		18	25	mΩ
				Full			27	
			V_{IN} = 0.8 V	25°C		17	25	mΩ
				Full			27	
R_{PD}	Output pull-down resistance	V_{IN} = 2.5 V, V_{ON} = 0 V, I_{OUT} = 1 mA		Full		275	325	Ω

7.7 Switching Characteristics

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN} = V_{ON} = V_{BIAS} = 5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		1325		µs
t_{OFF}	Turn-off time			10		
t_R	V_{OUT} rise time			1625		
t_F	V_{OUT} fall time			3.5		
t_D	ON delay time			500		
V_{IN} = 0.8 V, V_{ON} = V_{BIAS} = 5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		600		µs
t_{OFF}	Turn-off time			80		
t_R	V_{OUT} rise time			300		
t_F	V_{OUT} fall time			5.5		
t_D	ON delay time			460		
V_{IN} = 2.5V, V_{ON} = 5 V, V_{BIAS} = 2.5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		2200		µs
t_{OFF}	Turn-off time			9		
t_R	V_{OUT} rise time			2275		
t_F	V_{OUT} fall time			3.1		
t_D	ON delay time			1075		
V_{IN} = 0.8 V, V_{ON} = 5 V, V_{BIAS} = 2.5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turn-on time	R_L = 10 Ω, C_L = 0.1 µF, C_T = 1000 pF		1450		µs
t_{OFF}	Turn-off time			60		
t_R	V_{OUT} rise time			875		
t_F	V_{OUT} fall time			5.5		
t_D	ON delay time			1010		



A. Rise and fall times of the control signal is 100 ns.

Figure 1. Test Circuit

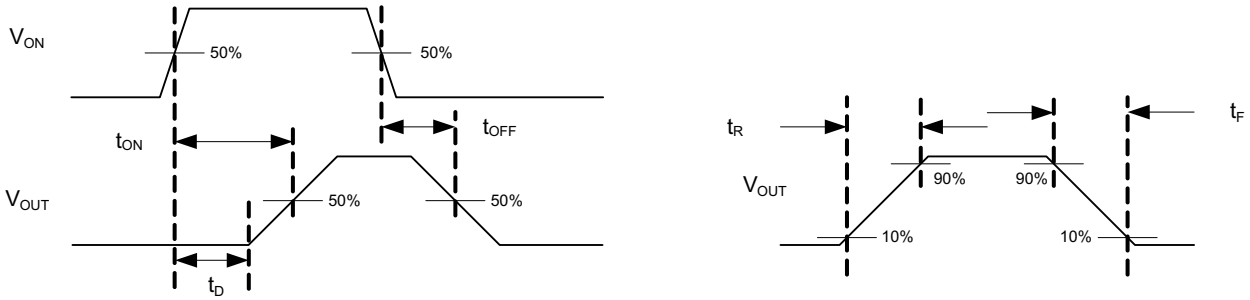
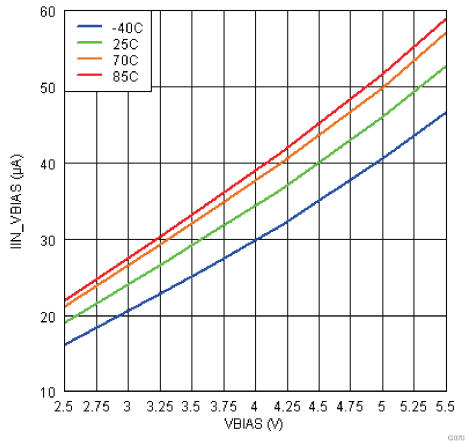


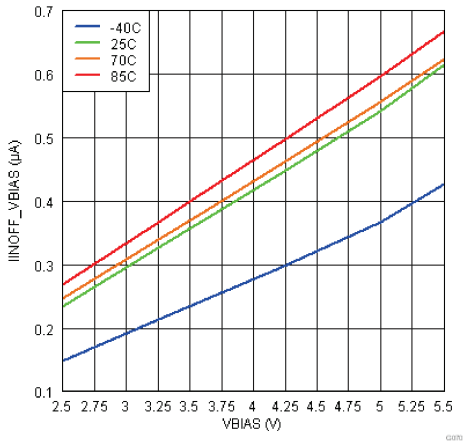
Figure 2. t_{ON}/t_{OFF} Waveforms

7.8 Typical Characteristics



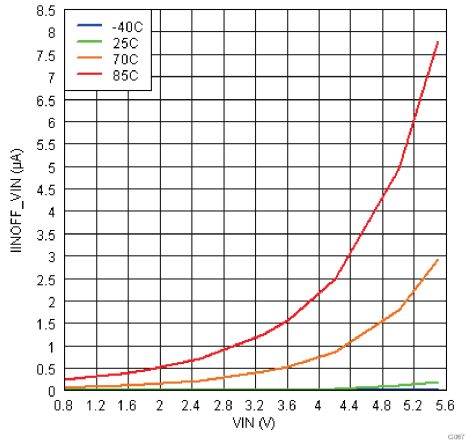
$V_{IN} = V_{BIAS}$ V_{ON} = 5 V V_{OUT} = Open

Figure 3. Quiescent Current vs V_{BIAS}



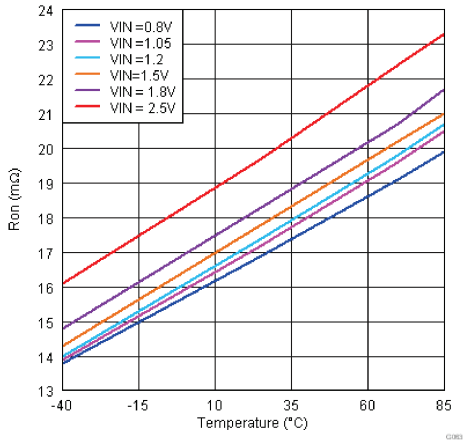
$V_{IN} = V_{BIAS}$ V_{ON} = 0 V V_{OUT} = 0 V

Figure 4. Shutdown Current v. V_{BIAS}



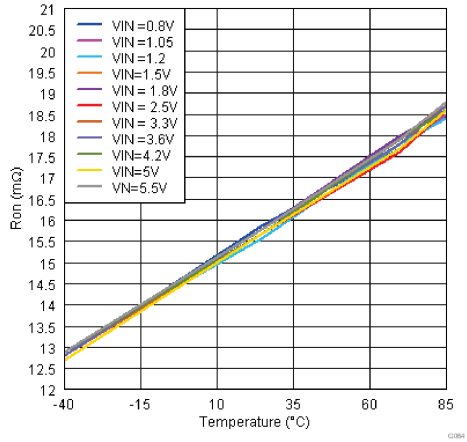
V_{BIAS} = 5.5 V V_{ON} = 0 V V_{OUT} = 0 V

Figure 5. Off-state VIN Current vs V_{IN}



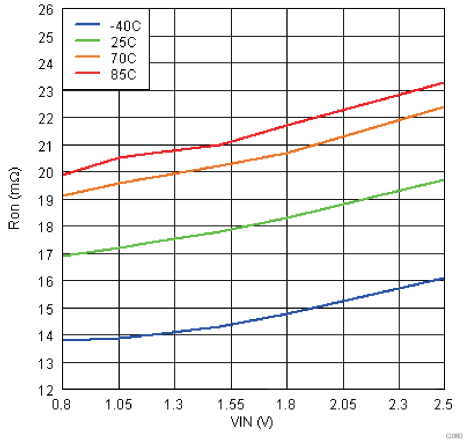
V_{BIAS} = 2.5 V I_{OUT} = –200 mA

Figure 6. R_{ON} vs Temperature



V_{BIAS} = 5.5 V I_{OUT} = –200 mA

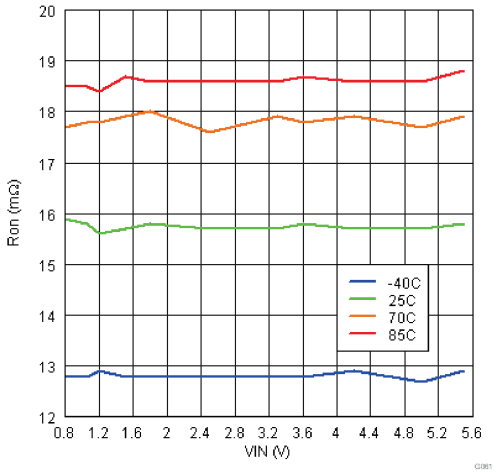
Figure 7. R_{ON} vs Temperature



V_{BIAS} = 2.5 V I_{OUT} = –200 mA

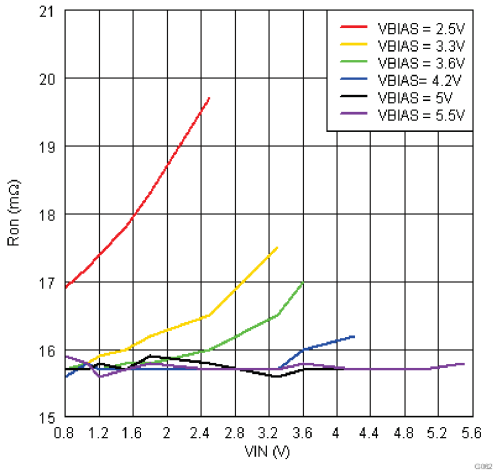
Figure 8. R_{ON} vs V_{IN}

Typical Characteristics (continued)



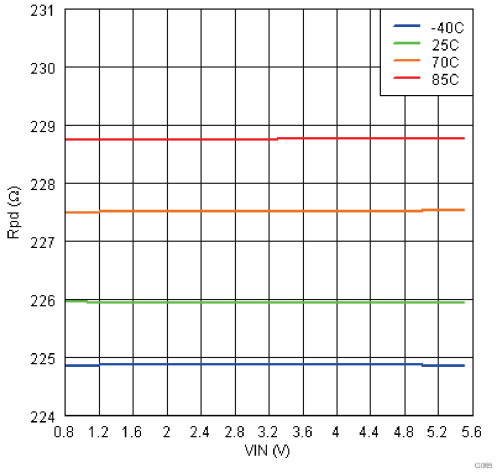
V_{BIAS} = 5.5 V I_{OUT} = –200 mA

Figure 9. R_{ON} vs V_{IN}



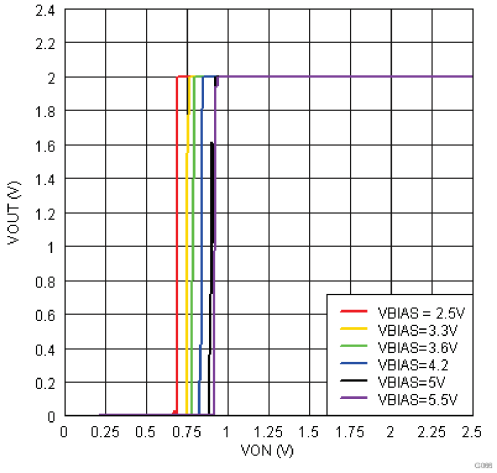
T_A = 25 °C I_{OUT} = –200 mA

Figure 10. R_{ON} vs V_{IN}



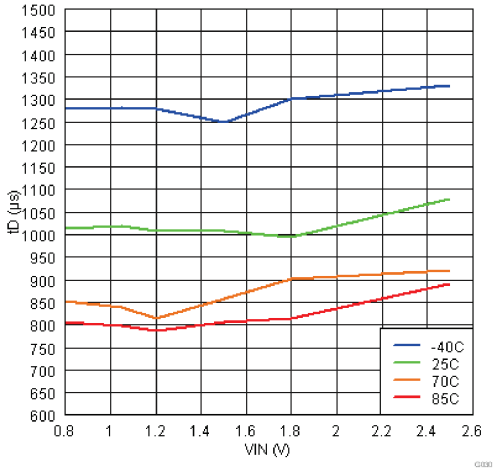
V_{BIAS} = 5.5 V V_{ON} = 0 V IPD = 1 mA

Figure 11. R_{PD} vs V_{IN}



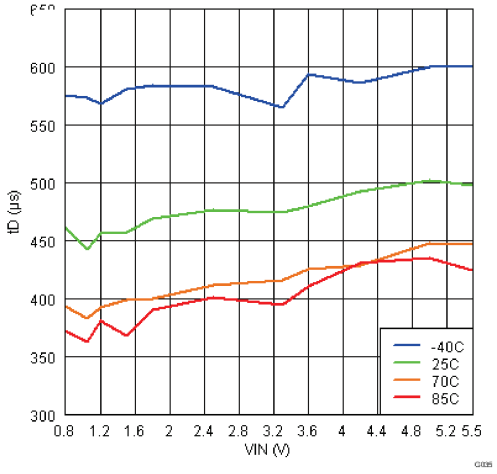
T_A = 25 °C V_{IN} = 2 V

Figure 12. V_{OUT} vs V_{ON}



V_{BIAS} = 2.5 V CT = 1 nF

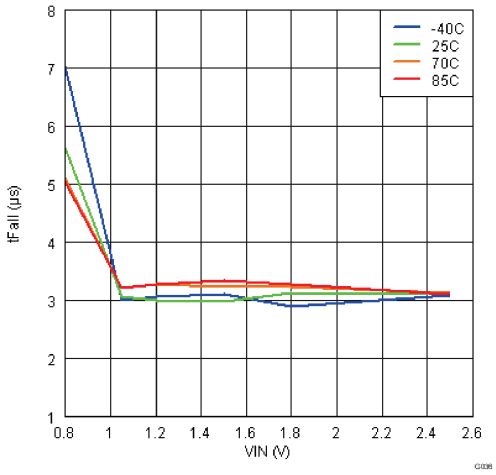
Figure 13. t_D vs V_{IN}



V_{BIAS} = 5.5 V CT = 1 nF

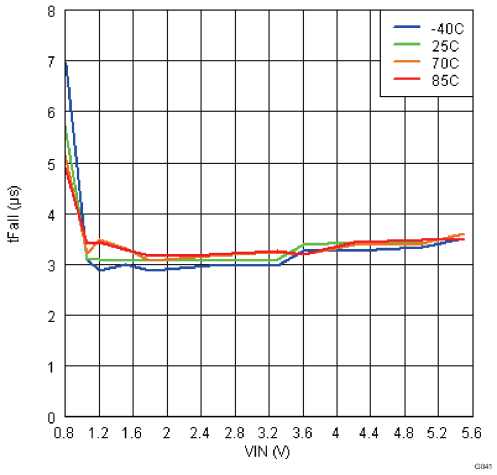
Figure 14. t_D vs V_{IN}

Typical Characteristics (continued)



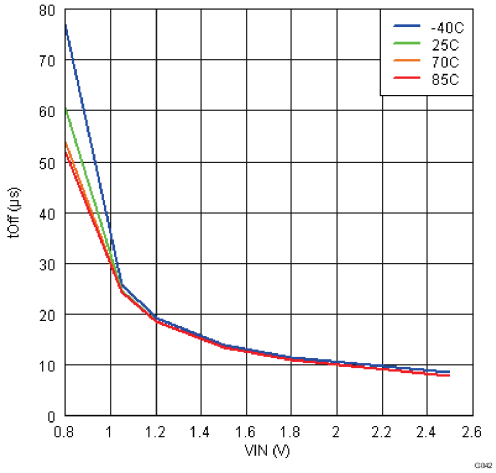
V_{BIAS} = 2.5 V CT = 1 nF

Figure 15. t_F vs V_{IN}



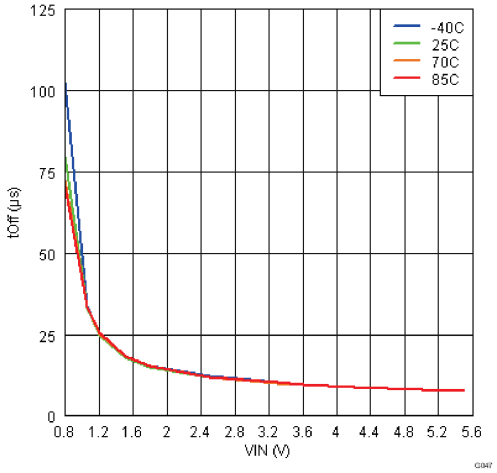
V_{BIAS} = 5.5 V CT = 1 nF

Figure 16. t_F vs V_{IN}



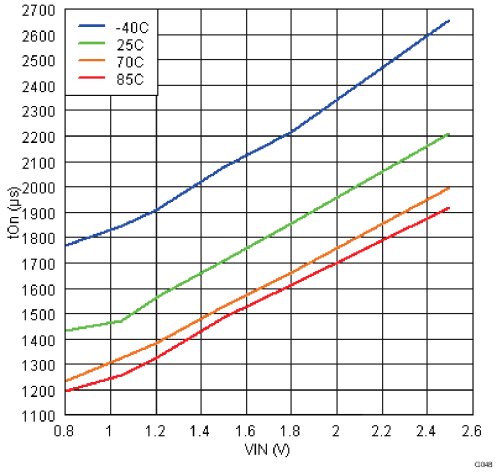
V_{BIAS} = 2.5 V CT = 1 nF

Figure 17. t_{OFF} vs V_{IN}



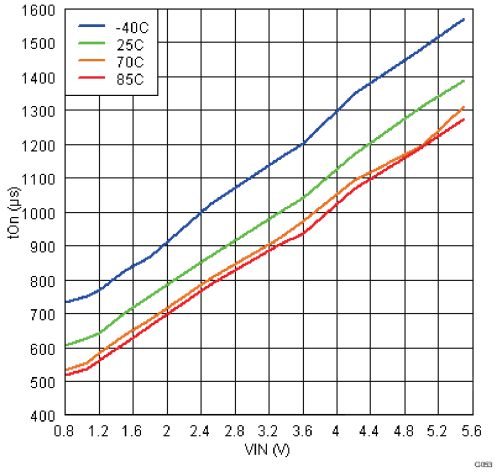
V_{BIAS} = 5.5 V CT = 1 nF

Figure 18. t_{OFF} vs V_{IN}



V_{BIAS} = 2.5 V CT = 1 nF

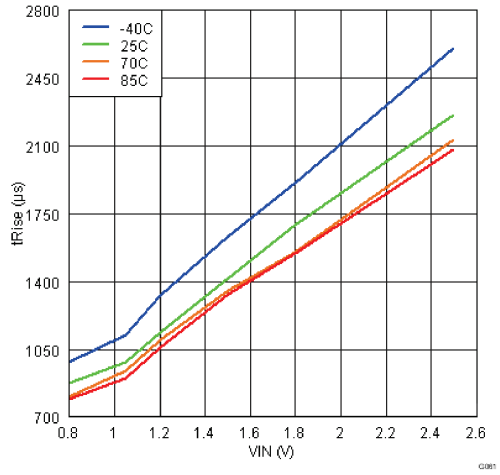
Figure 19. t_{ON} vs V_{IN}



V_{BIAS} = 5.5 V CT = 1 nF

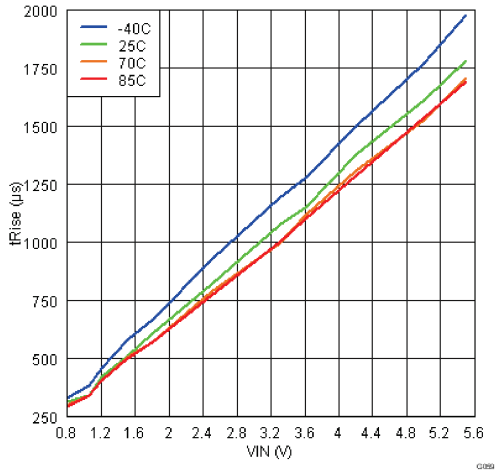
Figure 20. t_{ON} vs V_{IN}

Typical Characteristics (continued)



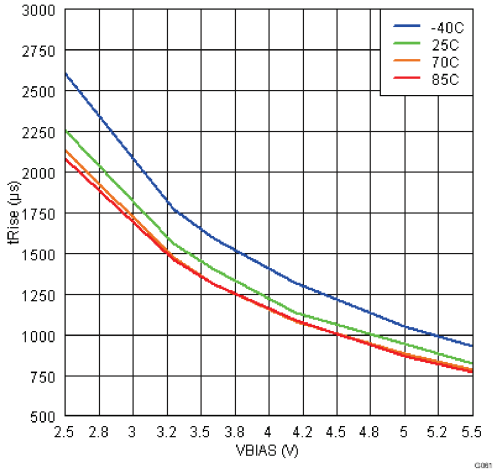
V_{BIAS} = 2.5 V CT = 1 nF

Figure 21. t_R vs V_{IN}



V_{BIAS} = 5.5 V CT = 1 nF

Figure 22. t_R vs V_{IN}

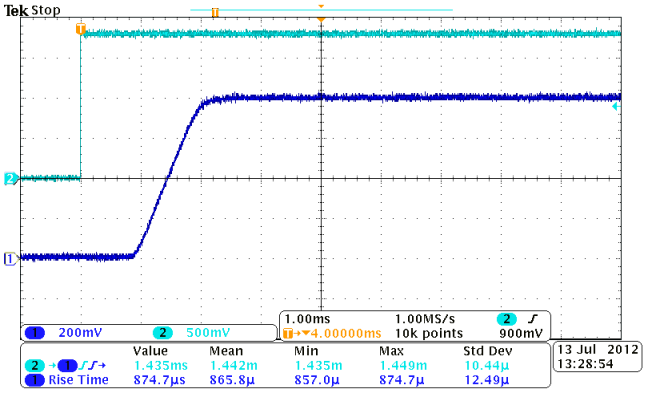


V_{IN} = 2.5 V CT = 1 nF

Figure 23. t_R vs V_{BIAS}

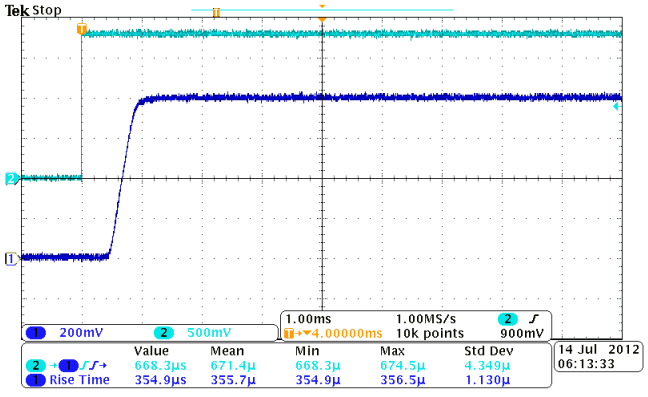
7.9 Typical Switching Characteristics

T_A = 25 °C, C_T = 1 nF, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω, CH1 = V_{OUT}, CH2 = V_{ON}



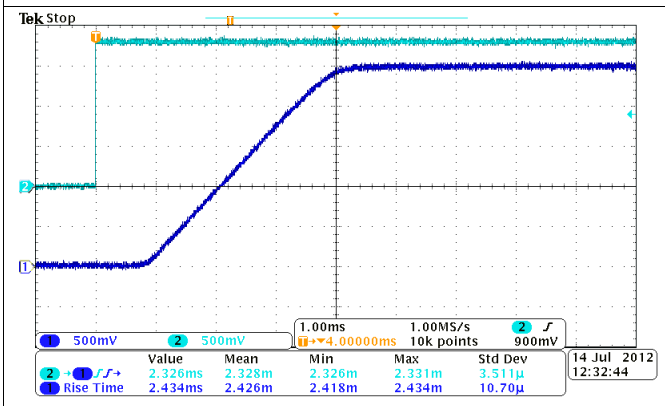
V_{IN} = 0.8 V V_{BIAS} = 2.5 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

Figure 24. Turn-on Response Time



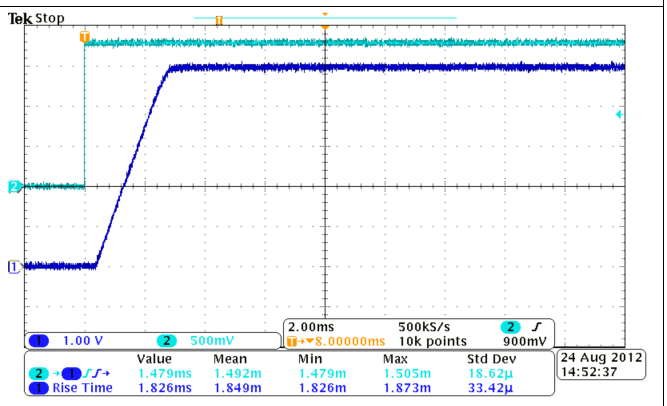
V_{IN} = 0.8 V V_{BIAS} = 5.0 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

Figure 25. Turn-on Response Time



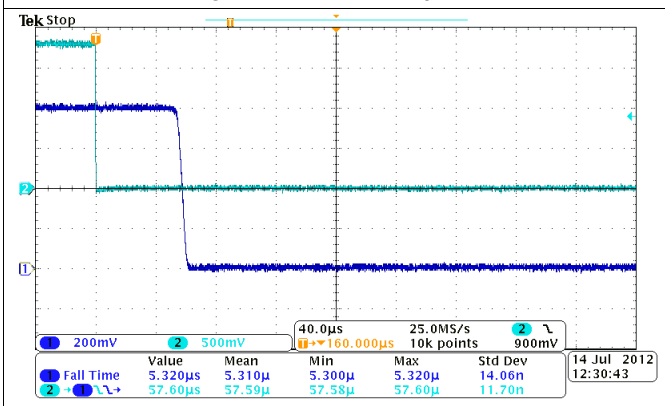
V_{IN} = 2.5 V V_{BIAS} = 2.5 V C_{IN} = 1 µF,
C_L = 0.1 µF R_L = 10 Ω

Figure 26. Turn-on Response Time



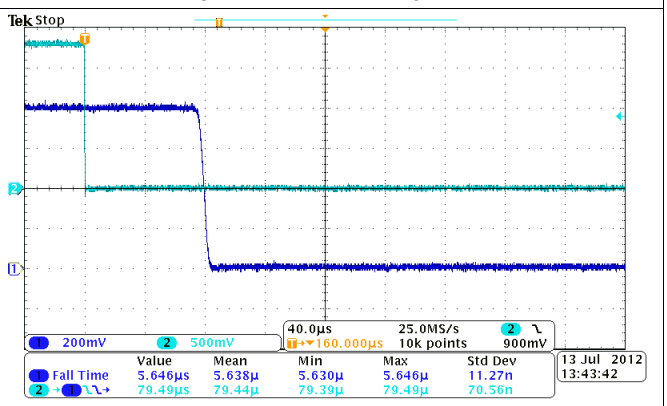
V_{IN} = 5.0 V V_{BIAS} = 5.0 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

Figure 27. Turn-off Response Time



V_{IN} = 0.8 V V_{BIAS} = 2.5 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

Figure 28. Turn-off Response Time

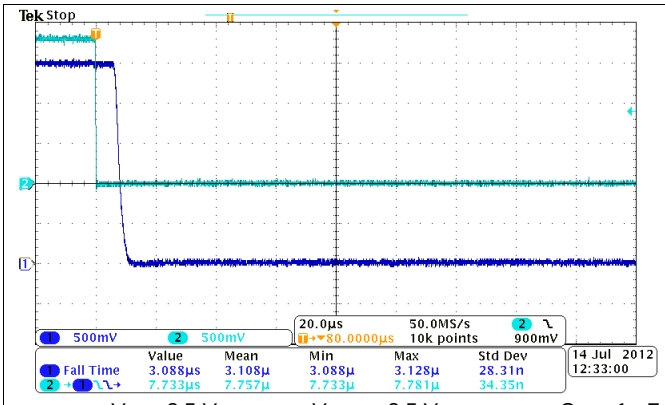


V_{IN} = 0.8 V V_{BIAS} = 5.0 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

Figure 29. Turn-on Response Time

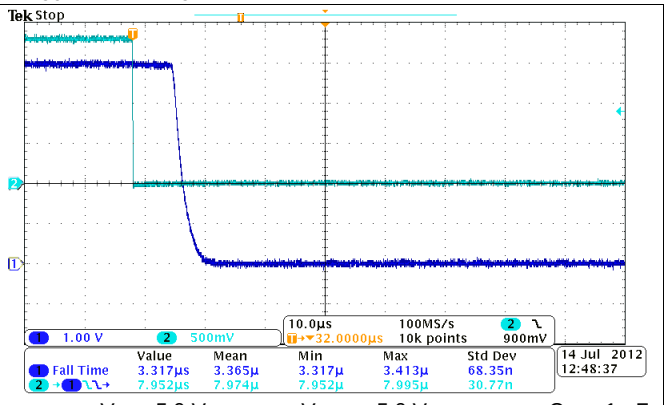
Typical Switching Characteristics (continued)

T_A = 25 °C, C_T = 1 nF, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω, CH1 = V_{OUT}, CH2 = V_{ON}



V_{IN} = 2.5 V V_{BIAS} = 2.5 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

Figure 30. Turn-off Response Time



V_{IN} = 5.0 V V_{BIAS} = 5.0 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω)

Figure 31. Turn-off Response Time

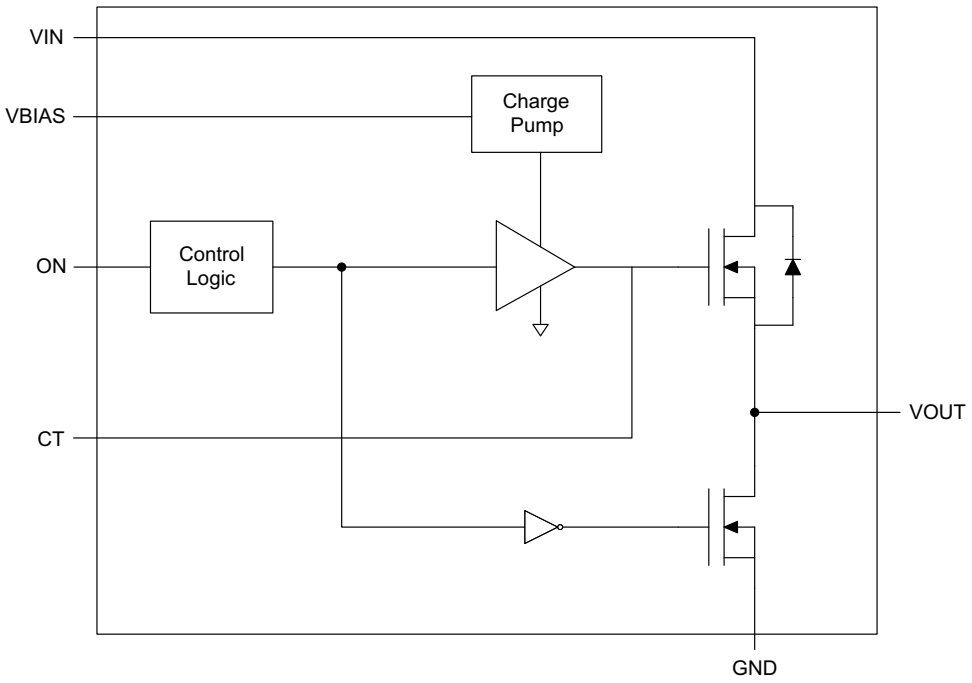
8 Detailed Description

8.1 Overview

The device is a single channel, 6-A load switch in an 8-terminal SON package. To reduce the voltage drop in high current rails, the device implements an ultra-low resistance N-channel MOSFET. The device has a programmable slew rate for applications that require specific rise-time.

The device has very low leakage current during off state. This prevents downstream circuits from pulling high standby current from the supply. Integrated control logic, driver, power supply, and output discharge FET eliminates the need for any external components, which reduces solution size and bill of materials (BOM) count.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Adjustable Rise Time

A capacitor to GND on the CT terminal sets the slew rate. The voltage on the CT terminal can be as high as 12 V. Therefore, the minimum voltage rating for the CT cap should be 25 V for optimal performance. An approximate formula for the relationship between CT and slew rate when V_{BIAS} is set to 5 V is shown in Equation 1 below. This equation accounts for 10% to 90% measurement on V_{OUT} and does **NOT** apply for CT = 0 pF. Use table below to determine rise times for when CT = 0 pF.

$$SR = 0.39 \times CT + 13.4 \quad (1)$$

Where,

SR = slew rate (in µs/V)
CT = the capacitance value on the CT terminal (in pF)
The units for the constant 13.4 are µs/V. The units for the constant 0.39 are µs/(V*pF).

Rise time can be calculated by multiplying the input voltage by the slew rate. The table below contains rise time values measured on a typical device. Rise times shown below are only valid for the power-up sequence where V_{IN} and V_{BIAS} are already in steady state condition before the ON terminal is asserted high.

Table 1. Rise Time vs CT Capacitor

CT (pF)	RISE TIME (µs) 10% - 90%, C_L = 0.1 µF, C_{IN} = 1 µF, R_L = 10 Ω, V_{BIAS} = 5 V TYPICAL VALUES at 25°C with a 25V X7R 10% CERAMIC CAPACITOR on CT						
	VIN = 5 V	VIN = 3.3 V	VIN = 1.8 V	VIN = 1.5 V	VIN = 1.2 V	VIN = 1.05 V	VIN = 0.8 V
0	127	93	62	55	51	46	42
220	475	314	188	162	141	125	103
470	939	637	359	304	255	218	188
1000	1869	1229	684	567	476	414	344
2200	4020	2614	1469	1211	1024	876	681
4700	8690	5746	3167	2703	2139	1877	1568
10000	18360	12550	6849	5836	4782	4089	3449

8.3.2 Quick Output Discharge

The TPS22965 includes a Quick Output Discharge (QOD) feature. When the switch is disabled, a discharge resistor is connected between VOUT and GND. This resistor has a typical value of 225-Ω and prevents the output from floating while the switch is disabled.

8.3.3 Low Power Consumption During Off State

The I_{SD} V_{IN} supply current is 0.01-µA typical at 1.8-VIN. Typically, the downstream loads would have a significantly higher off-state leakage current. The load switch allows system standby power consumption to be reduced.

8.4 Device Functional Modes

Table 2. Functional Table

ON	VIN to VOUT	VOUT to GND
L	Off	On
H	On	Off

9 Application and Implementation

9.1 Application Information

9.1.1 ON/OFF Control

The ON pin controls the state of the switch. Asserting ON high enables the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic thresholds. It can be used with any microcontroller with 1.2 V or higher GPIO voltage. This pin cannot be left floating and must be driven either high or low for proper functionality.

9.1.2 Input Capacitor (Optional)

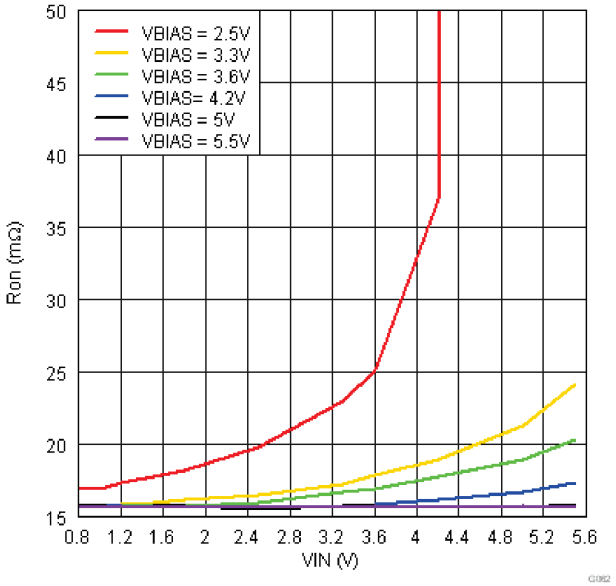
To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between VIN and GND. A 1-µF ceramic capacitor, C_{IN}, placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high current applications. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

9.1.3 Output Capacitor (Optional)

Due to the integrated body diode in the NMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN}. A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup, however a 10 to 1 ratio for capacitance is not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) could cause slightly more V_{IN} dip upon turn-on due to inrush currents. This can be mitigated by increasing the capacitance on the CT pin for a longer rise time (see *Adjustable Rise Time* section below).

9.1.4 V_{IN} and V_{BIAS} Voltage Range

For optimal R_{ON} performance, make sure $V_{IN} \leq V_{BIAS}$. The device will still be functional if $V_{IN} > V_{BIAS}$ but it will exhibit R_{ON} greater than what is listed in the *Electrical Characteristics* table. See Figure 32 for an example of a typical device. Notice the increasing R_{ON} as V_{IN} exceeds V_{BIAS} voltage. Be sure to never exceed the maximum voltage rating for V_{IN} and V_{BIAS}.



T_A = 25 °C I_{OUT} = –200 mA

Figure 32. R_{ON} vs. V_{IN}

9.2 Typical Application

This application demonstrates how the TPS22965 can be used to power downstream modules.

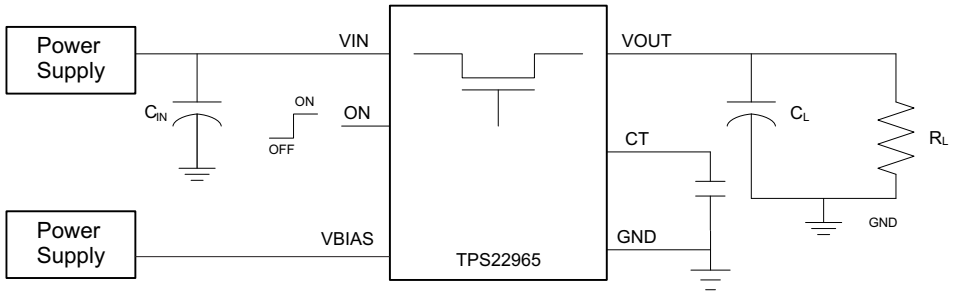


Figure 33. Powering a Downstream Module

9.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	3.3 V
V_{BIAS}	5 V
C_L	22 µF
Maximum Acceptable Inrush Current	400 mA

9.2.2 Detailed Design Procedure

9.2.2.1 Inrush Current

When the switch is enabled, the output capacitors must be charged up from 0-V to the set value (3.3-V in this example). This charge arrives in the form of inrush current. Inrush current can be calculated using the following equation:

$$\text{Inrush Current} = C \times dV/dt \quad (2)$$

Where:

C = output capacitance

dV = output voltage

dt = rise time

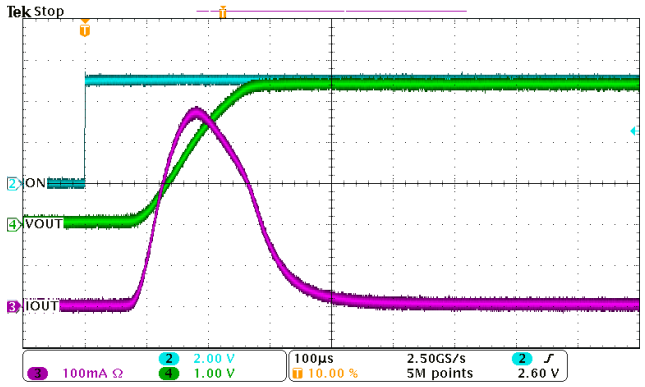
The TPS22965 offers adjustable rise time for VOUT. This feature allows the user to control the inrush current during turn-on. The appropriate rise time can be calculated using the design requirements and the inrush current equation.

$$400\ \text{mA} = 22\ \mu\text{F} \times 3.3\ \text{V}/dt \quad (3)$$

$$dt = 181.5\ \mu\text{s} \quad (4)$$

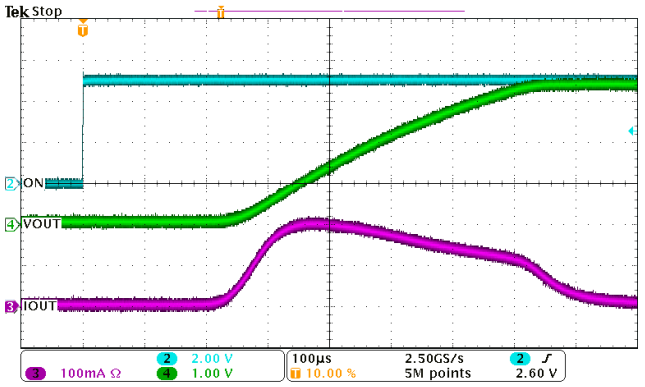
To ensure an inrush current of less than 400 mA, choose a CT value that will yield a rise time of more than 181.5 µs. See the oscilloscope captures below for an example of how the CT capacitor can be used to reduce inrush current.

9.2.3 Application Curves



V_{BIAS} = 5 V V_{IN} = 3.3 V C_L = 22 µF

Figure 34. Inrush Current with CT = 0pF



V_{BIAS} = 5 V V_{IN} = 3.3 V C_L = 22 µF

Figure 35. Inrush Current with CT = 220pF

10 Power Supply Recommendations

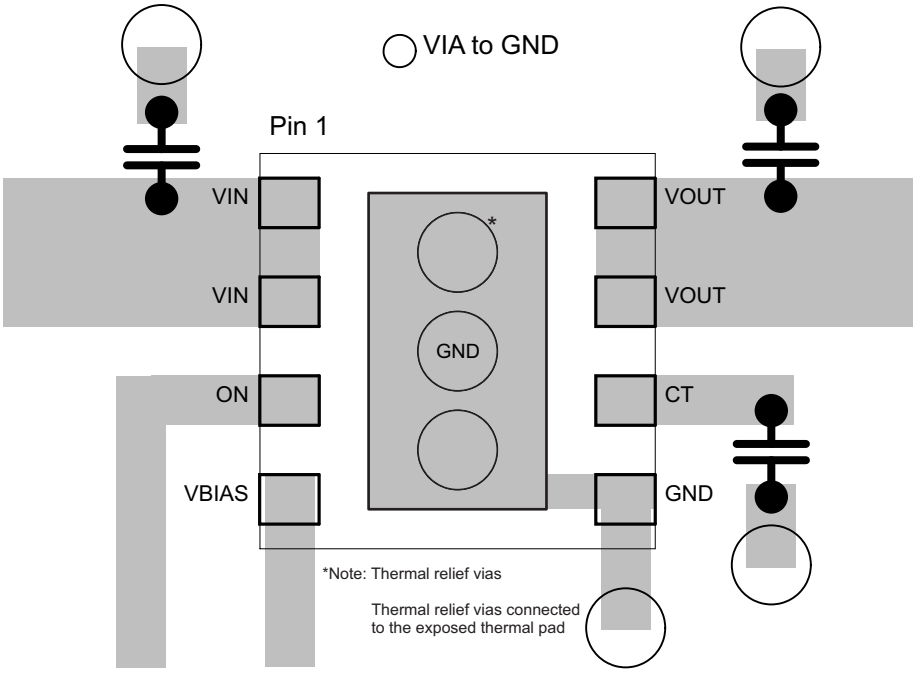
The device is designed to operate from a VBIAS range of 2.5 V to 5.7 V and a VIN range of 0.8 V to VBIAS.

11 Layout

11.1 Layout Guidelines

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance. The CT trace should be as short as possible to avoid parasitic capacitance.

11.2 Layout Example



11.3 Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use the following equation as a guideline:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\Theta_{JA}} \quad (5)$$

Where:

- $P_{D(max)}$ = maximum allowable power dissipation
- $T_{J(max)}$ = maximum allowable junction temperature (125°C for the TPS22965)
- T_A = ambient temperature of the device
- Θ_{JA} = junction to air thermal impedance. See *Thermal Information* section. This parameter is highly dependent upon board layout.

Refer to the *Layout Example*, notice that the thermal vias are located under the exposed thermal pad of the device. This allows for thermal diffusion away from the device.

12 器件和文档支持

12.1 商标

Ultrabook is a trademark of Intel.
All other trademarks are the property of their respective owners.

12.2 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.3 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

13 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22965DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ZSA0	Samples
TPS22965DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ZSA0	Samples
TPS22965NDSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ZDVI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS22965 :

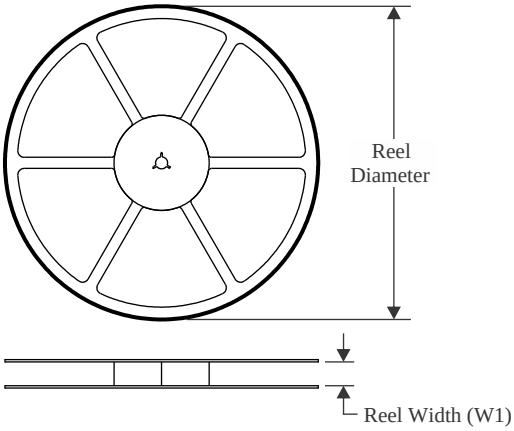
- Automotive : TPS22965-Q1

NOTE: Qualified Version Definitions:

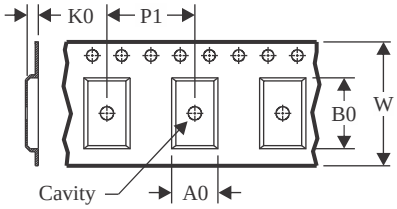
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

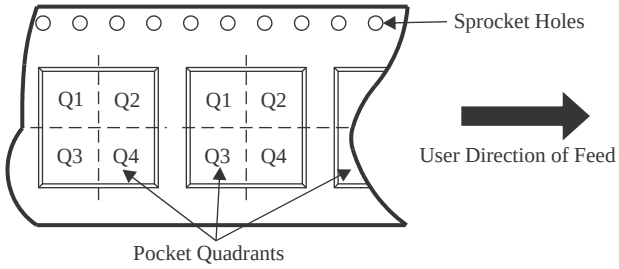


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

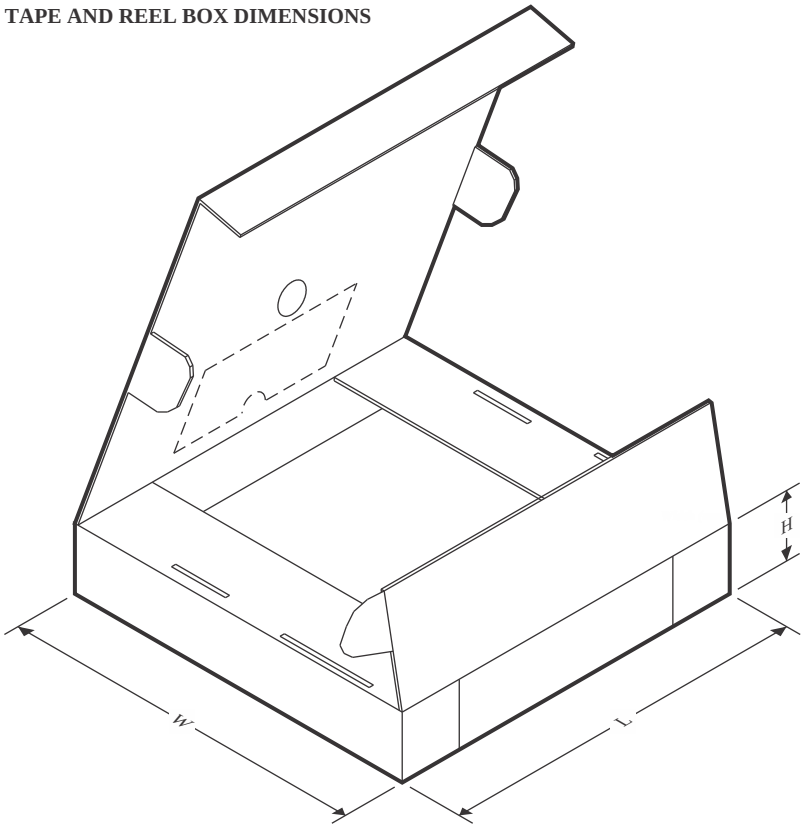
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22965DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS22965DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS22965NDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22965DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TPS22965DSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS22965NDSGR	WSON	DSG	8	3000	182.0	182.0	20.0

GENERIC PACKAGE VIEW

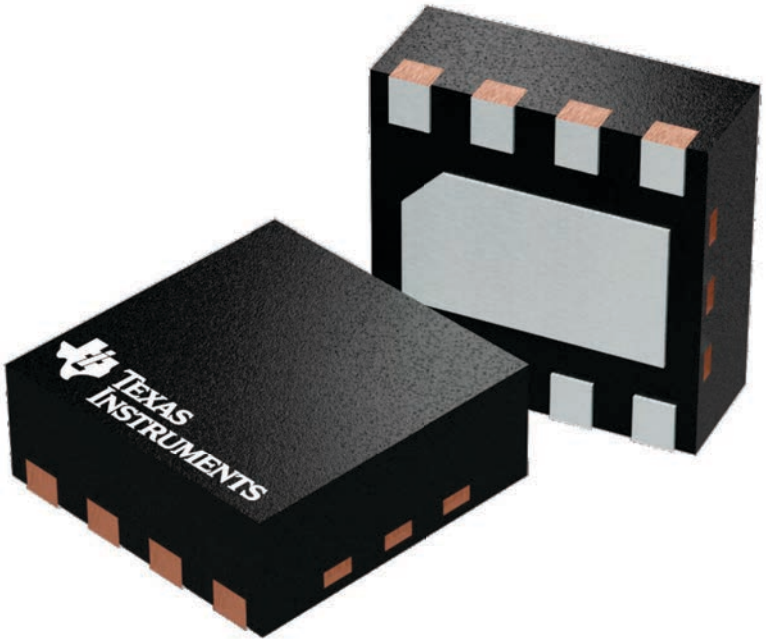
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



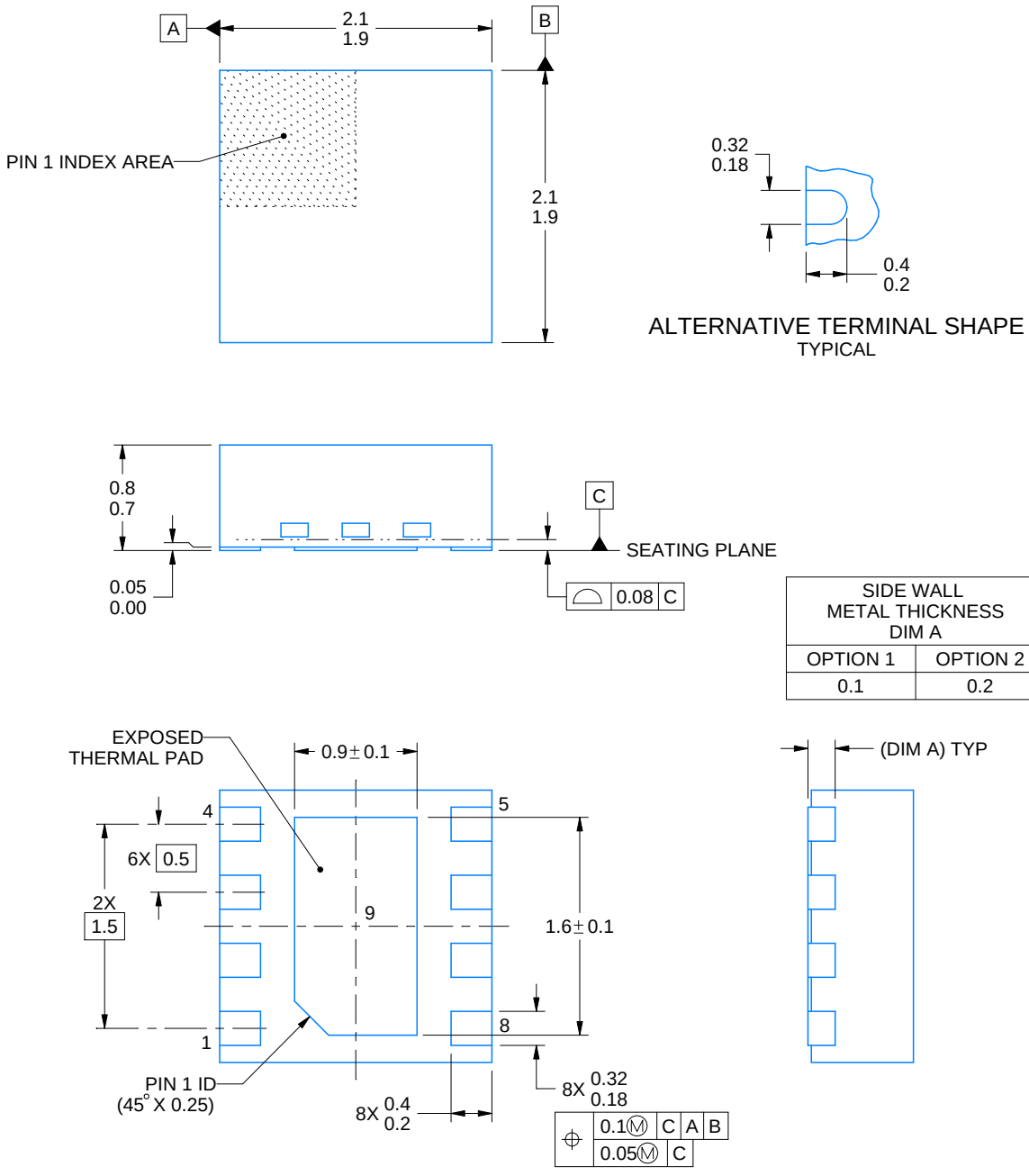
4224783/A

PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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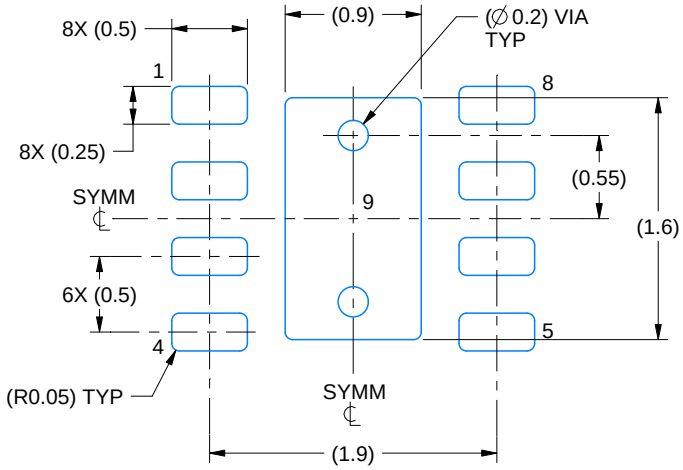
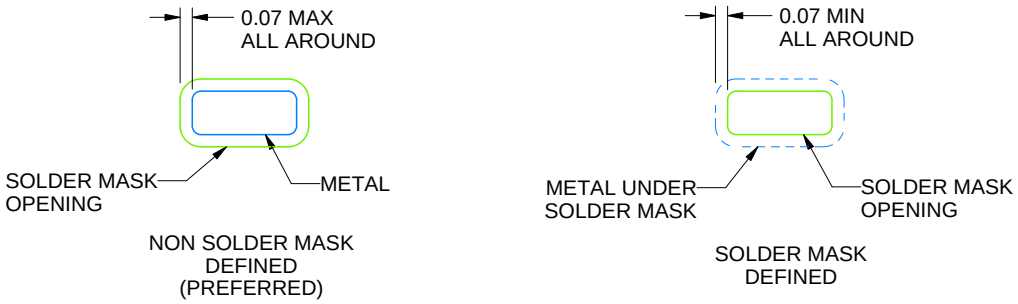
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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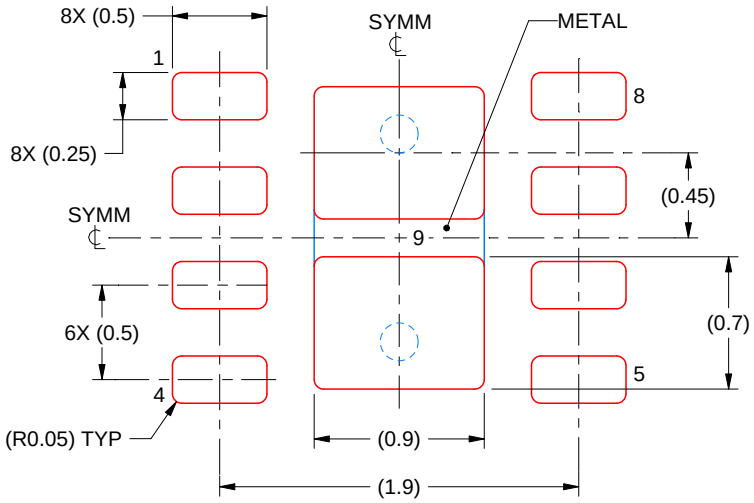
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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