TEXAS INSTRUMENTS
TPS3813K33-Q1, TPS3813I50-Q1
ZHCSKC4H – MAY 2008 – REVISED OCTOBER 2021

TPS3813-Q1 具有窗口看门狗的汽车处理器监控电路

1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度等级 1：–40°C 至 +125°C 环境工作温度范围
  - 器件 HBM 分类等级 2
  - 器件 CDM 分类等级 C4B
- 具有可编程延迟和窗口比率的窗口看门狗
- 6 引脚 SOT-23 封装
- 电源电流 9μA（典型值）
- 具有 25ms 固定延时时间的上电复位发生器
- 精密电源电压监测器 (V_{IT})：2.5V、3V、3.3V、5V
- 开漏复位输出

2 应用

- 车载充电器 (OBC) 和无线充电器
- 驾驶员监控
- 数字驾驶舱处理单元
- ADAS 域控制器
- 汽车远程信息处理控制单元

3 描述

TPS3813-Q1 监控电路主要为 DSP 和基于处理器的系统提供电路初始化和计时监测等功能。

上电期间，$\overline{RESET}$ 引脚会在电源电压 (V_{DD}) 超出 1.1V 时有效。因此，只要 V_{DD} 保持在阈值电压 (V_{IT}) 以下，监控电路就会监测 V_{DD} 并使 $\overline{RESET}$ 引脚保持有效状态。

内部计时器将会延迟输出恢复至无效（高电平）状态的时间，以确保系统正常复位。延时时间 t_d = 25ms（典型值）在 V_{DD} 上升至高于阈值电压 (V_{IT}) 之后开始。当电源电压降至阈值电压 (V_{IT}) 以下时，输出再次变为有效状态（低电平）。无需外部组件。该系列中的所有器件均具有一个通过内部分压器设定的固定感应阈值电压 (V_{IT})。

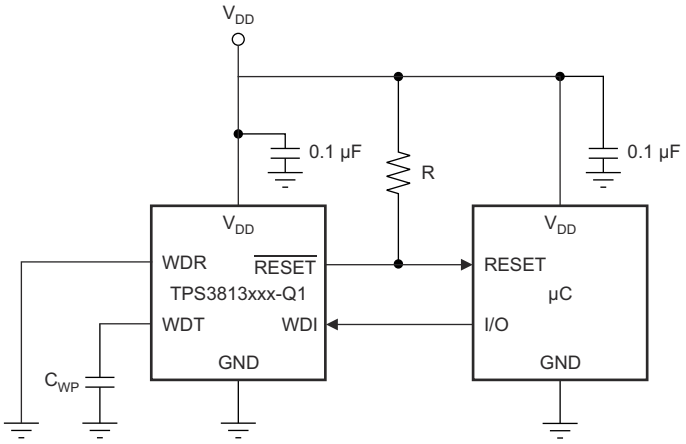
对于安全关键型应用，TPS3813-Q1 系列器件包含具备可编程延迟和窗口比率的窗口看门狗。可以通过将 WDT 引脚连接到 GND 或 V_{DD} 或使用外部电容器来设置看门狗超时的上限。可以通过将 WDR 引脚连接到 GND 或 V_{DD} 来设置下限和窗口比率。如果为看门狗操作不当，$\overline{RESET}$ 引脚将使微控制器复位。

该产品系列专为 2.5V、3V、3.3V 和 5V 电源电压而设计。这些该器件采用 6 引脚 SOT-23 封装。这些器件的工作温度范围为 –40°C 至 125°C。

器件信息

器件型号	封装 (1)	封装尺寸（标称值）
TPS3813K33-Q1	SOT-23 (6)	2.90mm × 1.60mm
TPS3813I50-Q1		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



典型工作电路

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision G (October 2019) to Revision H (October 2021) **Page**

- Changed t_w parameter name to t_{GI_VIT} in *7.6 Timing Requirements* section and added *Glitch immunity* V_{IT} in parameter definition. 6
- Added timing diagram 7
- Added Input Voltage (VDD), VDD Hysteresis, and VDD Glitch Immunity sections into datasheet 10

Changes from Revision F (December 2016) to Revision G (October 2019) **Page**

- Updated text for device conditions on start-up. 9
- Added information to further clarify shaded areas in the Upper and Lower Boundary Visualization 11

Changes from Revision E (October 2016) to Revision F (December 2016) **Page**

- Changed the part numbers in the *Electrical Characteristics* table and deleted references to TPS3813-Q1J25 and TPS3813-Q1L30 6

Changes from Revision D (June 2015) to Revision E (October 2016) **Page**

- Added *+ 1* back to the $t_{window,typ}$ equation in the *Programming Window-Watchdog Using an External Capacitor* section 14

Changes from Revision C (September 2013) to Revision D (June 2015) **Page**

- 删除了数据表中的 TPS38131J25-Q1 和 TPS3813L30-Q1 器件 1
- 添加了 *ESD 等级* 表、*特性说明* 部分、*器件功能模式* 部分、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 1
- Deleted the *Dissipation Ratings* table 6
- Changed the voltage on the V_{DD} pin from 0.6 V to 1.1 V in the *Timing Diagram* figure 12

Changes from Revision B (May 2012) to Revision C (August 2013)	Page
• Deleted banner stating that TPS3813K33-Q1 is *Not Recommended for New Designs*	8

Changes from Revision A (November 2008) to Revision B (April 2012)	Page
• Changed value from 47 pF to 155 pF	14

5 Pin Configuration and Functions

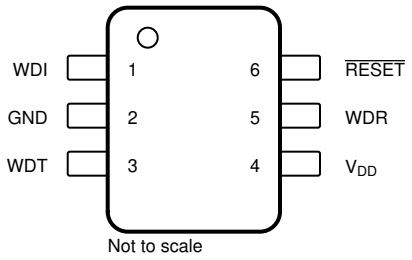


图 5-1. DBV Package
6-Pin SOT-23
Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	WDI	I	Watchdog timer input. This input must be driven at all times and not left floating.
2	GND	I	Ground
3	WDT	I	Programmable watchdog delay input
4	V_{DD}	I	Supply voltage and supervising input
5	WDR	I	Selectable watchdog window ratio input. This input must be tied to V_{DD} or GND and not left floating.
6	$\overline{\text{RESET}}$	O	Open-drain reset output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{DD}	Supply voltage (2)	V_{DD}		7	V
		$\overline{RESET}$	–0.3	V_{DD} + 0.3	
		All other pins (2)	–0.3	7	
I_{OL}	Maximum low output current			5	mA
I_{OH}	Maximum high output current			–5	mA
I_{IK}	Input clamp current (V_I < 0 or V_I > V_{DD})			±20	mA
I_{OK}	Output clamp current (V_O < 0 or V_O > V_{DD})			±20	mA
	Continuous total power dissipation		See ♯ 6.4		
T_A	Operating free-air temperature		–40	125	°C
	Soldering temperature			260°C	
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to GND. For reliable operation the device should not be operated at 7 V for more than t = 1000h continuously.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 3, 4, and 6)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

at specified temperature range

		MIN	MAX	UNIT
V_{DD}	Supply voltage	2	6	V
V_I	Input voltage	0	V_{DD} + 0.3	V
V_{IH}	High-level input voltage	0.7 × V_{DD}		V
V_{IL}	Low-level input voltage		0.3 × V_{DD}	V
$\Delta t/\Delta V$	Input transition rise and fall rate		100	ns/V
t_w	Pulse width of WDI trigger pulse	50		ns
T_A	Operating free-air temperature range	–40	125	°C

6.4 Thermal Information

THERMAL METRIC (1)		TPS3813-Q1 DBV (SOT-23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	202.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	164.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	44.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage		V_{DD} = 2 V to 6 V, I_{OL} = 500 µA			0.2	V
			V_{DD} = 3.3 V I_{OL} = 2 mA			0.4	
			V_{DD} = 6 V, I_{OL} = 4 mA			0.4	
	Power up reset voltage (1)		$V_{DD} \geq$ 1.1 V, I_{OL} = 50 µA			0.2	V
V_{IT}	Negative-going input threshold voltage (2)	TPS3813K33-Q1		2.87	2.93	3	V
		TPS3813I50-Q1		4.45	4.55	4.65	
V_{HYS}	Hysteresis	TPS3813K33-Q1			40		mV
		TPS3813I50-Q1			60		
I_{IH}	High-level input current	WDI, WDR	WDI = V_{DD} = 6 V, WDR = V_{DD} = 6 V	–125		125	nA
		WDT	WDT = V_{DD} = 6 V, $V_{DD} > V_{IT}$, $\overline{RESET}$ = High	–125		125	
I_{IL}	Low-level input current	WDI, WDR	WDI = 0 V, WDR = 0 V, V_{DD} = 6 V	–125		125	
		WDT	WDT = 0 V, $V_{DD} > V_{IT}$, $\overline{RESET}$ = High	–125		125	
I_{OH}	High-level output current		$V_{DD} = V_{IT}$ + 0.2 V, $V_{OH} = V_{DD}$			25	nA
I_{DD}	Supply current		V_{DD} = 2 V output unconnected		9	13	µA
			V_{DD} = 5 V output unconnected		20	25	
C_i	Input capacitance		V_I = 0 V to V_{DD}		5		pF

(1) The lowest supply voltage at which $\overline{RESET}$ becomes active. t_r, $V_{DD} \geq$ 15 µs/V.
(2) To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be placed near to the supply terminals.

6.6 Timing Requirements

At R_L = 1 MΩ, C_L = 50 pF, and T_A = –40°C to +125°C.

			MIN	TYP	MAX	UNIT
t_{GI_VIT}	Glitch immunity V_{IT} (Pulse width at V_{DD})	$V_{DD} = V_{IT}$ + 0.2 V, $V_{DD} = V_{IT}$ – 0.2 V	3			µs

6.7 Switching Characteristics

R_L = 1 MΩ, C_L = 50 pF, T_A = –40°C to 125°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_d	Delay time		$V_{DD} \geq V_{IT}$ + 0.2 V (see 图 7-3)	20	25	30	ms
$t_{t(out)}$	Watchdog time-out	Upper limit	WDT = 0 V	0.2	0.25	0.3	s
			WDT = V_{DD}	2	2.5	3	
			WDT = programmable (1)		See (2)		ms
	Watchdog window ratio		WDR = 0 V, WDT = 0 V		1:31.8		
			WDR = 0 V, WDT = V_{DD}		1:32		
			WDR = 0 V, WDT = programmable		1:25.8		
			WDR = V_{DD}, WDT = 0 V		1:124.9		
			WDR = V_{DD}, WDT = V_{DD}		1:127.7		
			WDR = V_{DD}, WDT = programmable		1:64.5		
t_{PHL}	Propagation (delay) time, high-to-low-level output	V_{DD} to $\overline{RESET}$ delay	V_{IL} = V_{IT} – 0.2 V, V_{IH} = V_{IT} + 0.2 V		30	50	µs

(1) 155 pF < $C_{(ext)}$ < 63 nF
(2) ($C_{(ext)}$ / 15.55 pF + 1) × 6.25 ms

6.8 Timing Diagrams

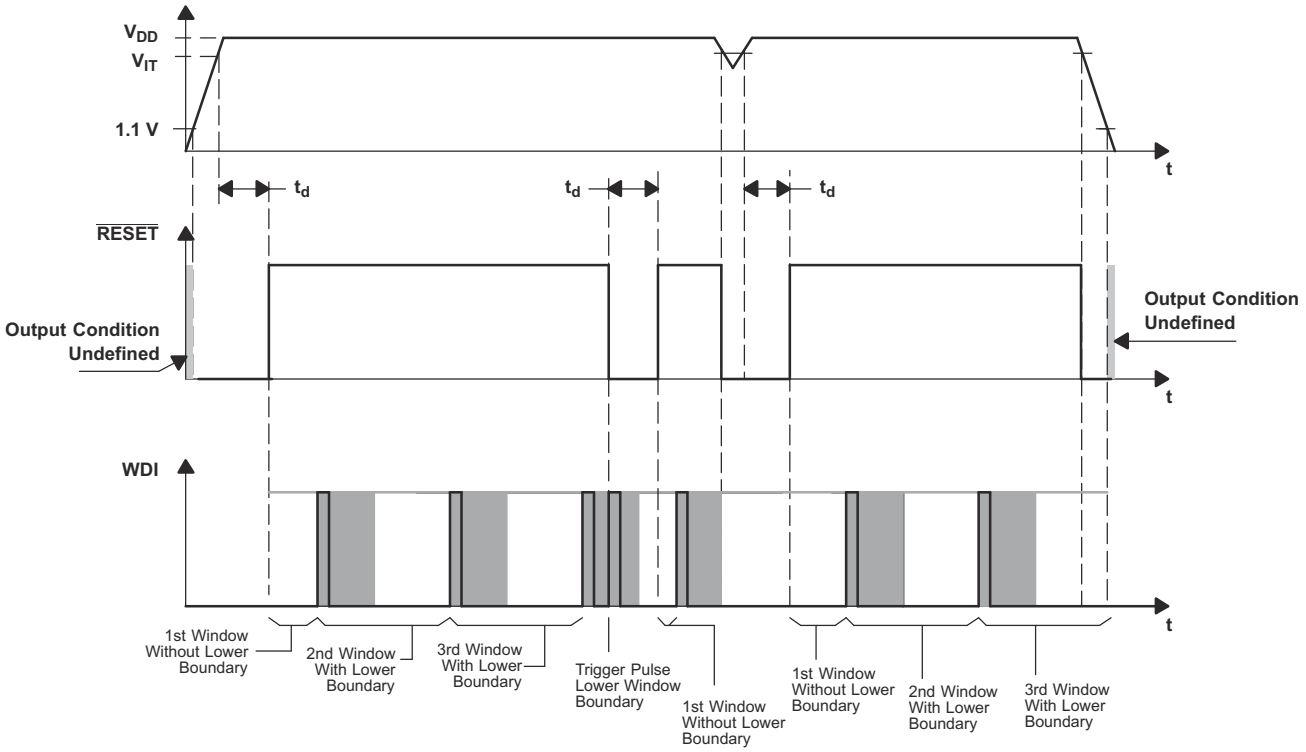
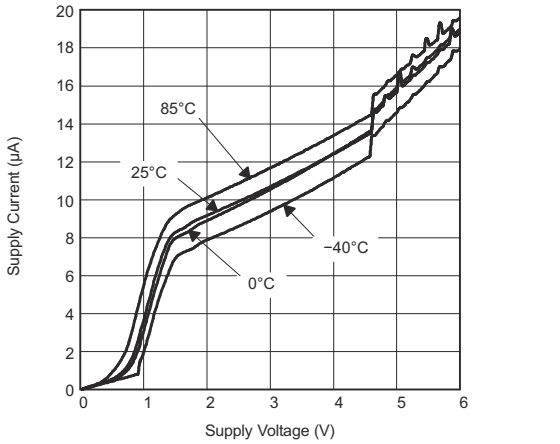


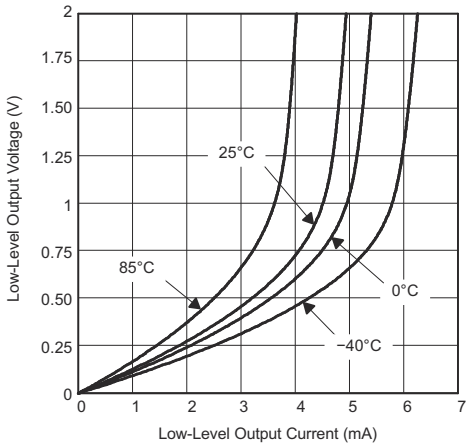
图 6-1. Timing Diagram

6.9 Typical Characteristics



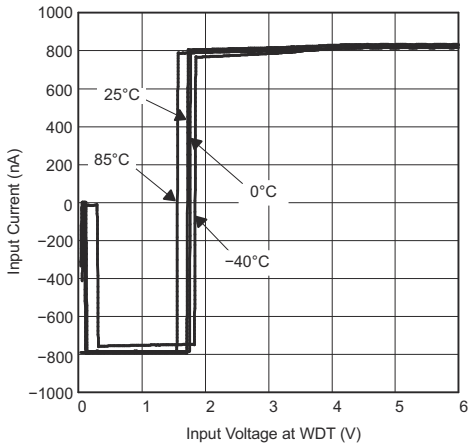
WDI = GND WDT = GND WDR = GND

图 6-2. Supply Current vs Supply Voltage



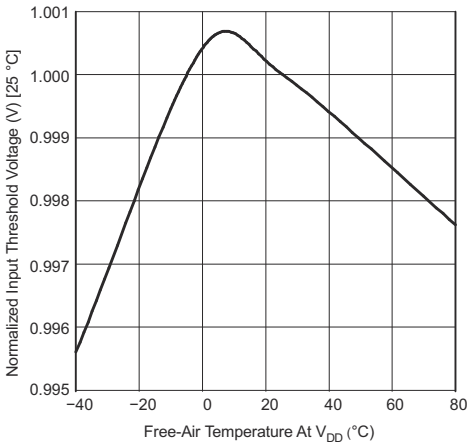
WDI = GND WDT = GND WDR = GND
V_{DD} = 2 V

图 6-3. Low-Level Output Voltage vs Low-Level Output Current



WDI = GND WDR = GND V_{DD} = 6 V

图 6-4. Input Current vs Input Voltage at WDT



WDI = Triggered WDT = GND WDR = GND

图 6-5. Normalized Input Threshold Voltage vs Free-Air Temperature at V_{DD}

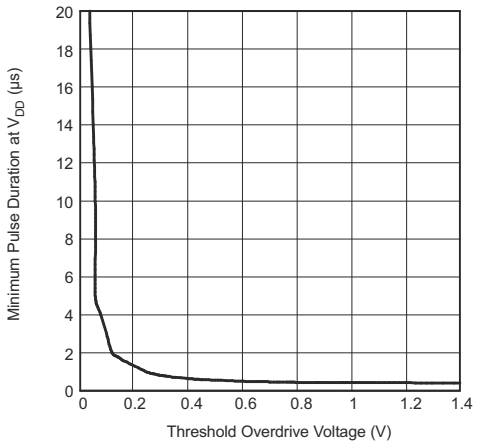


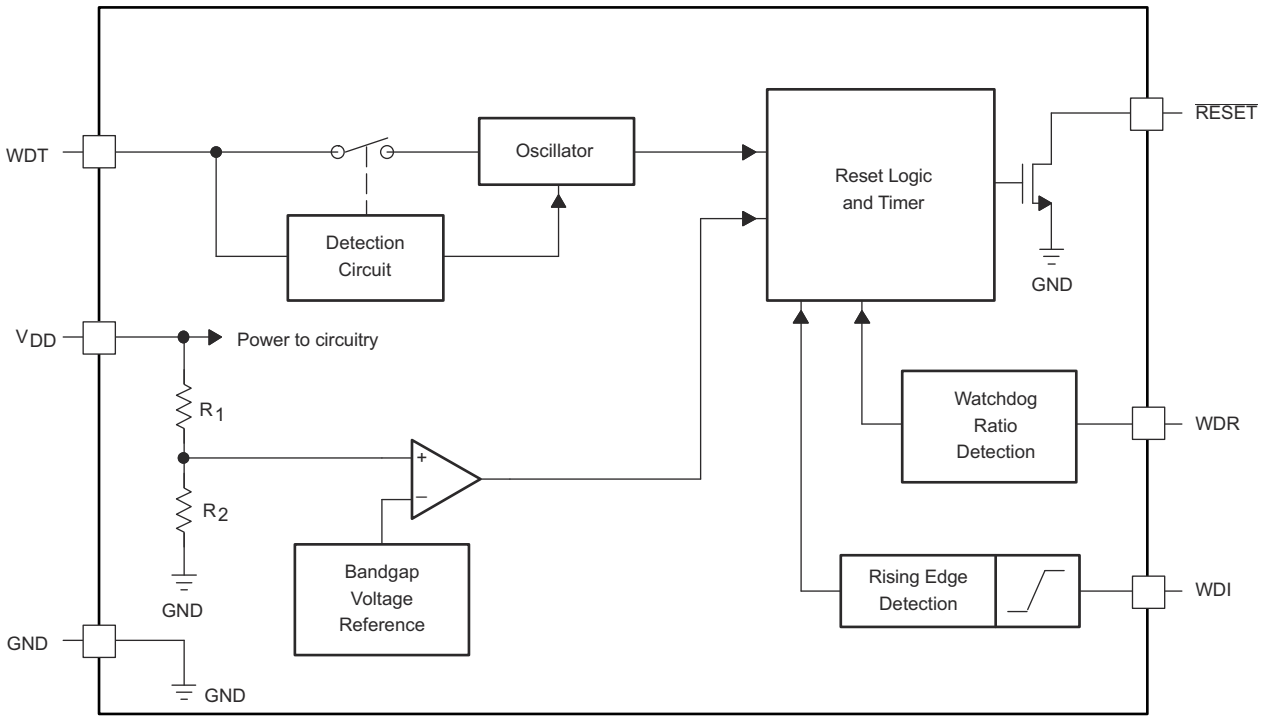
图 6-6. Minimum Pulse Duration At V_{DD} vs V_{DD} Threshold Overdrive Voltage

7 Detailed Description

7.1 Overview

The TPS3813-Q1 devices (TPS3813K33-Q1 and TPS3813I50-Q1) are a family of supervisory circuits with watchdog functionality. The TPS3813-Q1 family of devices is designed to assert a reset on the $\overline{\text{RESET}}$ pin when the supply (V_{DD}) drops below the threshold voltage (V_{IT}) which varies depending on which device is used. When the V_{DD} supply rises above 1.1 V, the $\overline{\text{RESET}}$ pin output state becomes valid and is active in logic low state until the V_{DD} supply crosses the voltage threshold (V_{IT} + V_{HYS}). The watchdog window can be programmed using the WDT and WDR pins with several different configurations, all of which are explained in the following sections.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Voltage (VDD)

VDD pin is monitored by the internal comparator with integrated reference to indicate when VDD falls below the fixed threshold voltage. VDD also functions as the supply for the following:

- Internal bandgap (reference voltage)
- Internal regulator
- State machine
- Buffers
- Other control logic blocks

Good design practice involves placing a 0.1 µF to 1 µF bypass capacitor at VDD input for noisy applications and to ensure enough charge is available for the device to power up correctly. The reset output is undefined when VDD is below V_{POR}.

7.3.1.1 VDD Hysteresis

The internal comparator has built-in hysteresis to avoid erroneous output reset release. If the voltage at the VDD pin falls below the falling voltage threshold V_{IT}, the output reset is asserted. When the voltage at the VDD pin rises above the rising voltage threshold (V_{IT+} = V_{IT} + V_{HYS}), the output reset is deasserted after t_D reset time delay.

7.3.1.2 VDD Glitch Immunity

These devices are immune to quick voltage transient or excursion on VDD. Sensitivity to transients depends on both pulse duration (t_{GI_VIT}) found in 节 6.6 and transient overdrive. Overdrive is defined by how much VDD exceeds the specified threshold. Threshold overdrive is calculated as a percent of the threshold in question, as shown in 方程式 1.

$$\text{Overdrive} = | ((VDD / V_{IT}) - 1) \times 100\% | \quad (1)$$

where

- V_{IT} = V_{IT-} is the threshold voltage
- V_{IT+} = V_{IT} + V_{HYS} is the rising threshold voltage
- VDD is the input voltage crossing V_{IT}

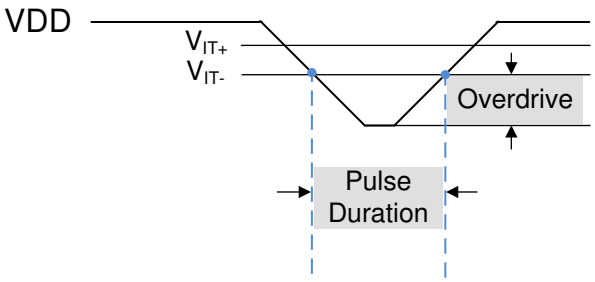


图 7-1. Overdrive Versus Pulse Duration

TPS3813-Q1 devices have built-in glitch immunity (t_{GI_VIT-}) as shown in 节 6.6. 图 7-1 shows that VDD must fall below V_{IT} for t_{GI_VIT}, otherwise the faling transistion is ignored. When VDD falls below V_{IT} for t_{GI_VIT}, $\overline{\text{RESET}}$ transitions low to indicate a fault condition after the propagation delay high-to-low (t_{PHL}). When VDD rises above V_{IT+} = V_{IT} + V_{HYS}, $\overline{\text{RESET}}$ deasserts to a logic high indicating there is no more fault condition only if VDD remains above V_{IT+} for longer than the reset delay (t_D).

7.3.2 Implemented Window-Watchdog Settings

The watchdog window can be set up in two different ways. The first way is to use the implemented timing, which is a default setting. The other way is to activate the default settings by wiring the WDT and WDR pin to V_{DD} or GND. Four different timings available with these settings which are listed in 表 7-1.

表 7-1. Window-Watchdog Configuration Settings

SELECTED OPERATION MODE		t_{window}	$t_{boundary}$
WDT = 0 V	WDR = 0 V	Max = 0.3 s	Max = 9.46 ms
		Typ = 0.25 s	Typ = 7.86 ms
		Min = 0.2 s	Min = 6.27 ms
	WDR = V_{DD}	Max = 0.3 s	Max = 2.43 ms
		Typ = 0.25 s	Typ = 2 ms
		Min = 0.2 s	Min = 1.58 ms
WDT = V_{DD}	WDR = 0 V	Max = 3 s	Max = 93.8 ms
		Typ = 2.5 s	Typ = 78.2 ms
		Min = 2 s	Min = 62.5 ms
	WDR = V_{DD}	Max = 3 s	Max = 23.5 ms
		Typ = 2.5 s	Typ = 19.6 ms
		Min = 2 s	Min = 15.6 ms

See 图 7-2 to visualize the values named in the table. The upper boundary of the window frame is defined by t_{window} and the lower boundary of the window frame is defined by $t_{boundary}$. 表 7-1 describes the upper and lower boundary settings. The device must detect a rising edge at the WDI pin between $t_{boundary,max}$ and $t_{window,min}$ to prevent asserting a reset. The values in 表 7-1 are typical and worst case conditions and are valid over the whole temperature range of –40°C to +125°C.

The shaded areas shown in 图 7-2 are cases where undefined operation may happen. This device may not detect a violation if a WDI pulse occurs within these three shaded areas. The first shaded area addresses the situation of two consecutive rising edges occur within a quick amount of time. The typical time between rising edges should be more than 500 µs. The second and third shaded areas are defined by the min and max variance of the lower boundary ($t_{boundary}$) and upper boundary (t_{window}). Set the WDI rising edge within the $t_{boundary,max}$ and $t_{window,min}$ for correct operation.

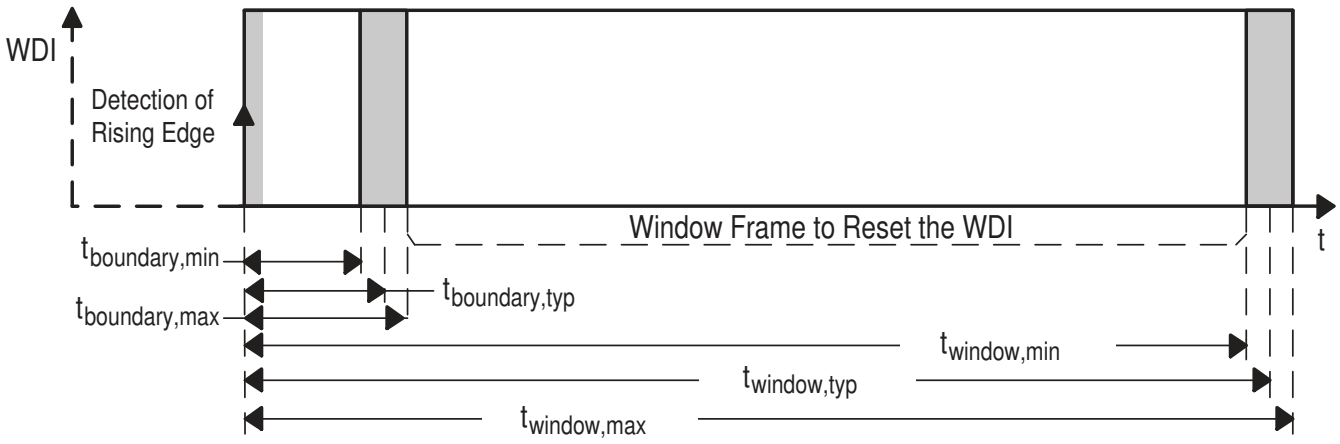


图 7-2. Upper and Lower Boundary Visualization

7.3.2.1 Timing Rules of Window-Watchdog

After the reset of the supervisor is released, the lower boundary of the first WDI window is disabled. However, after the first WDI pulse low-to-high transition is detected, the lower boundary function of the window is enabled. All further WDI pulses must fit into the configured window frame.

The lower boundary of the watchdog window begins with the rising edge of the WDI trigger pulse. At the same time, all internal timers are reset. If an external capacitor is used, the lower boundary is impacted because of the different oscillator frequency. See the 节 *8.2.2.1* section for additional details. 图 7-3, especially the shaded boundary area, was prepared in a nonreal ratio scale to better visualize the description.

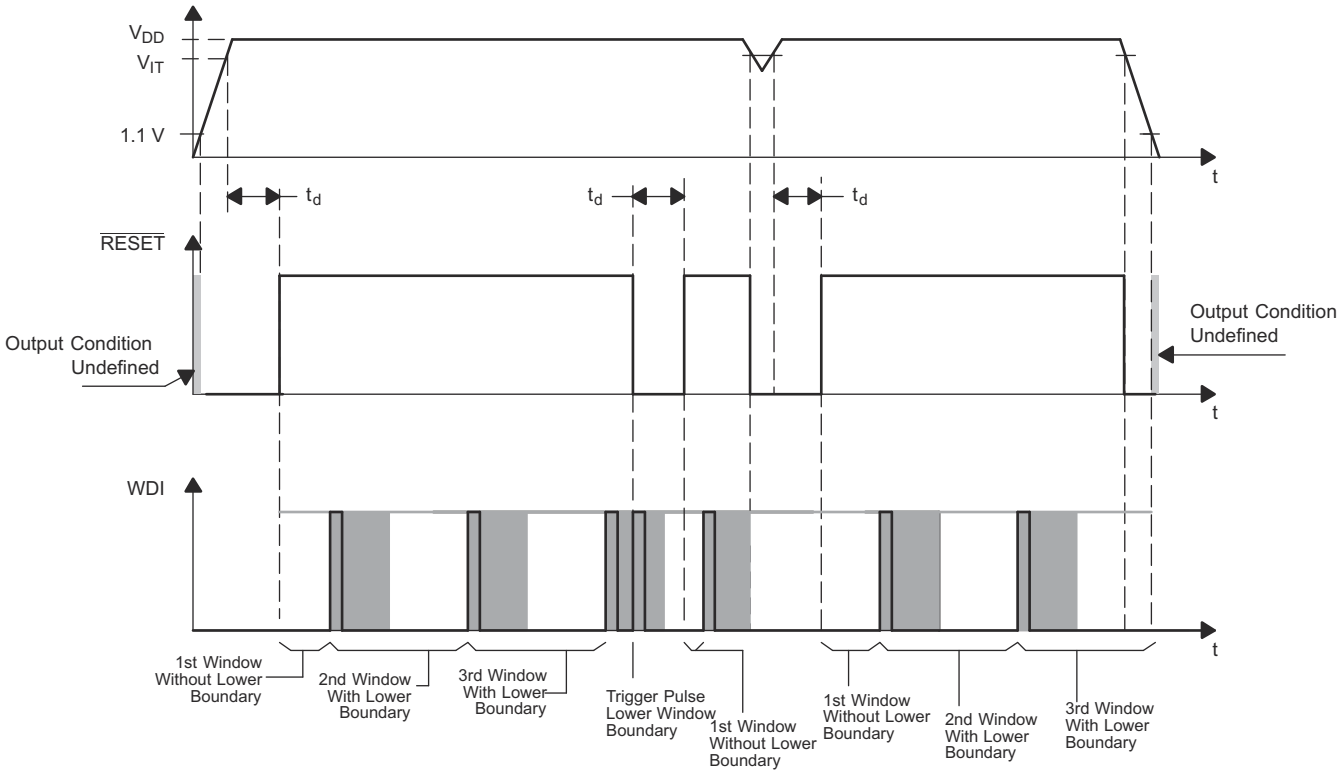


图 7-3. Timing Diagram

7.3.3 Watchdog Software Considerations

To benefit from the window watchdog feature and help the watchdog timer monitor the software execution more closely, TI recommends that the watchdog be set and reset at different points in the program rather than pulsing the watchdog input periodically by using the prescaler of a microcontroller or DSP. Furthermore, the watchdog trigger pulses should be set to different timings inside the window frame to release a defined reset if the program should hang in any subroutine. This setting allows the window watchdog to detect timeouts of the trigger pulse as well as pulses that distort the lower boundary.

7.4 Device Functional Modes

The functional mode for the TPS3813-Q1 family family of devices is either on or reset. 表 7-2 lists the device truth table.

表 7-2. Device States

CONDITION	STATE	$\overline{\text{RESET}}$
$V_{DD} > V_{IT}$	On	H
$V_{DD} < V_{IT}$	Reset	L
Watchdog fault		

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

8.1.1 Lower-Boundary Calculation

The lower boundary can be calculated based on the values listed in the *节 6.7* table. Additionally, facts must be taken into account to verify that the lower boundary is where it is expected. Because the internal oscillator of the window watchdog is running free, any rising edge at the WDI pin is taken into account at the next internal clock cycle. Accounting for any rising edge at the WDI pin occurs regardless of the external source. Because the shift between internal and external clock is not known, consider the worst-case condition when calculating this value.

表 8-1. Watchdog Lower-Boundary Calculation

SELECTED OPERATION MODE		LOWER BOUNDARY OF FRAME
WDT = external capacitor $C_{(ext)}$	WDR = 0 V	$t_{boundary,max} = t_{window,max} / 23.5$
		$t_{boundary,typ} = t_{window,typ} / 25.8$
		$t_{boundary,min} = t_{window,min} / 28.7$
	WDR = V_{DD}	$t_{boundary,max} = t_{window,max} / 51.6$
		$t_{boundary,typ} = t_{window,typ} / 64.5$
		$t_{boundary,min} = t_{window,min} / 92.7$

8.2 Typical Application

A typical application example (see 图 8-1) is used to describe the function of the watchdog in more detail.

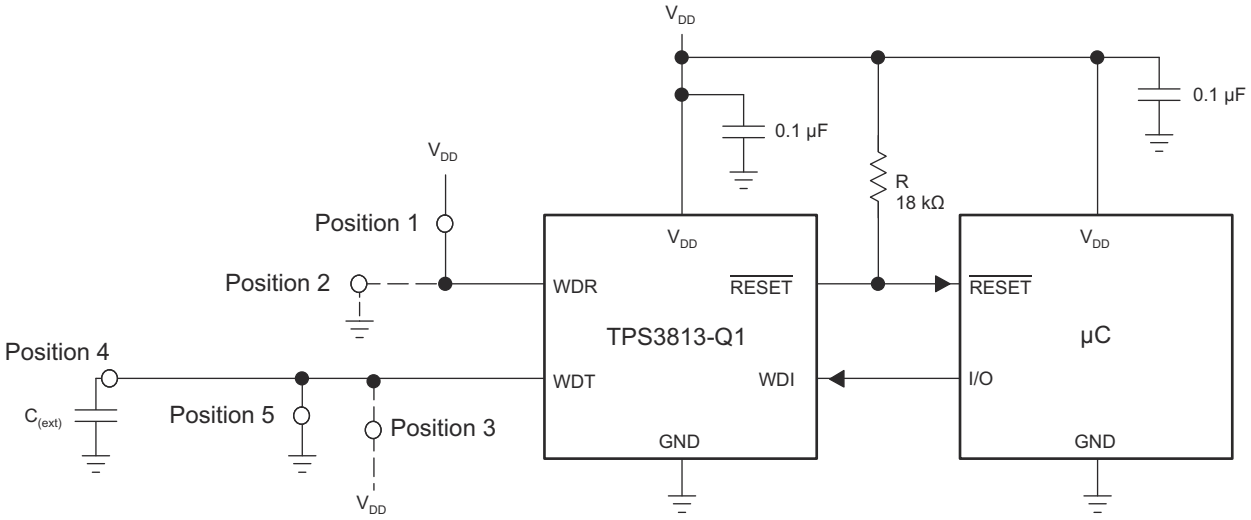


图 8-1. Application Example

8.2.1 Design Requirements

Design requirements include any design parameters that are solely based on the watchdog timing desired by the user. The 节 7.3.2 and 节 8.2.2 sections describe these timings. Select the TPS3813-Q1 device option based on desired threshold voltage of either 2.5 V, 3 V, 3.3 V, or 5 V.

8.2.2 Detailed Design Procedure

To configure the window watchdog function, two pins are provided by the TPS3813-Q1 family of devices. These pins set the window timeout and ratio.

The window watchdog ratio is a fixed ratio, which determines the lower boundary of the window frame. This ratio can be configured in two different frame sizes.

If the window watchdog ratio pin (WDR) is set to V_{DD} (Position 1 in 图 8-1) then the lower boundary frame is a value based on a ratio calculation of the overall window timeout size. For the watchdog timeout pin (WDT) connected to GND, the value is a ratio of 1:124.9, for WDT connected to V_{DD}, the value is a ratio of 1:127.7, and for an external capacitor connected to WDT, the value is a ratio of 1:64.5.

If the window watchdog ratio pin (WDR) is set to GND (Position 2) the lower boundary frame is a value based on a ratio calculation of the overall window timeout size. For the watchdog timeout pin (WDT) connected to GND, the value is a ratio of 1:31.8, for WDT connected to V_{DD} the value is a ratio 1:32, and for an external capacitor connected to WDT the value is a ratio of 1:25.8.

The watchdog timeout can be set in two fixed timings of 0.25 s and 2.5 s for the window or can by programmed by connecting a external capacitor with a low leakage current at WDT.

For example, if the watchdog timeout pin (WDT) is connected to V_{DD}, the timeout is 2.5 s. If the window watchdog ratio pin (WDR) is set in this configuration to a ratio of 1:127.7 by connecting the pin to V_{DD}, the lower boundary is 19.6 ms.

8.2.2.1 Programming Window-Watchdog Using an External Capacitor

The upper boundary of the watchdog timer can be set by an external capacitor connected between the WDT pin and GND. Common consumer electronic capacitors can be used to implement this feature. The capacitors that are used should have low ESR and low tolerances because the tolerances must be considered to perform the calculations. The first formula is used to calculate the upper window frame. After calculating the upper window frame, the lower boundary can be calculated. As in the last example, the most important values are the $t_{boundary,max}$ and $t_{window,min}$. The trigger pulse must fit into this window frame.

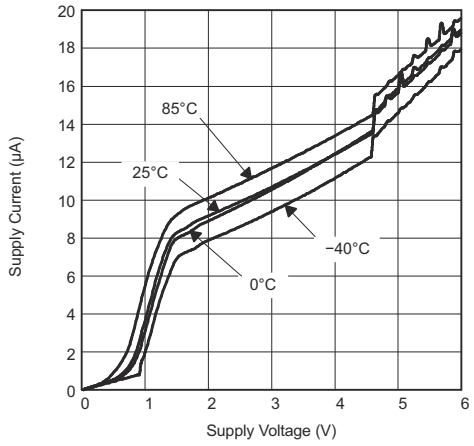
The external capacitor should have a value between a minimum of 155 pF and a maximum of 63 nF.

$$t_{window,typ} = \left(\frac{C_{(ext)}}{15.55\ pF} + 1 \right) \times 6.25\ ms \quad (2)$$

表 8-2. Watchdog Upper-Boundary Capacitor Programming

SELECTED OPERATION MODE		WINDOW FRAME
WDT = external capacitor $C_{(ext)}$	WDR = 0 V and WDR = V_{DD}	$t_{window,max} = 1.25 \times t_{window,typ}$
		$t_{window,min} = 0.75 \times t_{window,typ}$

8.2.3 Application Curve



WDI = GND WDT = GND WDR = GND

图 8-2. Supply Current vs Supply Voltage

9 Power Supply Recommendations

TPS3813-Q1 family of devices are designed to operate from an input supply with a voltage range from 2 V to 6 V. Although not required, placing a 0.1-µF ceramic capacitor close to the V_{DD} pin is good analog design practice.

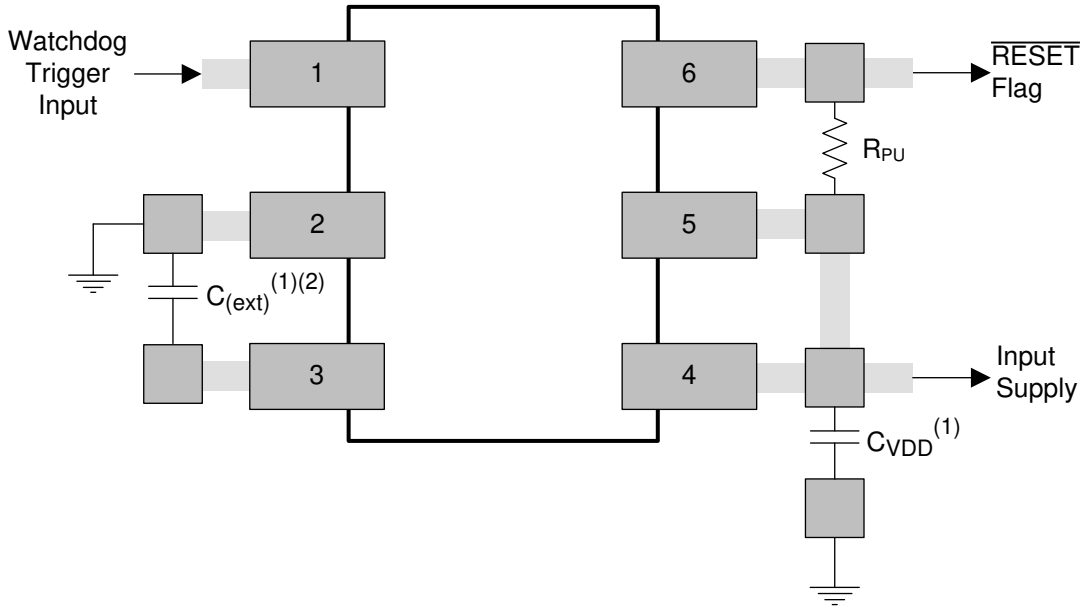
10 Layout

10.1 Layout Guidelines

Use the following guidelines for proper layout design of the device:

- Place the V_{DD} decoupling capacitor as close to the device as possible.
- Avoid using long traces for the V_{DD} supply node. The V_{DD} capacitor, along with the parasitic inductance from the supply to the capacitor, can cause ringing if the traces are excessive.
- If using a capacitor between the WDT pin and GND pin to program the upper boundary of the window-watchdog, the capacitor must be placed as close to the device as possible.
- Traces for WDR and WDT pins must be short and tight to avoid building up excessive parasitics.

10.2 Layout Example



A. In this layout example, the WDR pin is tied to V_{DD} and the WDT pin is tied to GND through an external capacitor.

B. The overall window timeout in this configuration is based on the external capacitor connected to the WDT pin. The formula used to calculate this value can be found in the 节 8.2.2 section.
In this configuration, the ratio of the frame lower boundary is 1:64.5 (typical) of the overall window timeout size. The maximum and minimum ratios are 1:51.6 and 1:92.7 of the overall window timeout size, respectively.

图 10-1. Device Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

图 11-1 shows a legend for reading the complete device name for and TPS3813-Q1 device.

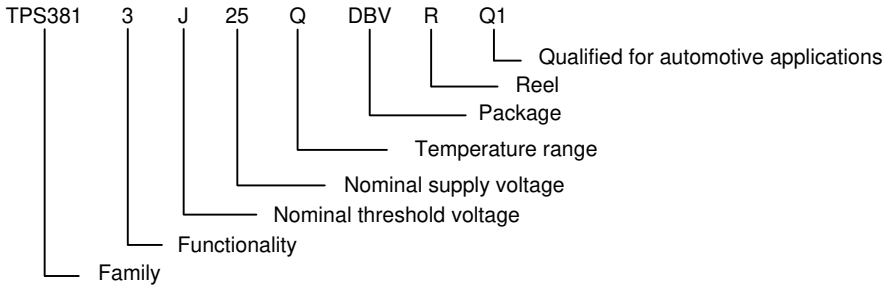


图 11-1. Device Nomenclature

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *All Window – Watchdog Supervisors* (SLVA365)
- *Choosing an Appropriate Pull-up/Pull-down Resistor for Open Drain Outputs* (SLVA485)
- *Disabling the Watchdog Timer for TI's Family of Supervisors* (SLVA145)
- *Window Watchdog Calculator for TPS3813 Voltage Supervisors* (SPRCAG1)

11.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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11.5 Trademarks

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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3813I50QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PFBI	Samples
TPS3813K33QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PFBQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS3813-Q1 :

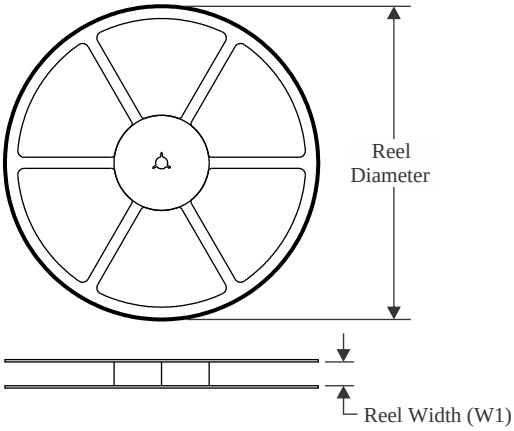
- Catalog : TPS3813

NOTE: Qualified Version Definitions:

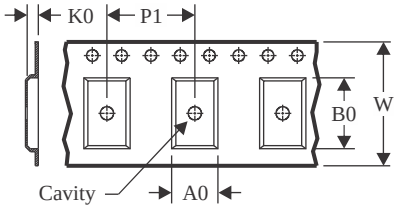
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

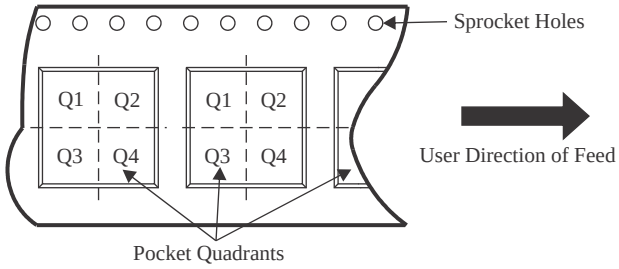


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

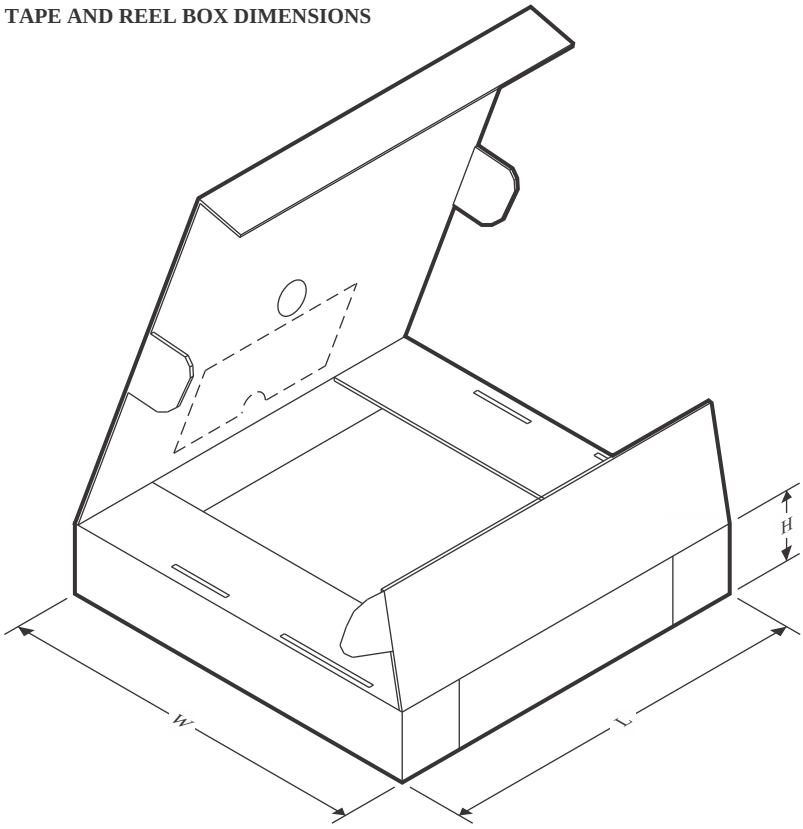
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3813I50QDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3813K33QDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

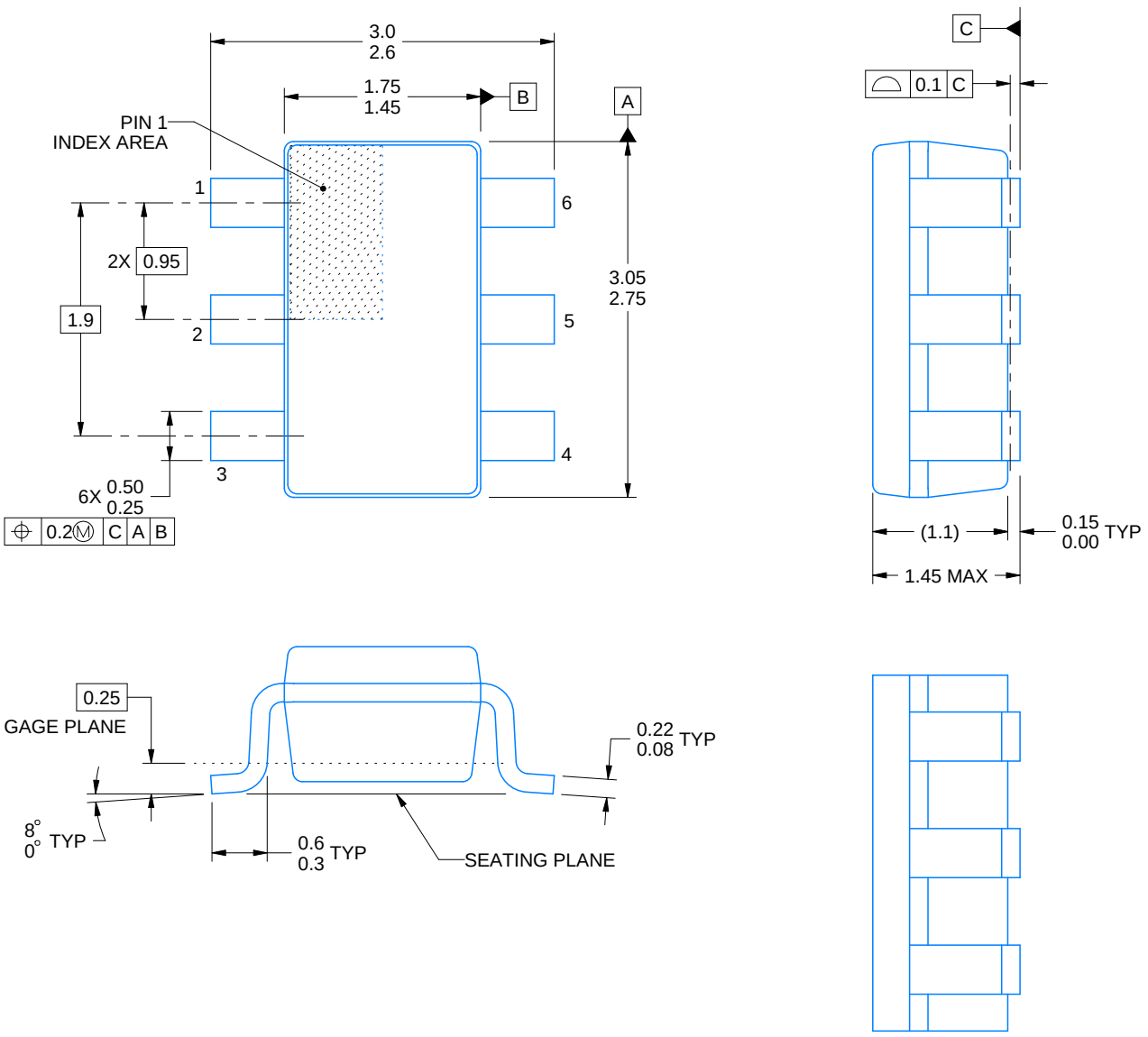
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3813I50QDBVRQ1	SOT-23	DBV	6	3000	210.0	185.0	35.0
TPS3813K33QDBVRQ1	SOT-23	DBV	6	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



ALTERNATIVE PACKAGE SINGULATION VIEW

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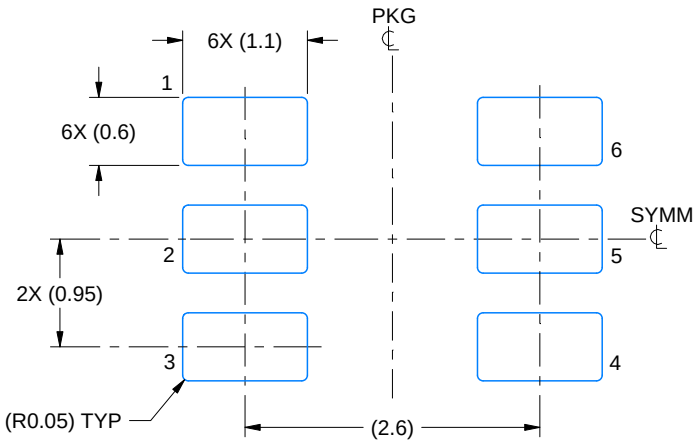
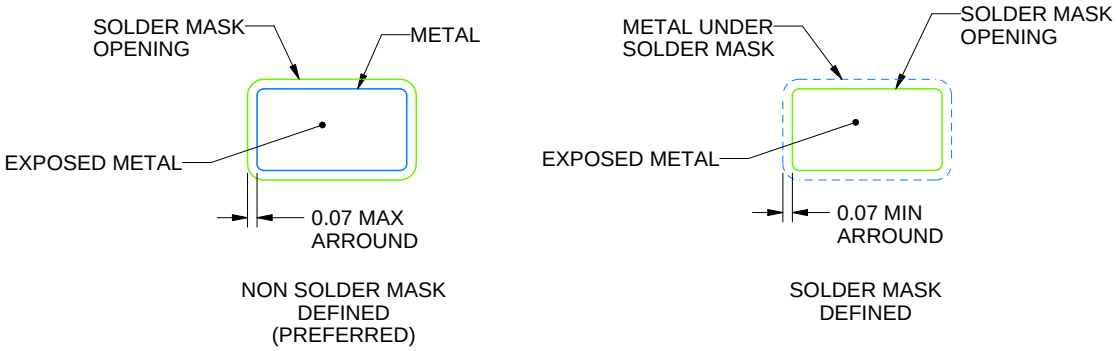
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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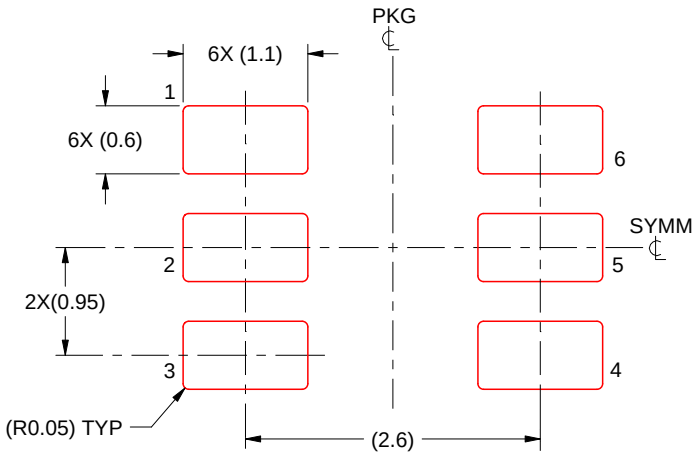
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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