TPS53353 具有 Eco-mode™ 的 20A 高效同步降压 SWIFT™ 转换器

1 特性

- 推出的新产品：TPS548B28 具有遥感功能的 16V、20A 同步降压转换器
- 转换输入电压范围：1.5V 至 15V
- VDD 输入电压范围：4.5V 至 25V
- 20A 时，在 12V 至 1.5V 之间效率达到 92%
- 输出电压范围：0.6V 至 5.5V
- 5V LDO 输出
- 支持单轨输入
- 具有 20A 连续输出电流的集成功率 MOSFET
- 用于在轻负载时实现高效率的自动跳跃 Eco-mode ™
- 关断电流 < 10μA
- 具有快速瞬态响应的 D-CAP™ 模式
- 可借助外部电阻器在 250kHz 至 1MHz 之间选择开关频率
- 可选自动跳跃或仅 PWM 工作模式
- 内置 1% 0.6V 基准电压
- 0.7ms、1.4ms、2.8ms 和 5.6ms 可选内部电压伺服器软启动
- 集成升压开关
- 预充电启动能力
- 具有热补偿的可调过流限制
- 过压、欠压、UVLO 和过热保护
- 支持全陶瓷输出电容器
- 漏极开路电源正常指示
- 整合 NexFET™ 电源块技术
- 采用 PowerPAD™ 的 22 引脚 QFN 封装
- 对于 SWIFT™ 电源产品文档，请参阅 http://www.ti.com/swift

2 应用

- 企业机架服务器和存储
- 有线网络交换机和路由器
- ASIC、SoC、FPGA、DSP 内核和 I/O 电压

3 说明

TPS53353 是一款具有集成 MOSFET 的 D-CAP™ 模式、20A 同步降压转换器。它们被设计用于易于使用、低外部组件数量和空间有限的电源系统。

这个器件特有 5.5mΩ/2.2mΩ 集成 MOSFET，精准 1% 0.6V 基准和集成的升压开关。具有竞争力的特性包括：1.5V 至 15V 的转换输入电压范围、极低外部元件数、针对超快速瞬态响应的 D-CAP™ 模式控制、自动跳跃模式操作、内部软启动控制、可选择频率以及无需补偿。

转换输入电压范围为 1.5V 至 15V，电源电压范围为 4.5V 至 25V，输出电压范围为 0.6V 至 5.5V。

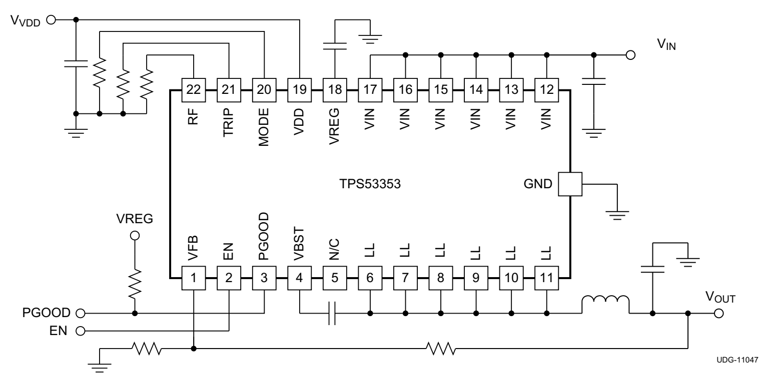
该器件采用 5mm × 6mm、22 引脚 QFN 封装，额定工作温度范围为 –40°C 至 85°C。

TPS548B28 是一款较新的 20A 器件、专为数据中心应用而设计、具有较小的无铅封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS53353	LSON-CLIP (22)	6.00mm × 5.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。



简化应用

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (December 2016) to Revision D (April 2021) **Page**

- 添加了*特性*：可选“绿色环保”（符合 RoHS 标准）.......... 1
- 向节 1 添加了 TPS548B28 信息，作为封装尺寸更小的较新 20A 器件.......... 1
- 更新了整个文档中的表格、图和交叉参考的编号格式.......... 1
- 在 节 3 中将 TPS548B28 信息添加为更新的 20A 器件 更小的封装.......... 1
- Changed the EN waveform and overall delay time on 图 7-1 and updated and moved the 图 7-1 note into the 节 7.3.1 description 14
- Added BST Resistor Selection to 节 8.2.2.2.1 24
- Added 方程式 19 and supporting information.......... 25
- MODE and RF pins updated in 图 10-1 31

Changes from Revision B (February 2015) to Revision C (February 2016) **Page**

- 将数据表标题从“TPS53353 具有 Eco-mode™ 的高效 20A 同步降压转换器”更改为“TPS53353 具有 Eco-mode™ 的 20A 高效同步降压 SWIFT™ 转换器” 1
- 添加了 *节 1*：“对于 SWIFT™ 电源产品文档...” 1

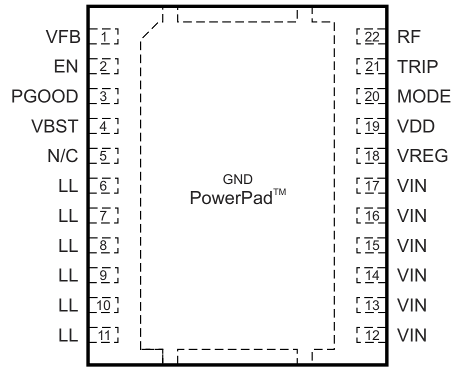
Changes from Revision A (April 2012) to Revision B (February 2015) **Page**

- 添加了*引脚配置和功能* 部分、*ESD 等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械*、*封装和可订购信息* 部分.......... 1

Changes from Revision Original (August 2011) to Revision A (April 2012) **Page**

- 将转换输入电压从“3V”更改为“1.5V” 1
- Changed VIN input voltage range minimum from "3 V" to "1.5 V".......... 3
- Changed to correct typographical error in THERMAL INFORMATION table.......... 4
- Changed VIN (main supply) input voltage range minimum from "3 V' to "1.5 V" in 节 6.3 4
- Changed conversion input voltage range from "3 V" to "1.5" in 节 7.1 13
- Added note to the 节 7.3 13
- Changed "ripple injection capacitor" to "ripple injection resistor" in the last bullet of the *Layout Guidelines* section.......... 30

5 Pin Configuration and Functions



A. N/C = no connection

图 5-1. 22-Pins LSON-CLIP DQP Package (Top View)

表 5-1. Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
EN	2	I	Enable pin.Typical turnon threshold voltage is 1.2 V. Typical turnoff threshold voltage is 0.95 V.
GND		G	Ground and thermal pad of the device. Use proper number of vias to connect to ground plane.
LL	6 7 8 9 10 11	B	Output of converted power. Connect this pin to the output Inductor.
MODE	20	I	Soft-start and Skip/CCM selection. Connect a resistor to select soft-start time using 表 7-3. The soft-start time is detected and stored into internal register during start-up.
N/C	5		No connect.
PGOOD	3	O	Open drain power good flag. Provides 1-ms start-up delay after VFB falls in specified limits. When VFB goes out of the specified limits PGOOD goes low after a 2-µs delay
RF	22	I	Switching frequency selection. Connect a resistor to GND or VREG to select switching frequency using 表 7-1. The switching frequency is detected and stored during the startup.
TRIP	21	I	OCL detection threshold setting pin. I_{TRIP} = 10 µA at room temperature, 4700 ppm/°C current is sourced and set the OCL trip voltage as follows. $V_{OCL}=V_{TRIP}/32$ ($V_{TRIP} \leqslant 1.2$ V, $V_{OCL} \leqslant 37.5$ mV)
VBST	4	P	Supply input for high-side FET gate driver (boost terminal). Connect capacitor from this pin to LL node. Internally connected to VREG via bootstrap MOSFET switch.
VDD	19	P	Controller power supply input. VDD input voltage range is from 4.5 V to 25 V.
VFB	1	I	Output feedback input. Connect this pin to Vout through a resistor divider.
VIN	12 13 14 15 16 17	P	Conversion power input.The conversion input voltage range is from 1.5 V to 15 V.
VREG	18	P	5-V low drop out (LDO) output. Supplies the internal analog circuitry and driver circuitry.

(1) I=Input, O=Output, B=Bidirectional, P=Supply, G=Ground

6 Specifications

6.1 Absolute Maximum Ratings[1]

			MIN	MAX	UNIT
Input voltage range	VIN (main supply)		–0.3	25	V
	VDD		–0.3	28	
	VBST		–0.3	32	
	VBST(with respect to LL)		–0.3	7	
	EN, TRIP, VFB, RF, MODE		–0.3	7	
Output voltage range	LL	DC	–2	25	V
		Pulse < 20ns, E=5 µJ	–7	27	
	PGOOD, VREG		–0.3	7	
	GND		–0.3	0.3	
Source/Sink current	VBST		50		mA
Operating free-air temperature, T_A			–40	85	°C
Junction temperature, T_J			–40	150	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds				300	
Storage temperature, T_{stg}			–55	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under 节 6.3 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage range	VIN (main supply)	1.5	15	V
	VDD	4.5	25	
	VBST	4.5	28	
	VBST(with respect to LL)	4.5	6.5	
	EN, TRIP, VFB, RF, MODE	–0.1	6.5	
Output voltage range	LL	–1	22	V
	PGOOD, VREG	–0.1	6.5	
Junction temperature range, T_J		–40	125	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		TPS53353 DQP (LSON-CLIP) 22 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	27.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	17.1	°C/W
θ_{JB}	Junction-to-board thermal resistance	5.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.8	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	1.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Over recommended free-air temperature range, V_{VDD}= 12 V (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{VIN}	VIN pin power conversion input voltage		1.5		15	V
V_{VDD}	Supply input voltage		4.5		25	V
$I_{VIN(leak)}$	VIN pin leakage current	V_{EN} = 0 V			1	µA
I_{VDD}	VDD supply current	T_A = 25°C, No load, V_{EN} = 5 V, V_{VFB} = 0.630 V		420	590	µA
I_{VDDSDN}	VDD shutdown current	T_A = 25°C, No load, V_{EN} = 0 V			10	µA
INTERNAL REFERENCE VOLTAGE						
V_{VFB}	VFB regulation voltage	CCM condition[(1)]		0.6		V
V_{VFB}	VFB regulation voltage	T_A = 25°C	0.597	0.6	0.603	V
		0°C ≤ T_A ≤ 85°C	0.5952	0.6	0.6048	
		–40°C ≤ T_A ≤ 85°C	0.594	0.6	0.606	
I_{VFB}	VFB input current	V_{VFB} = 0.630 V, T_A = 25°C		0.01	0.2	µA
LDO OUTPUT						
V_{VREG}	LDO output voltage	0 mA ≤ I_{VREG} ≤ 30 mA	4.77	5	5.36	V
I_{VREG}	LDO output current[(1)]	Maximum current allowed from LDO			30	mA
V_{DO}	Low drop out voltage	V_{VDD} = 4.5 V, I_{VREG} = 30 mA			230	mV
BOOT STRAP SWITCH						
V_{FBST}	Forward voltage	$V_{VREG-VBST}$, I_F = 10 mA, T_A = 25°C		0.1	0.2	V
I_{VBSTLK}	VBST leakage current	V_{VBST} = 23 V, V_{SW} = 17 V, T_A = 25°C		0.01	1.5	µA
DUTY AND FREQUENCY CONTROL						
$t_{OFF(min)}$	Minimum off time	T_A = 25°C	150	260	400	ns
$t_{ON(min)}$	Minimum on time	V_{IN} = 17 V, V_{OUT} = 0.6 V, R_{RF} = 39 kΩ, T_A = 25 °C[(1)]		35		ns
SOFT START						
t_{SS}	Internal soft-start time from V_{OUT} = 0 V to 95% of V_{OUT}	R_{MODE} = 39 kΩ		0.7		ms
		R_{MODE} = 100 kΩ		1.4		
		R_{MODE} = 200 kΩ		2.8		
		R_{MODE} = 470 kΩ		5.6		
INTERNAL MOSFETs						

Over recommended free-air temperature range, V_{VDD}= 12 V (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
$R_{DS(on)H}$	High-side MOSFET on-resistance	T_A = 25 °C		5.5		mΩ
$R_{DS(on)L}$	Low-side MOSFET on-resistance	T_A = 25 °C		2.2		mΩ
POWERGOOD						
V_{THPG}	PG threshold	PG in from lower	92.5%	95%	98.5%	
		PG in from higher	107.5%	110%	112.5%	
		PG hysteresis	2.5%	5%	7.5%	
R_{PG}	PG transistor on-resistance		15	30	55	Ω
t_{PGDEL}	PG delay	Delay for PG in	0.8	1	1.2	ms
LOGIC THRESHOLD AND SETTING CONDITIONS						
V_{EN}	EN Voltage	Enable	1.8			V
		Disable			0.6	V
I_{EN}	EN Input current	V_{EN} = 5 V			1	μA
f_{SW}	Switching frequency	R_{RF} = 0 Ω to GND, T_A = 25°C(2)	200	250	300	kHz
		R_{RF} = 187 kΩ to GND, T_A = 25°C(2)	250	300	350	kHz
		R_{RF} = 619 kΩ, to GND, T_A = 25°C(2)	350	400	450	kHz
		R_{RF} = Open, T_A= 25°C(2)	450	500	550	kHz
		R_{RF} = 866 kΩ to VREG, T_A = 25°C(2)	580	650	720	kHz
		R_{RF} = 309 kΩ to VREG, T_A = 25°C(2)	670	750	820	kHz
		R_{RF} = 124 kΩ to VREG, T_A = 25°C(2)	770	850	930	kHz
		R_{RF} = 0 Ω to VREG, T_A = 25°C(2)	880	970	1070	kHz
PROTECTION: CURRENT SENSE						
I_{TRIP}	TRIP source current	V_{TRIP} = 1 V, T_A = 25°C	9.4	10	10.6	μA
TC_{ITRIP}	TRIP current temperature coeffficient	On the basis of 25°C(1)		4700		ppm/°C
V_{TRIP}	Current limit threshold setting range	$V_{TRIP-GND}$	0.4		1.2	V
V_{OCL}	Current limit threshold	V_{TRIP} = 1.2 V	32	37.5	43	mV
		V_{TRIP} = 0.4	7.5	12.5	17.5	mV
V_{OCLN}	Negative current limit threshold	V_{TRIP} = 1.2 V	–160	–150	–140	mV
		V_{TRIP} = 0.4 V	–58	–50	–42	mV
V_{AZCADJ}	Auto zero cross adjustable range	Positive	3	15		mV
		Negative		–15	–3	mV
PROTECTION: UVP and OVP						
V_{OVP}	OVP trip threshold	OVP detect	115%	120%	125%	
t_{OVPDEL}	OVP proprogation delay	VFB delay with 50-mV overdrive		1		μs
V_{UVP}	Output UVP trip threshold	UVP detect	65%	70%	75%	
t_{UVPDEL}	Output UVP proprogation delay		0.8	1	1.2	ms
t_{UVPEN}	Output UVP enable delay	From enable to UVP workable	1.8	2.6	3.2	ms
UVLO						
V_{UVVREG}	VREG UVLO threshold	Wake up	4	4.2	4.33	V
		Hysteresis		0.25		V
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature(1)		145		°C
		Hysteresis(1)		10		°C

(1) Ensured by design. Not production tested.
(2) Not production tested. Test condition is V_{IN}= 12 V, V_{OUT}= 1.1 V, I_{OUT} = 10 A using application circuit shown in 图 8-1.

6.6 Typical Characteristics

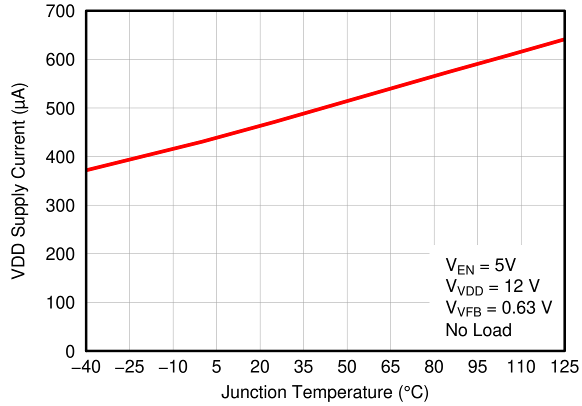


图 6-1. VDD Supply Current vs. Junction Temperature

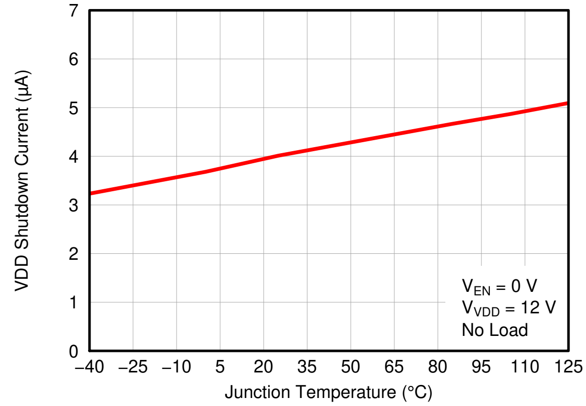


图 6-2. VDD Shutdown Current vs. Junction Temperature

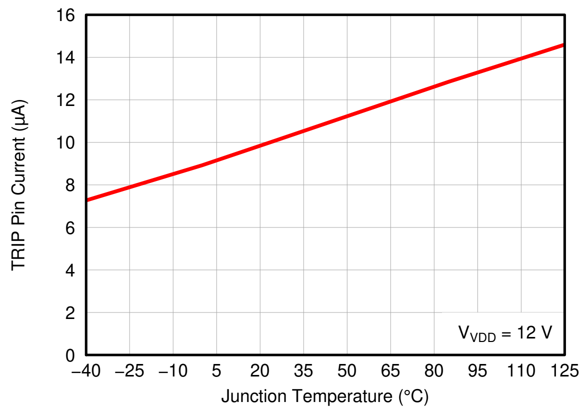


图 6-3. TRIP Pin Current vs. Junction Temperature

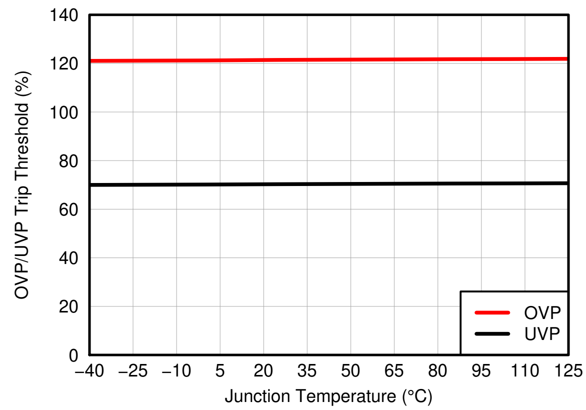


图 6-4. OVP/UVP Trip Threshold vs. Junction Temperature

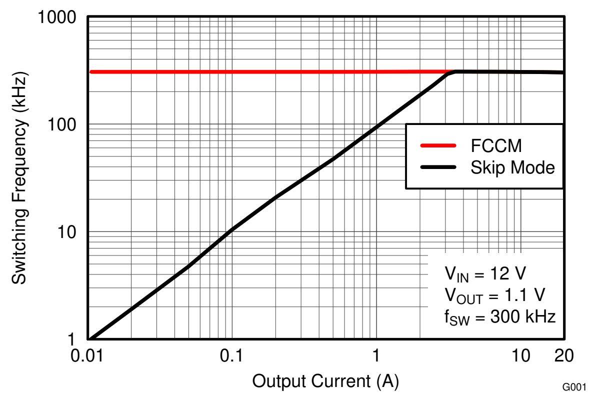


图 6-5. Switching Frequency vs. Output Current

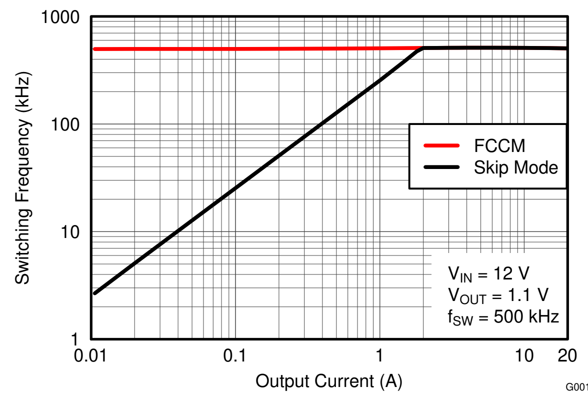


图 6-6. Switching Frequency vs. Output Current

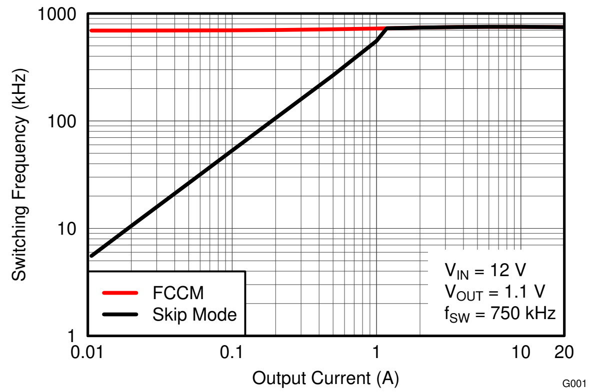


图 6-7. Switching Frequency vs. Output Current

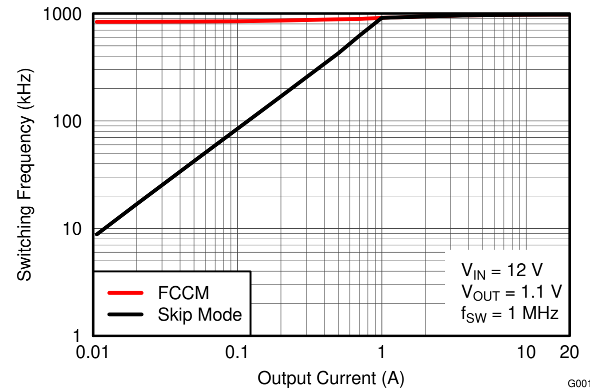


图 6-8. Switching Frequency vs. Output Current

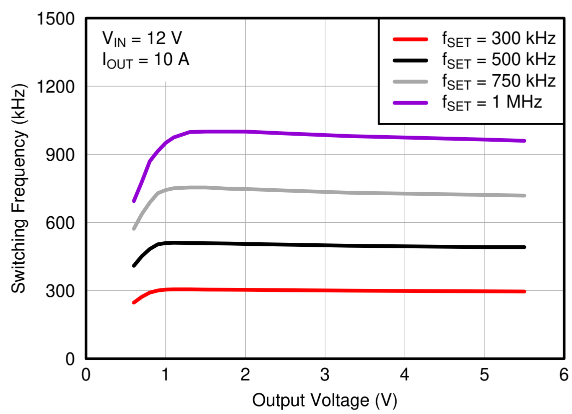


图 6-9. Switching Frequency vs. Output Voltage

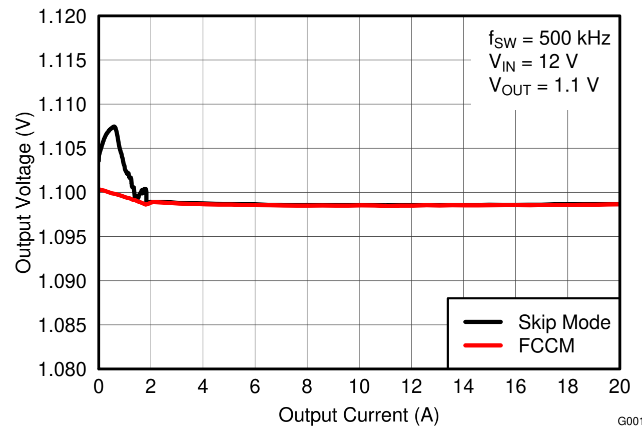


图 6-10. Output Voltage vs. Output Current

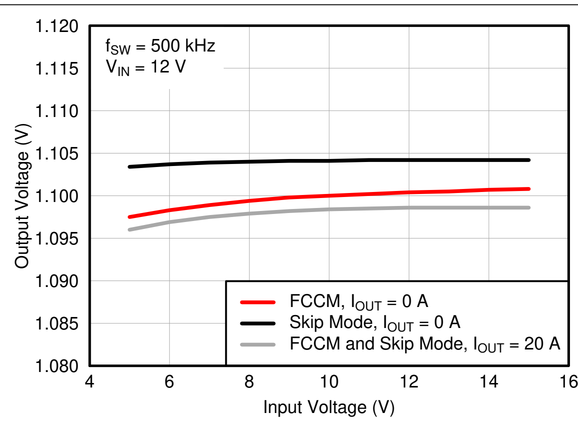


图 6-11. Output Voltage vs. Input Voltage

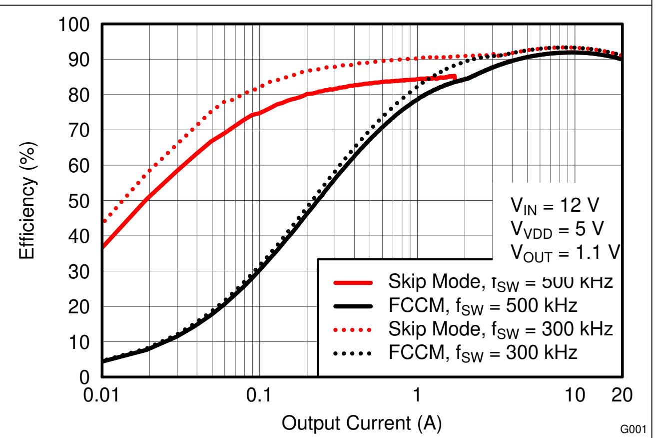


图 6-12. Efficiency vs Output Current

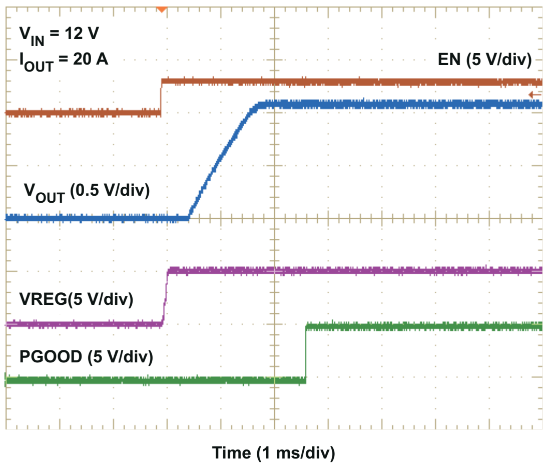


图 6-13. Start-Up Waveforms

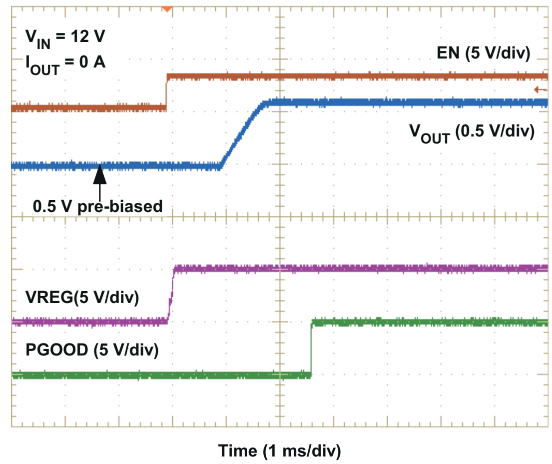


图 6-14. Prebias Start-Up Waveforms

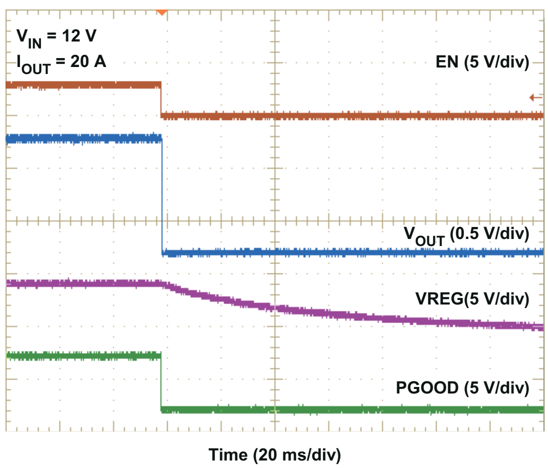


图 6-15. Shutdown Waveforms

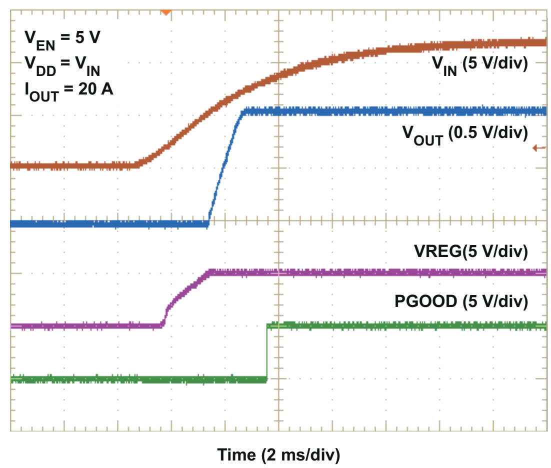


图 6-16. UVLO Start-Up Waveforms

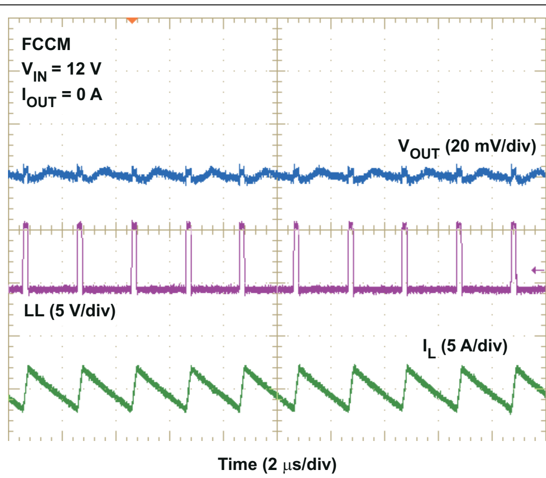


图 6-17. 1.1-V Output FCCM Mode Steady-State Operation

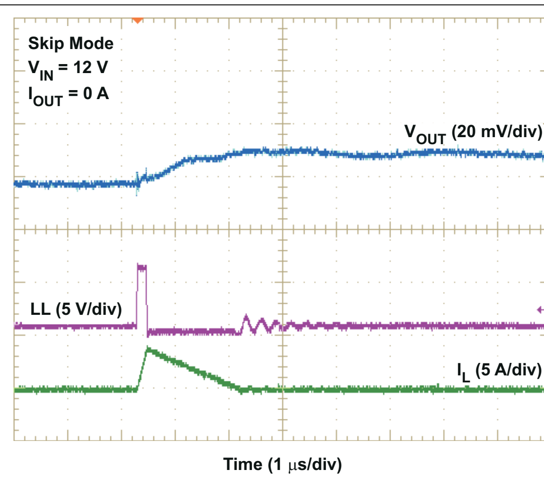


图 6-18. 1.1-V Output Skip Mode Steady-State Operation

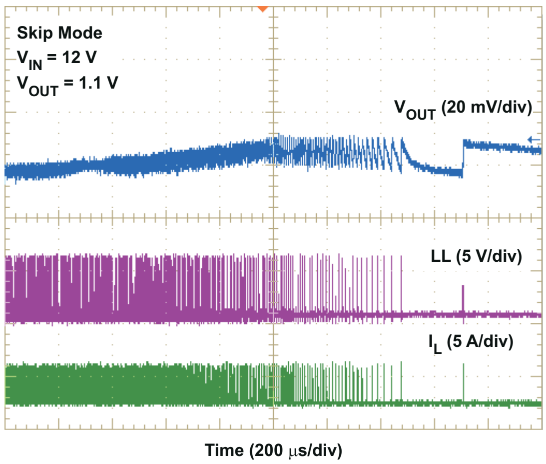


图 6-19. CCM-to-DCM Transition Waveforms

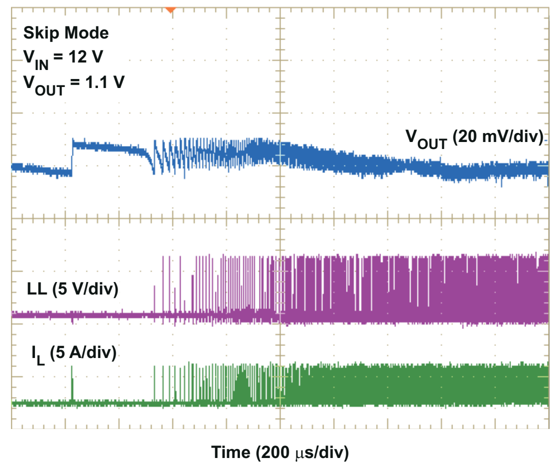


图 6-20. DCM-to-CCM Transition Waveforms

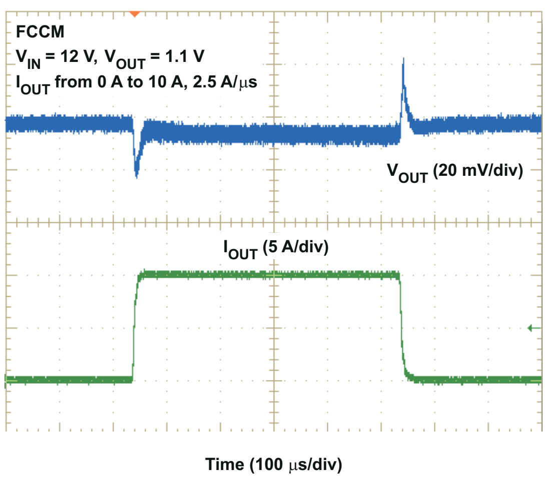


图 6-21. FCCM Load Transient

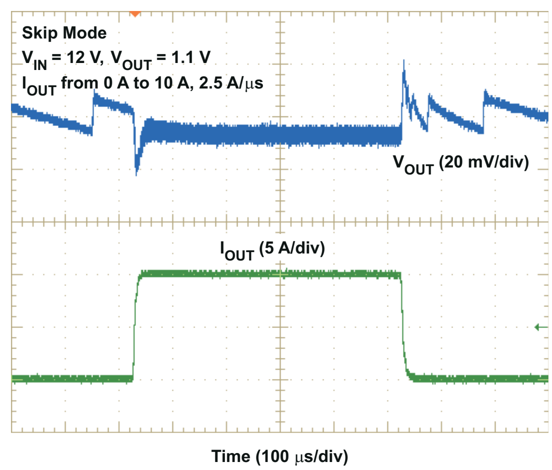


图 6-22. Skip Mode Load Transeint

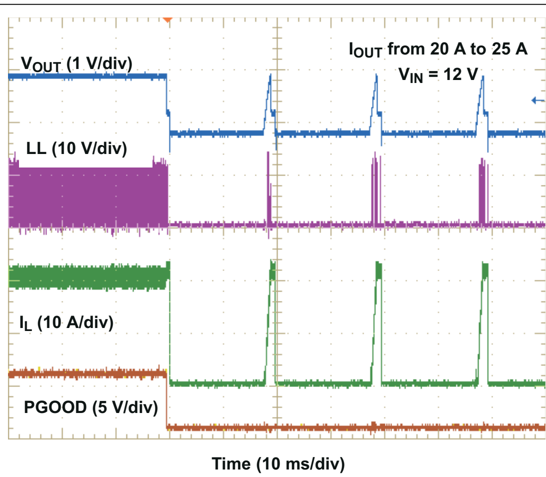


图 6-23. Overcurrent Protection Waveforms

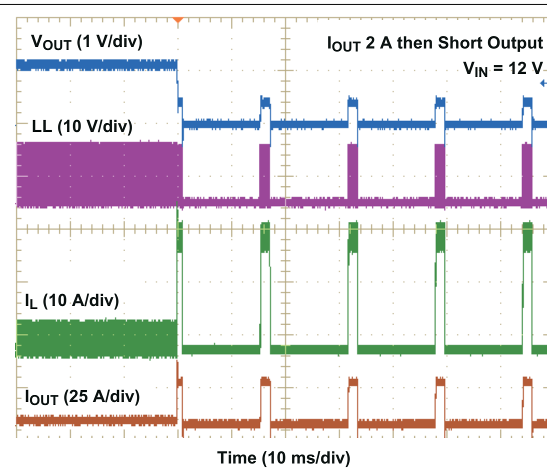


图 6-24. Output Short-Circuit Protection Waveforms

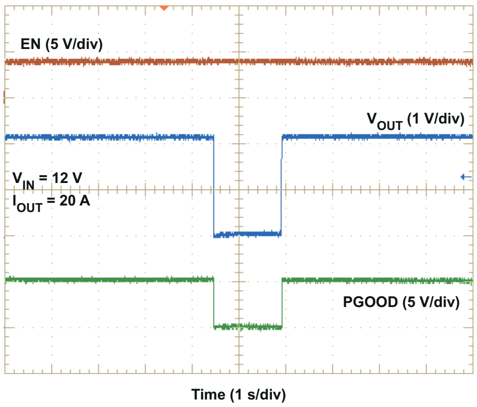


图 6-25. Overtemperature Protection Waveforms

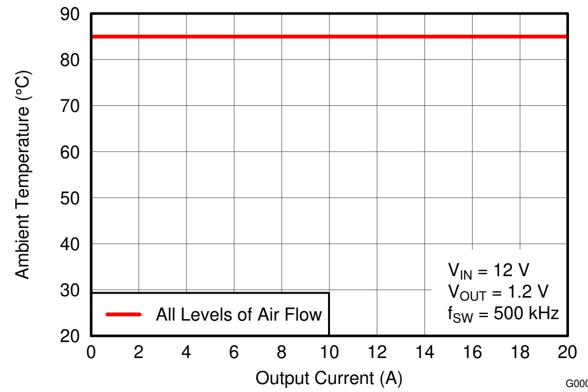


图 6-26. Safe Operating Area

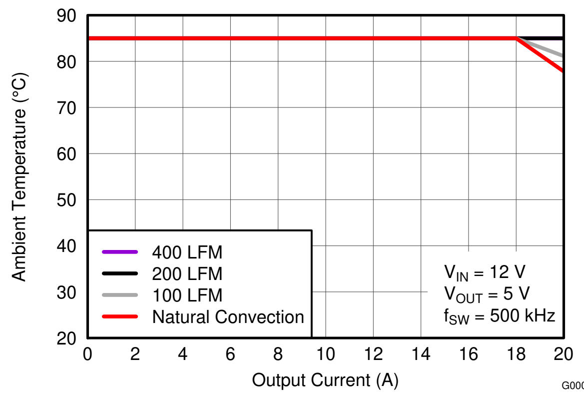


图 6-27. Safe Operating Area

For V_{OUT} = 5 V, an SC5026-1R0 inductor is used. For 1 ≤ V_{OUT} ≤ 3.3 V, a PA0513.441 inductor is used

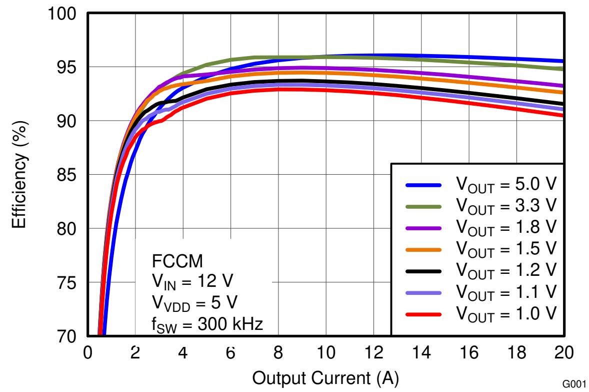


图 6-28. Efficiency vs Output Current

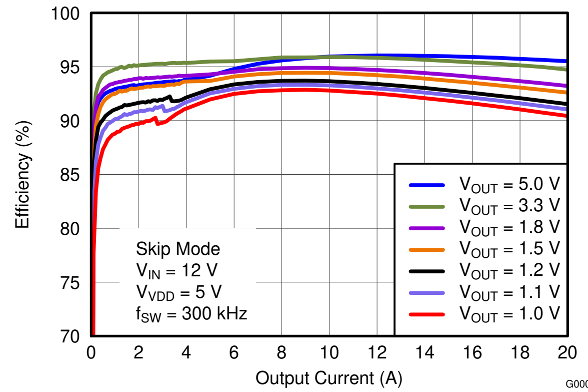


图 6-29. Efficiency vs Output Current

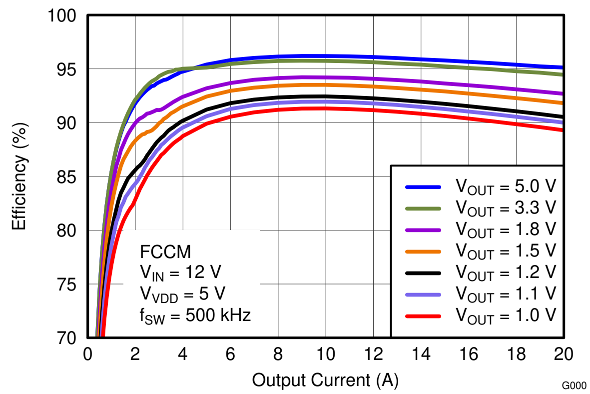


图 6-30. Efficiency vs Output Current

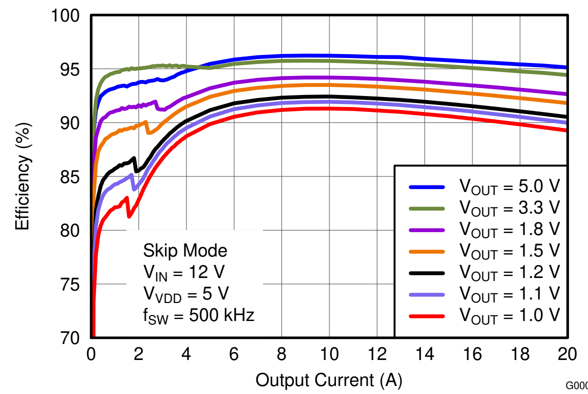


图 6-31. Efficiency vs Output Current

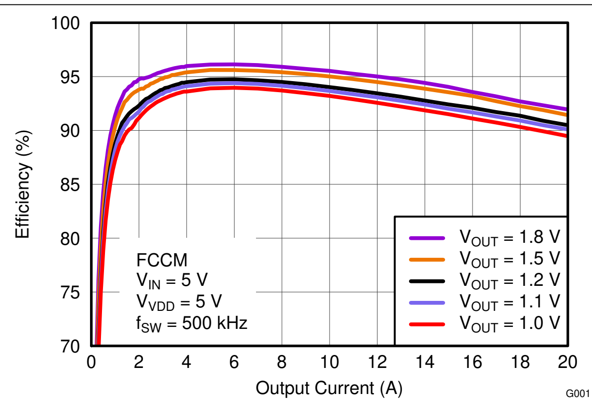


图 6-32. Efficiency vs Output Current

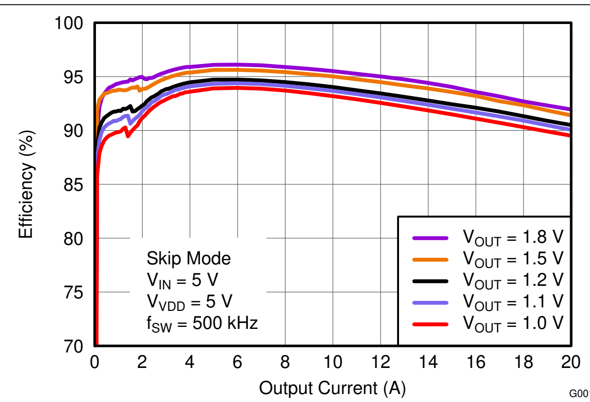


图 6-33. Efficiency vs Output Current

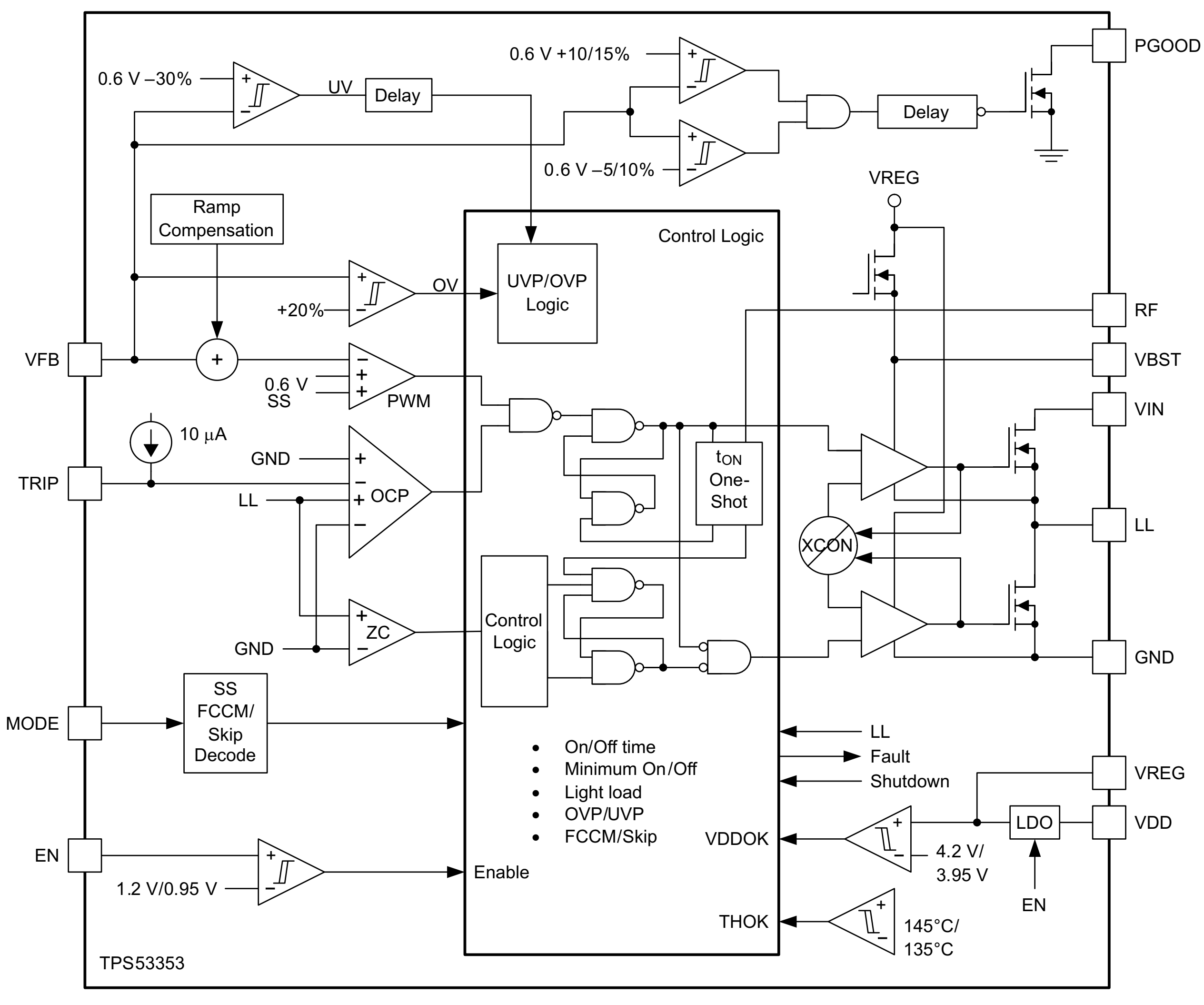
7 Detailed Description

7.1 Overview

The TPS53353 is a high-efficiency, single channel, synchronous buck converter suitable for low output voltage point-of-load applications in computing and similar digital consumer applications. The device features proprietary D-CAP™ mode control combined with an adaptive on-time architecture. This combination is ideal for building modern low duty ratio, ultra-fast load step response DC-DC converters. The output voltage ranges from 0.6 V to 5.5 V. The conversion input voltage range is from 1.5 V up to 15 V and the VDD bias voltage is from 4.5 V to 25 V. The D-CAP™ mode uses the equivalent series resistance (ESR) of the output capacitor(s) to sense the device current . One advantage of this control scheme is that it does not require an external phase compensation network. This allows a simple design with a low external component count. Eight preset switching frequency values can be chosen using a resistor connected from the RF pin to ground or VREG. Adaptive on-time control tracks the preset switching frequency over a wide input and output voltage range while allowing the switching frequency to increase at the step-up of the load.

The TPS53353 has a MODE pin to select between auto-skip mode and forced continuous conduction mode (FCCM) for light load conditions. The MODE pin also sets the selectable soft-start time ranging from 0.7 ms to 5.6 ms as shown in 表 7-3.

7.2 Functional Block Diagram



Note

The thresholds in this block diagram are typical values. Refer to the 节 6.5 table for threshold limits.

7.3 Feature Description

7.3.1 5-V LDO and VREG Start-Up

TPS53353 provides an internal 5V LDO function using input from VDD and output to VREG. The 5V LDO is gated by the EN pin. The LDO starts-up when EN is approximately 1.8V and VDD is approximately 2V. (See 图 7-1) The LDO outputs its voltage to the VREG pin. The VREG voltage provides the bias voltage for the internal analog circuitry and also provides the supply voltage for the gate drives.

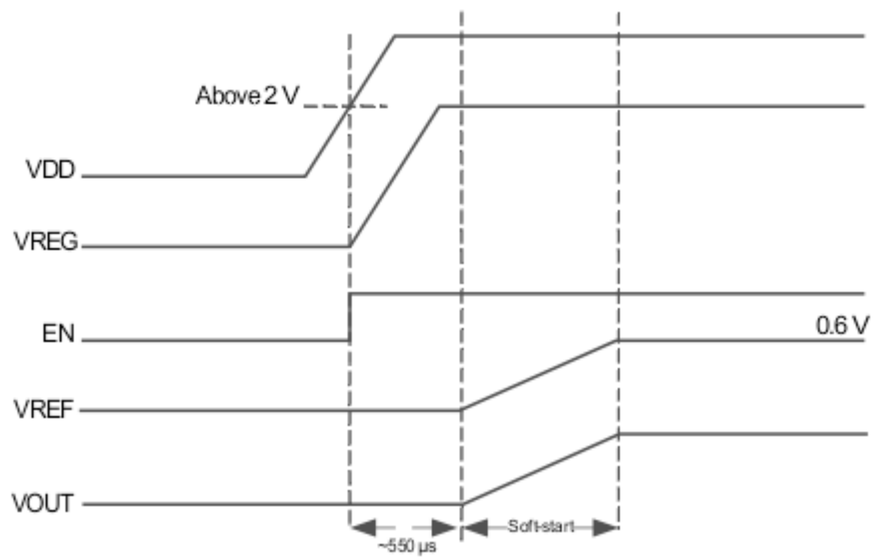


图 7-1. Power Up Sequence

7.3.2 Adaptive On-Time D-CAP™ Control and Frequency Selection

The TPS53353 does not have a dedicated oscillator to determine switching frequency. However, the device operates with pseudo-constant frequency by feed-forwarding the input and output voltages into the on-time one-shot timer. The adaptive on-time control adjusts the on-time to be inversely proportional to the input voltage and proportional to the output voltage ($t_{ON} \propto V_{OUT}/V_{IN}$).

This makes the switching frequency fairly constant in steady state conditions over a wide input voltage range. The switching frequency is selectable from eight preset values by a resistor connected between the RF pin and GND or between the RF pin and the VREG pin as shown in 表 7-1. (Maintaining open resistance sets the switching frequency to 500 kHz.)

表 7-1. Resistor and Switching Frequency

RESISTOR (R_{RF}) CONNECTIONS		SWITCHING FREQUENCY (f_{SW}) (kHz)
VALUE (kΩ)	CONNECT TO	
0	GND	250
187	GND	300
619	GND	400

表 7-1. Resistor and Switching Frequency (continued)

RESISTOR (R_{RF}) CONNECTIONS		SWITCHING FREQUENCY (f_{SW}) (kHz)
VALUE (kΩ)	CONNECT TO	
OPEN	n/a	500
866	VREG	650
309	VREG	750
124	VREG	850
0	VREG	970

The off-time is modulated by a PWM comparator. The VFB node voltage (the mid-point of resistor divider) is compared to the internal 0.6-V reference voltage added with a ramp signal. When both signals match, the PWM comparator asserts a set signal to terminate the off time (turn off the low-side MOSFET and turn on high-side MOSFET). The set signal is valid if the inductor current level is below the OCP threshold, otherwise the off time is extended until the current level falls below the threshold.

图 7-2 and 图 7-3 show two on-time control schemes.

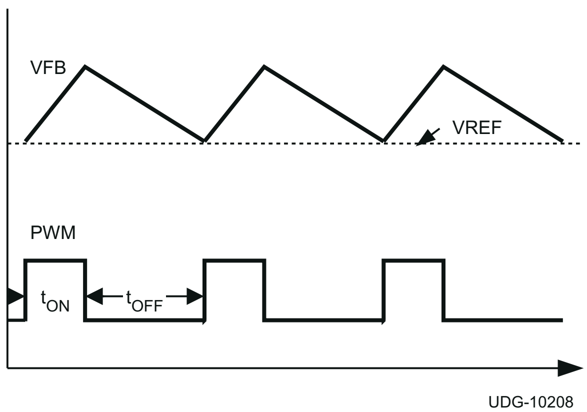


图 7-2. On-Time Control Without Ramp Compensation

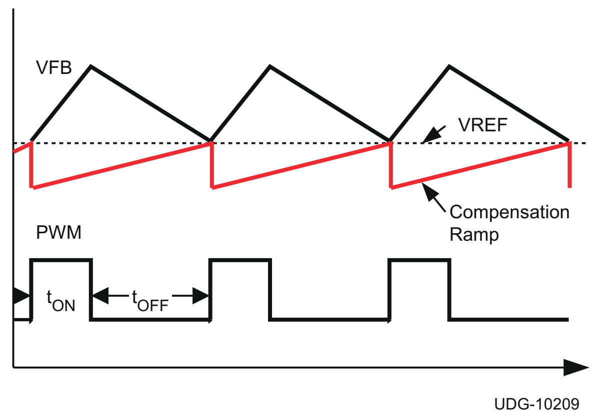


图 7-3. On-Time Control With Ramp Compensation

7.3.3 Ramp Signal

The TPS53353 adds a ramp signal to the 0.6-V reference in order to improve jitter performance. As described in the previous section, the feedback voltage is compared with the reference information to keep the output voltage in regulation. By adding a small ramp signal to the reference, the signal-to-noise ratio at the onset of a new switching cycle is improved. Therefore the operation becomes less jittery and more stable. The ramp signal is controlled to start with –7 mV at the beginning of an on-cycle and becomes 0 mV at the end of an off-cycle in steady state.

During skip mode operation, under discontinuous conduction mode (DCM), the switching frequency is lower than the nominal frequency and the off-time is longer than the off-time in CCM. Because of the longer off-time, the ramp signal extends after crossing 0 mV. However, it is clamped at 3 mV to minimize the DC offset.

7.3.4 Adaptive Zero Crossing

The TPS53353 has an adaptive zero crossing circuit which performs optimization of the zero inductor current detection at skip mode operation. This function pursues ideal low-side MOSFET turning off timing and compensates inherent offset voltage of the Z-C comparator and delay time of the Z-C detection circuit. It prevents SW-node swing-up caused by too late detection and minimizes diode conduction period caused by too early detection. As a result, better light load efficiency is delivered.

7.3.5 Power-Good

The TPS53353 has power-good output that indicates high when switcher output is within the target. The power-good function is activated after soft-start has finished. If the output voltage becomes within +10% and –5% of the target value, internal comparators detect power-good state and the power-good signal becomes high after a 1-ms internal delay. If the output voltage goes outside of +15% or –10% of the target value, the power-good signal becomes low after two microsecond (2-μs) internal delay. The power-good output is an open drain output and must be pulled up externally.

The power-good MOSFET is powered through the VDD pin. V_{VDD} must be >1 V in order to have a valid power-good logic. It is recommended to pull PGOOD up to VREG (or a voltage divided from VREG) so that the power-good logic is still valid even without VDD supply.

7.3.6 Current Sense, Overcurrent and Short Circuit Protection

TPS53353 has cycle-by-cycle overcurrent limiting control. The inductor current is monitored during the *OFF* state and the controller maintains the *OFF* state during the period in that the inductor current is larger than the overcurrent trip level. In order to provide both good accuracy and cost effective solution, TPS53353 supports temperature compensated MOSFET $R_{DS(on)}$ sensing. The TRIP pin should be connected to GND through the trip voltage setting resistor, R_{TRIP}. The TRIP terminal sources current (I_{TRIP}) which is 10 μA typically at room temperature, and the trip level is set to the OCL trip voltage V_{TRIP} as shown in 方程式 1.

$$V_{TRIP}\left(mV\right) = R_{TRIP}\left(k\Omega\right) \times I_{TRIP}\left(\mu A\right) \quad (1)$$

The inductor current is monitored by the LL pin. The GND pin is used as the positive current sensing node and the LL pin is used as the negative current sense node. The trip current, I_{TRIP} has 4700ppm/°C temperature slope to compensate the temperature dependency of the $R_{DS(on)}$.

As the comparison is made during the *OFF* state, V_{TRIP} sets the valley level of the inductor current. Thus, the load current at the overcurrent threshold, I_{OCP}, can be calculated as shown in 方程式 2.

$$I_{OCP} = \frac{V_{TRIP}}{\left(32 \times R_{DS(on)}\right)} + \frac{I_{IND(ripple)}}{2} = \frac{V_{TRIP}}{\left(32 \times R_{DS(on)}\right)} + \frac{1}{2 \times L \times f_{SW}} \times \frac{\left(V_{IN} - V_{OUT}\right) \times V_{OUT}}{V_{IN}} \quad (2)$$

In an overcurrent or short circuit condition, the current to the load exceeds the current to the output capacitor thus the output voltage tends to decrease. Eventually, it crosses the undervoltage protection threshold and shuts down. After a hiccup delay (16 ms with 0.7 ms sort-start), the controller restarts. If the overcurrent condition remains, the procedure is repeated and the device enters hiccup mode.

Hiccup time calculation:

$$t_{HIC(wait)} = (2^n + 257) \times 4\ \mu s \quad (3)$$

where

- N = 8, 9, 10, or 11 depending on soft start time selection

$$t_{HIC(dly)} = 7 \times (2^n + 257) \times 4\ \mu s \quad (4)$$

表 7-2. Hiccup Time Calculation

SELECTED SOFT-START TIME (t_{SS}) (ms)	n	HICCUP WAIT TIME ($t_{HIC(wait)}$) (ms)	HICCUP DELAY TIME ($t_{HIC(dly)}$) (ms)
0.7	8	2.052	14.364
1.4	9	3.076	21.532
2.8	10	5.124	35.868
5.6	11	9.22	64.54

7.3.7 Overvoltage and Undervoltage Protection

TPS53353 monitors a resistor divided feedback voltage to detect over and under voltage. When the feedback voltage becomes lower than 70% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 1ms, TPS53353 latches OFF both high-side and low-side MOSFETs drivers. The controller restarts after a hiccup delay (16 ms with 0.7 ms soft-start). This function is enabled 1.5-ms after the soft-start is completed.

When the feedback voltage becomes higher than 120% of the target voltage, the OVP comparator output goes high and the circuit latches OFF the high-side MOSFET driver and latches ON the low-side MOSFET driver. The output voltage decreases. If the output voltage reaches UV threshold, then both high-side MOSFET and low-side MOSFET driver will be OFF and the device restarts after a hiccup delay. If the OV condition remains, both high-side MOSFET and low-side MOSFET driver remains OFF until the OV condition is removed.

7.3.8 UVLO Protection

The TPS53353 uses VREG undervoltage lockout protection (UVLO). When the VREG voltage is lower than 3.95 V, the device shuts off. When the VREG voltage is higher than 4.2V, the device restarts. This is a non-latch protection.

7.3.9 Thermal Shutdown

TPS53353 monitors the temperature of itself. If the temperature exceeds the threshold value (typically 145°C), TPS53353 is shut off. When the temperature falls about 10°C below the threshold value, the device will turn back on. This is a non-latch protection.

7.4 Device Functional Modes

7.4.1 Small Signal Model

From small-signal loop analysis, a buck converter using D-CAP™ mode can be simplified as shown in 图 7-4.

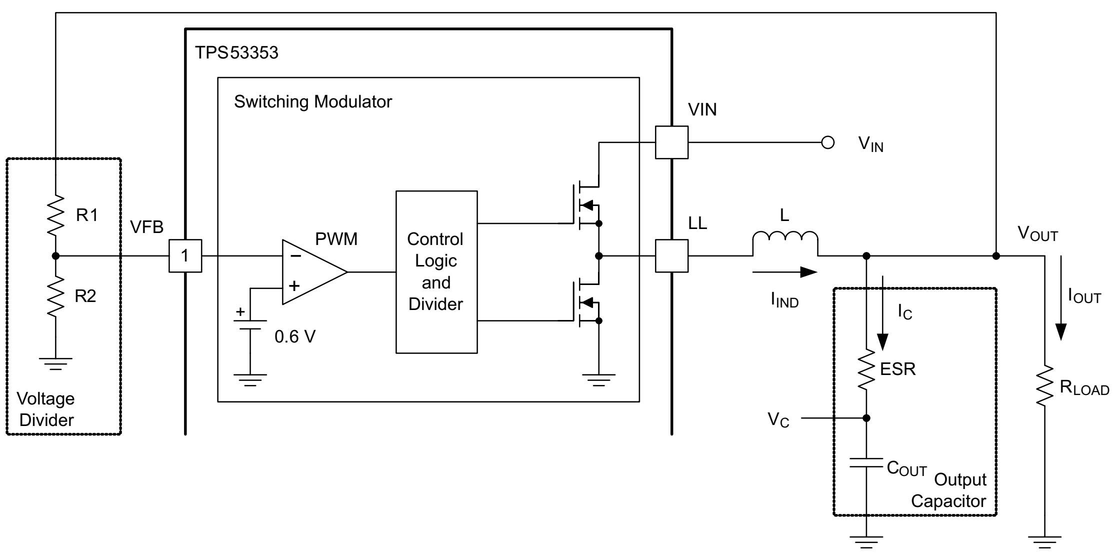


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图 7-4. Simplified Modulator Model

The output voltage is compared with the internal reference voltage (ramp signal is ignored here for simplicity). The PWM comparator determines the timing to turn on the high-side MOSFET. The gain and speed of the comparator can be assumed high enough to keep the voltage at the beginning of each on cycle substantially constant.

$$H(s) = \frac{1}{s \times ESR \times C_{OUT}} \quad (5)$$

For loop stability, the 0-dB frequency, f_0, defined in 方程式 6 needs to be lower than 1/4 of the switching frequency.

$$f_0 = \frac{1}{2\pi \times ESR \times C_{OUT}} \le \frac{f_{SW}}{4} \quad (6)$$

According to 方程式 6, the loop stability of D-CAP™ mode modulator is mainly determined by the capacitor's chemistry. For example, specialty polymer capacitors (SP-CAP) have an output capacitance in the order of several 100 µF and ESR in range of 10 mΩ. These makes f_0 on the order of 100 kHz or less, creating a stable loop. However, ceramic capacitors have an f_0 at more than 700 kHz, and need special care when used with this modulator. An application circuit for ceramic capacitor is described in 节 8.2.2.2.2.

7.4.2 Enable, Soft Start, and Mode Selection

When the EN pin voltage rises above the enable threshold voltage (typically 1.2 V), the controller enters its start-up sequence. The internal LDO regulator starts immediately and regulates to 5 V at the VREG pin. The controller then uses the first 250 µs to calibrate the switching frequency setting resistance attached to the RF pin and stores the switching frequency code in internal registers. During this period, the MODE pin also senses the resistance attached to this pin and determines the soft-start time. Switching is inhibited during this phase. In the second phase, an internal DAC starts ramping up the reference voltage from 0 V to 0.6 V. Depending on the MODE pin setting, the ramping up time varies from 0.7 ms to 5.6 ms. Smooth and constant ramp-up of the output voltage is maintained during start-up regardless of load current.

表 7-3. Soft-Start and MODE Settings

MODE SELECTION	ACTION	SOFT-START TIME (ms)	R_{MODE} (kΩ)
Auto-skip	Pulldown to GND	0.7	39
		1.4	100
		2.8	200
		5.6	475
Forced CCM(1)	Connect to PGOOD	0.7	39
		1.4	100
		2.8	200
		5.6	475

(1) Device enters FCCM after the PGOOD pin goes high when MODE is connected to PGOOD through the resistor R_{MODE}.

After soft-start begins, the MODE pin becomes the input of an internal comparator which determines auto-skip or FCCM mode operation. If MODE voltage is higher than 1.3 V, the converter enters into FCCM mode. Otherwise it will be in auto-skip mode at light load condition. Typically, when FCCM mode is selected, the MODE pin is connected to PGOOD through the R_{MODE} resistor, so that before PGOOD goes high the converter remains in auto-skip mode.

7.4.3 Auto-Skip Eco-mode™ Light Load Operation

While the MODE pin is pulled low via R_{MODE}, TPS53353 automatically reduces the switching frequency at light load conditions to maintain high efficiency. Detailed operation is described as follows. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to the point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The synchronous MOSFET is turned off when this zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode (DCM). The on-time is kept almost the same as it was in the continuous conduction mode so that it takes longer to discharge the output capacitor with smaller load current to the level of the reference voltage. The transition point to the light-load operation $I_{OUT(LL)}$ (that is, the threshold between continuous and discontinuous conduction mode) can be calculated as shown in 方程式 7.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (7)$$

where

- f_{SW} is the PWM switching frequency

Switching frequency versus output current in the light load condition is a function of L, V_{IN}, and V_{OUT}, but it decreases almost proportionally to the output current from the $I_{OUT(LL)}$ given in 方程式 7. For example, it is 60 kHz at $I_{OUT(LL)}/5$ if the frequency setting is 300 kHz.

7.4.4 Forced Continuous Conduction Mode

When the MODE pin is tied to PGOOD through a resistor, the controller keeps continuous conduction mode (CCM) in light load condition. In this mode, switching frequency is kept almost constant over the entire load range which is suitable for applications need tight control of the switching frequency at a cost of lower efficiency.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI' s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS53353 is a high-efficiency, single channel, synchronous buck converter suitable for low output voltage point-of-load applications in computing and similar digital consumer applications. The device features proprietary D-CAP mode control combined with an adaptive on-time architecture. This combination is ideal for building modern low duty ratio, ultra-fast load step response DC-DC converters. The output voltage ranges from 0.6 V to 5.5 V. The conversion input voltage range is from 1.5 V up to 15 V and the VDD bias voltage is from 4.5 V to 25 V. The D-CAP mode uses the equivalent series resistance (ESR) of the output capacitor(s) to sense the device current. One advantage of this control scheme is that it does not require an external phase compensation network. This allows a simple design with a low external component count. Eight preset switching frequency values can be chosen using a resistor connected from the RF pin to ground or VREG. Adaptive on-time control tracks the preset switching frequency over a wide input and output voltage range while allowing the switching frequency to increase at the step-up of the load.

8.2 Typical Applications

8.2.1 Typical Application Circuit Diagram

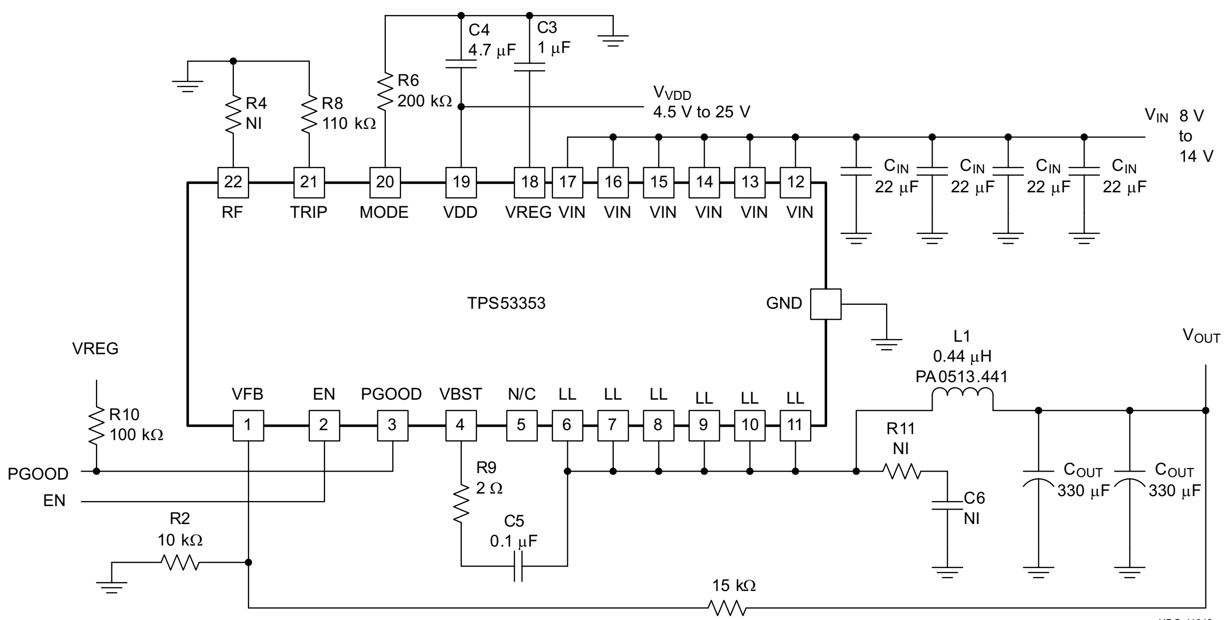

图 8-1. Typical Application Circuit Diagram

8.2.1.1 Design Requirements

表 8-1. Design Parameters

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	Voltage range		8	12	14	V
I_{MAX}	Maximum Input current	V_{IN} = 8 V, I_{OUT} = 20 A		4.1		A
	No load input current	V_{IN} = 14 V, I_{OUT} = 0 A with auto-skip mode		1		mA
OUTPUT CHARACTERISTICS						
V_{OUT}	Output voltage			1.5		V
	Output voltage regulation	Line regulation, 8 V ≤ V_{IN} ≤ 15 V		0.1%		
		Load regulation, V_{IN} = 12 V, 0 A ≤ I_{OUT} ≤ 20 A with FCCM		0.2%		
V_{RIPPLE}	Output voltage ripple	V_{IN} = 12 V, I_{OUT} = 20 A with FCCM		20		mV_{PP}
I_{LOAD}	Output load current		0		20	A
I_{OCP}	Output overcurrent threshold			26		A
t_{SS}	Soft-start time			1.4		ms
SYSTEMS CHARACTERISTICS						
f_{SW}	Switching frequency			500		kHz
η	Peak efficiency	V_{IN} = 12 V, V_{OUT} = 1.1 V, I_{OUT} = 10 A		91.87%		
	Full load efficiency	V_{IN} = 12 V, V_{OUT} = 1.1 V, I_{OUT} = 20 A		91.38%		
T_A	Operating temperature			25		°C

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 External Component Selection

Refer to *节 8.2.2.2.2* for guidelines for this design with all ceramic output capacitors.

The external components selection is a simple process when using organic semiconductors or special polymer output capacitors.

1. SELECT OPERATION MODE AND SOFT-START TIME

   Select operation mode and soft-start time using 表 7-3.
2. SELECT SWITCHING FREQUENCY

   Select the switching frequency from 250 kHz to 1 MHz using 表 7-1.
3. CHOOSE THE INDUCTOR

   The inductance value should be determined to give the ripple current of approximately 1/4 to 1/2 of maximum output current. Larger ripple current increases output ripple voltage and improves signal-to-noise ratio and helps ensure stable operation, but increases inductor core loss. Using 1/3 ripple current to maximum output current ratio, the inductance can be determined by 方程式 8.

$$L = \frac{1}{I_{IND(ripple)} \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} = \frac{3}{I_{OUT(max)} \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \tag{8}$$

   The inductor requires a low DCR to achieve good efficiency. It also requires enough room above peak inductor current before saturation. The peak inductor current can be estimated in 方程式 9.

$$I_{IND(peak)} = \frac{V_{TRIP}}{32 \times R_{DS(on)}} + \frac{1}{L \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \tag{9}$$

4. CHOOSE THE OUTPUT CAPACITORS

   When organic semiconductor capacitors or specialty polymer capacitors are used, for loop stability, capacitance and ESR should satisfy 方程式 6. For jitter performance, 方程式 10 is a good starting point to determine ESR.

$$ESR = \frac{V_{OUT} \times 10\,mV \times (1-D)}{0.6\,V \times I_{IND(ripple)}} = \frac{10\,mV \times L \times f_{SW}}{0.6\,V} = \frac{L \times f_{SW}}{60}\,(\Omega) \tag{10}$$

   where

   - D is the duty factor.
   - The required output ripple slope is approximately 10 mV per t_{SW} (switching period) in terms of VFB terminal voltage.

5. DETERMINE THE VALUE OF R1 AND R2

   The output voltage is programmed by the voltage-divider resistor, R1 and R2 shown in 图 7-4. R1 is connected between VFB pin and the output, and R2 is connected between the VFB pin and GND. Recommended R2 value is from 1 kΩ to 20 kΩ. Determine R1 using 方程式 11.

$$R1 = \frac{V_{OUT} - \frac{I_{IND(ripple)} \times ESR}{2} - 0.6}{0.6} \times R2 \tag{11}$$

6. CHOOSE THE OVERCURRENT SETTING RESISTOR

   The overcurrent setting resistor, R_{TRIP}, can be determined by 方程式 12 .

$$R_{TRIP}(k\Omega) = \frac{\left(I_{OCP} - \left(\frac{1}{2 \times L \times f_{SW}}\right) \times \frac{\left(V_{IN} - V_{OUT}\right) \times V_{OUT}}{V_{IN}}\right) \times 32 \times R_{DS(on)}\,(m\Omega)}{I_{TRIP}(\mu A)} \tag{12}$$

   where

   - I_{TRIP} is the TRIP pin sourcing current (10 µA).
   - $R_{DS(on)}$ is the thermally compensated on-time resistance value of the low-side MOSFET.

   Use an $R_{DS(on)}$ value of 1.6 mΩ for an overcurrent level of approximately 20 A. Use an $R_{DS(on)}$ value of 1.7 mΩ for overcurrent level of approximately 10 A.

8.2.1.3 Application Curves

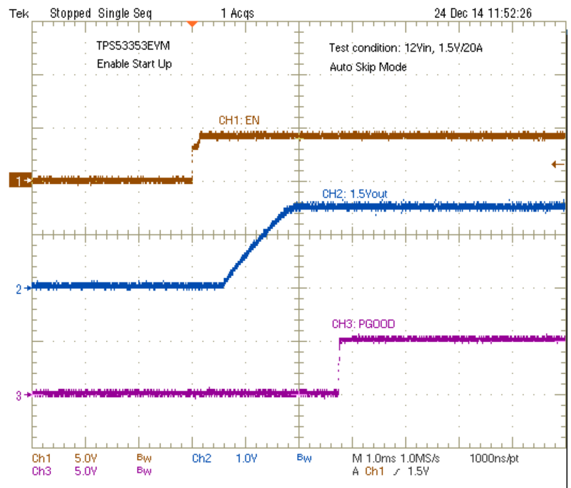

图 8-2. Enable Turnon

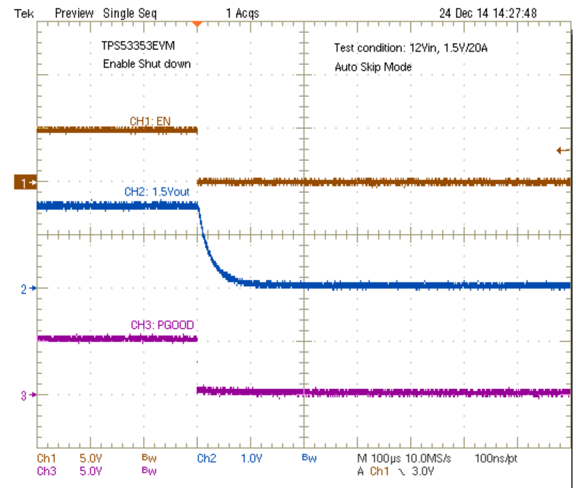

图 8-3. Enable Turnoff

8.2.2 Typical Application Circuit Diagram With Ceramic Output Capacitors

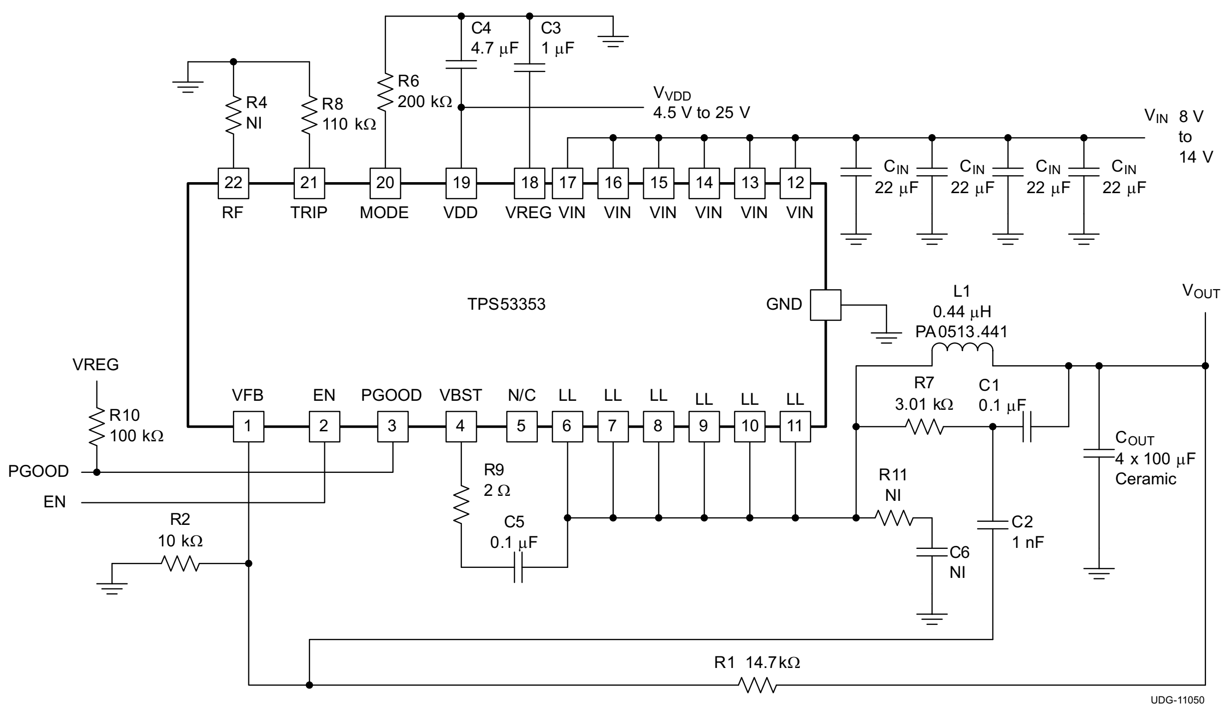

图 8-4. Typical Application Circuit Diagram With Ceramic Output Capacitors

8.2.2.1 Design Requirements

表 8-2. Design Parameters

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	Voltage range		8	12	14	V
I_{MAX}	Maximum Input current	V_{IN} = 8 V, I_{OUT} = 20 A		4.1		A
	No load input current	V_{IN} = 14 V, I_{OUT} = 0 A with auto-skip mode		1		mA
OUTPUT CHARACTERISTICS						
V_{OUT}	Output voltage			1.5		V
	Output voltage regulation	Line regulation, 8 V ⩽ V_{IN} ⩽ 15 V		0.1%		
		Load regulation, V_{IN} = 12 V, 0 A ⩽ I_{OUT} ⩽ 20 A with FCCM		0.2%		
V_{RIPPLE}	Output voltage ripple	V_{IN} = 12 V, I_{OUT} = 20 A with FCCM		20		mV_{PP}
I_{LOAD}	Output load current		0		20	A
I_{OCP}	Output overcurrent threshold			26		A
t_{SS}	Soft-start time			1.4		ms
SYSTEMS CHARACTERISTICS						
f_{SW}	Switching frequency			500		kHz
η	Peak efficiency	V_{IN} = 12 V, V_{OUT} = 1.1 V, I_{OUT} = 10 A		91.87%		
	Full load efficiency	V_{IN} = 12 V, V_{OUT} = 1.1 V, I_{OUT} = 20 A		91.38%		
T_A	Operating temperature			25		°C

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 External Component Selection

Refer to *节 8.2.2.2.2* for guidelines for this design with all ceramic output capacitors.

The external components selection is a simple process when using organic semiconductors or special polymer output capacitors.

1. **Select Operation Mode and Soft-Start Time**

   Select operation mode and soft-start time using 表 7-3.
2. **Select Switching Frequency**

   Select the switching frequency from 250 kHz to 1 MHz using 表 7-1.
3. **Choose The Inductor**

   The inductance value should be determined to give the ripple current of approximately 1/4 to 1/2 of maximum output current. Larger ripple current increases output ripple voltage and improves signal-to-noise ratio and helps ensure stable operation, but increases inductor core loss. Using 1/3 ripple current to maximum output current ratio, the inductance can be determined by 方程式 8.

$$L = \frac{1}{I_{IND(ripple)} \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} = \frac{3}{I_{OUT(max)} \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \quad (13)$$

   The inductor requires a low DCR to achieve good efficiency. It also requires enough room above peak inductor current before saturation. The peak inductor current can be estimated in 方程式 9.

$$I_{IND(peak)} = \frac{V_{TRIP}}{32 \times R_{DS(on)}} + \frac{1}{L \times f_{SW}} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \quad (14)$$

4. **External Component Selection with All Ceramic Output Capacitors**

   Refer to 节 *8.2.2.2.2* to select external components because ceramic output capacitors are used in this design.

5. **Choose the Overcurrent Setting Resistor**

   The overcurrent setting resistor, R_{TRIP}, can be determined by 方程式 15.

$$R_{TRIP}(k\Omega) = \frac{\left(I_{OCP} - \left(\frac{1}{2 \times L \times f_{SW}}\right) \times \frac{\left(V_{IN} - V_{OUT}\right) \times V_{OUT}}{V_{IN}}\right) \times 32 \times R_{DS(on)}(m\Omega)}{I_{TRIP}(\mu A)} \quad (15)$$

   where

   - I_{TRIP} is the TRIP pin sourcing current (10 µA).
   - $R_{DS(on)}$ is the thermally compensated on-time resistance value of the low-side MOSFET.

   Use an $R_{DS(on)}$ value of 1.6 mΩ for an overcurrent level of approximately 20 A. Use an $R_{DS(on)}$ value of 1.7 mΩ for overcurrent level of approximately 10 A.

6. **BST Resistor Selection**

   The recommended BST resistor value is 2 Ω and anything larger than 5.1 Ω is not recommended. Note that when the gate drive turns on, the voltage on the boot-strap capacitor splits between the internal pull-up resistance and the boot-strap resistance, with the internal circuits only seeing the portion across the internal pull-up resistance. Therefore, when the external resistor gets larger than the pull-up resistance, it crashes the head-room of the SW to BOOT logic, which can cause logic issues with the high-side gate driver.

8.2.2.2.2 External Component Selection Using All Ceramic Output Capacitors

When a ceramic output capacitor is used, the stability criteria in 方程式 6 cannot be satisfied. The ripple injection approach as shown in 图 8-4 is implemented to increase the ripple on the VFB pin and make the system stable. In addition to the selections made using Steps 1 through Step 5 in 节 *8.2.2.2.1*, the ripple injection components must be selected. The C2 value can be fixed at 1 nF. The value of C1 can be selected from 10 nF to 200 nF.

$$\frac{L \times C_{OUT}}{R7 \times C1} > N \times \frac{t_{ON}}{2} \tag{16}$$

where

- N is the coefficient to account for L and C_{OUT} variation.

N is also used to provide enough margin for stability. It is recommended N = 2 for $V_{OUT} \leqslant$ 1.8 V and N = 4 for $V_{OUT} \geqslant$ 3.3 V or when L $\leqslant$ 250 nH. The higher V_{OUT} needs a higher N value because the effective output capacitance is reduced significantly with higher DC bias. For example, a 6.3-V, 22-μF ceramic capacitor may have only 8 μF of effective capacitance when biased at 5 V.

Because the VFB pin voltage is regulated at the valley, the increased ripple on the VFB pin causes the increase of the VFB DC value. The AC ripple coupled to the VFB pin has two components, one coupled from SW node and the other coupled from the VOUT pin and they can be calculated using 方程式 17 and 方程式 18 when neglecting the output voltage ripple caused by equivalent series inductance (ESL).

$$V_{INJ\_SW} = \frac{V_{IN} - V_{OUT}}{R7 \times C1} \times \frac{D}{f_{SW}} \tag{17}$$

$$V_{INJ\_OUT} = ESR \times I_{IND(ripple)} + \frac{I_{IND(ripple)}}{8 \times C_{OUT} \times f_{SW}} \tag{18}$$

It is recommended that V_{INJ_SW} to be less than 50 mV and V_{INJ_TOTAL} to be less than 60mV. If the calculated V_{INJ_SW} is higher than 50 mV, then other parameters must be adjusted to reduce it. For example, C_{OUT} can be increased to satisfy 方程式 16 with a higher R7 value, thereby reducing V_{INJ_SW}. Use 方程式 19 to calculate C_{OUT} capacitance needed. For a more holistic calculation, please reference the TPS53353 calculator on ti.com

$$C_{OUT} = \frac{V_{IN(MAX)} - V_{OUT}}{2 \times L \times V_{INJ(MAX)}} \times N \times t_{ON} \tag{19}$$

The DC voltage at the VFB pin can be calculated by 方程式 20:

$$V_{VFB} = 0.6 + \frac{V_{INJ\_SW} + V_{INJ\_OUT}}{2} \tag{20}$$

And the resistor divider value can be determined by 方程式 21:

$$R1 = \frac{V_{OUT} - V_{VFB}}{V_{VFB}} \times R2 \tag{21}$$

8.2.2.3 Application Curves

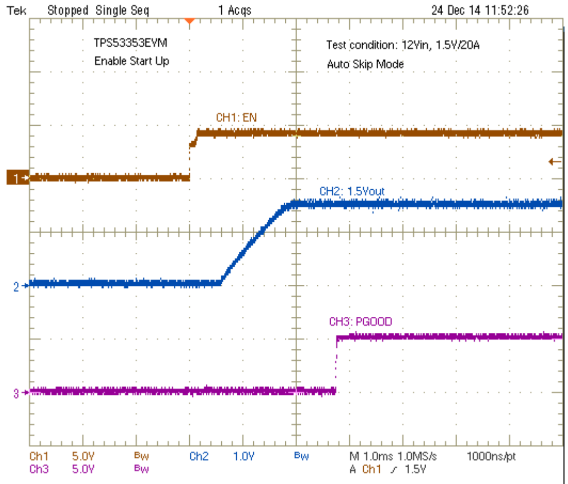

图 8-5. Enable Turnon

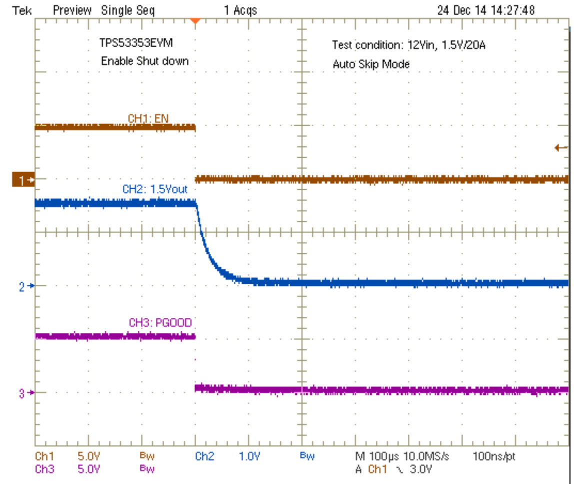

图 8-6. Enable Turnoff

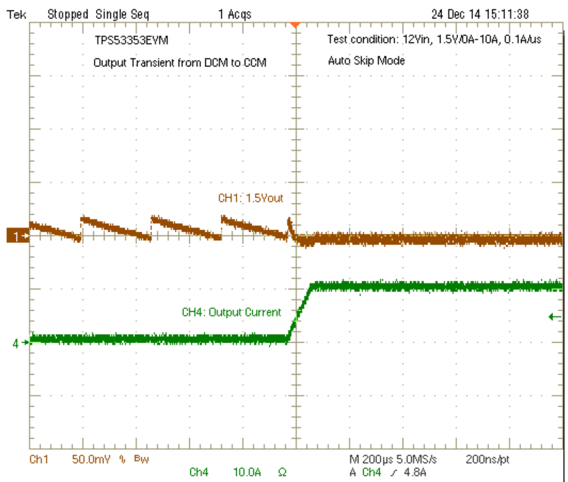

图 8-7. Output Transient from DCM to CCM

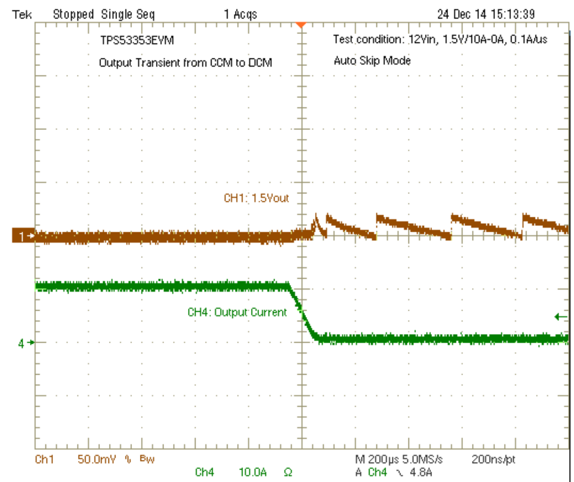

图 8-8. Output Transient from DCM to DCM

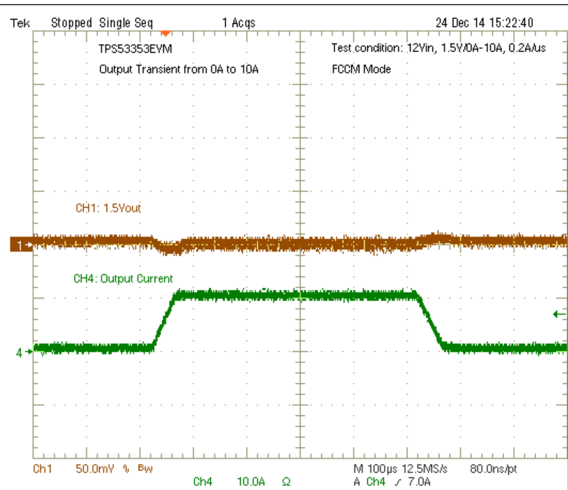

图 8-9. Output Transient with FCCM Mode

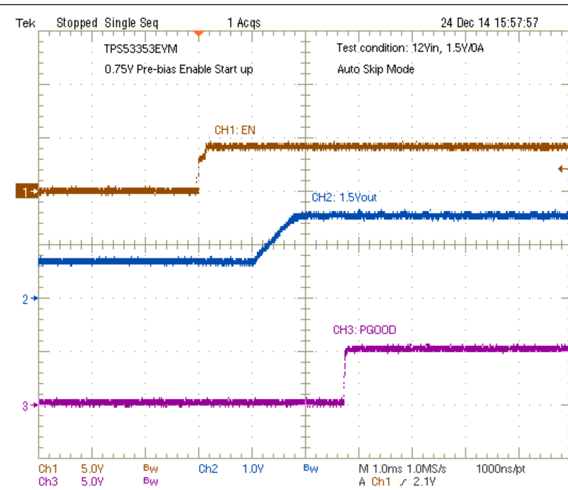

图 8-10. Output 0.75-V Prebias Turnon

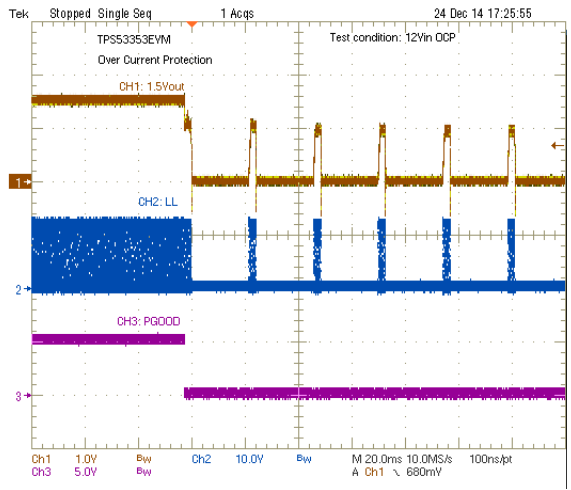

图 8-11. Output Overcurrent Protection

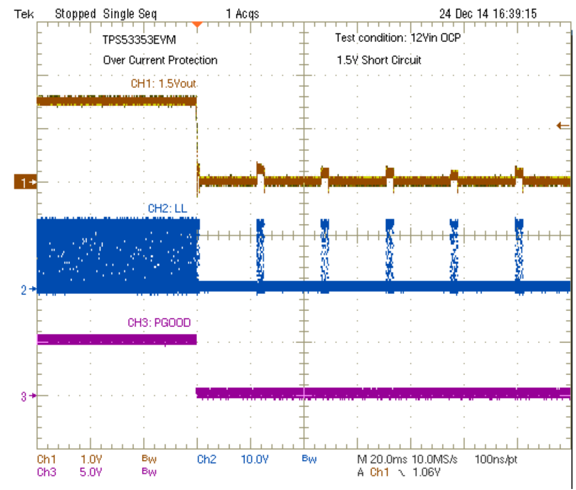

图 8-12. Output Short-Circuit Protection

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 1.5 V to 22 V (4.5 V to 25 V biased). This input supply must be well regulated. Proper bypassing of input supplies and internal regulators is also critical for noise performance, as is PCB layout and grounding scheme. See the recommendations in 节 10.

10 Layout

10.1 Layout Guidelines

Certain points must be considered before starting a layout work using the TPS53353.

- The power components (including input/output capacitors, inductor and TPS53353) should be placed on one side of the PCB (solder side). At least one inner plane should be inserted, connected to ground, in order to shield and isolate the small signal traces from noisy power lines.
- All sensitive analog traces and components such as VFB, PGOOD, TRIP, MODE and RF should be placed away from high-voltage switching nodes such as LL, VBST to avoid coupling. Use internal layer(s) as ground plane(s) and shield feedback trace from power traces and components.
- Place the VIN decoupling capacitors as close to the VIN and PGND pins as possible to minimize the input AC current loop.
- Because the TPS53353 controls output voltage referring to voltage across VOUT capacitor, the top-side resistor of the voltage divider should be connected to the positive node of the VOUT capacitor. The GND of the bottom side resistor should be connected to the GND pad of the device. The trace from these resistors to the VFB pin should be short and thin.
- Place the frequency setting resistor (R_F), OCP setting resistor (R_{TRIP}) and mode setting resistor (R_{MODE}) as close to the device as possible. Use the common GND via to connect them to GND plane if applicable.
- Place the VDD and VREG decoupling capacitors as close to the device as possible. Ensure to provide GND vias for each decoupling capacitor and make the loop as small as possible.
- The PCB trace defined as switch node, which connects the LL pins and high-voltage side of the inductor, should be as short and wide as possible.
- Connect the ripple injection V_{OUT} signal (V_{OUT} side of the C1 capacitor in 图 8-4) from the terminal of ceramic output capacitor. The AC coupling capacitor (C2 in 图 8-4) should be placed near the device, and R7 and C1 can be placed near the power stage.
- Use separated vias or trace to connect LL node to snubber, boot strap capacitor and ripple injection resistor. Do not combine these connections.

10.2 Layout Example

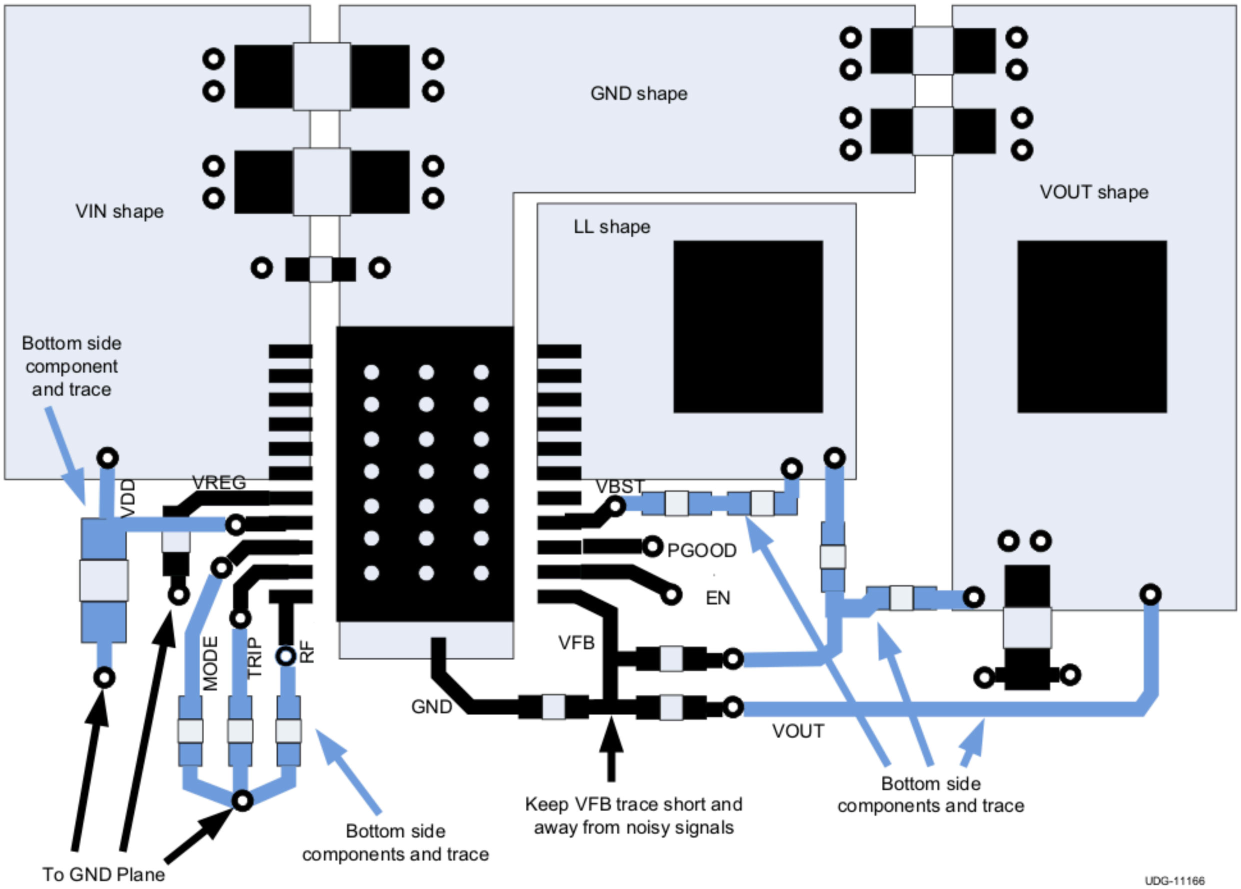

图 10-1. Layout Recommendation

11 Device and Documentation Support

11.1 Device Support

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链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS53353DQPR	Active	Production	LSON-CLIP (DQP) | 22	2500 | LARGE T&R	ROHS Exempt	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	53353DQP
TPS53353DQPR.A	Active	Production	LSON-CLIP (DQP) | 22	2500 | LARGE T&R	ROHS Exempt	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	53353DQP
TPS53353DQPR.B	Active	Production	LSON-CLIP (DQP) | 22	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TPS53353DQPRG4	Active	Production	LSON-CLIP (DQP) | 22	2500 | LARGE T&R	ROHS Exempt	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	53353DQP
TPS53353DQPRG4.A	Active	Production	LSON-CLIP (DQP) | 22	2500 | LARGE T&R	ROHS Exempt	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	53353DQP
TPS53353DQPRG4.B	Active	Production	LSON-CLIP (DQP) | 22	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TPS53353DQPT	Active	Production	LSON-CLIP (DQP) | 22	250 | SMALL T&R	ROHS Exempt	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	53353DQP
TPS53353DQPT.A	Active	Production	LSON-CLIP (DQP) | 22	250 | SMALL T&R	ROHS Exempt	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	53353DQP
TPS53353DQPT.B	Active	Production	LSON-CLIP (DQP) | 22	250 | SMALL T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

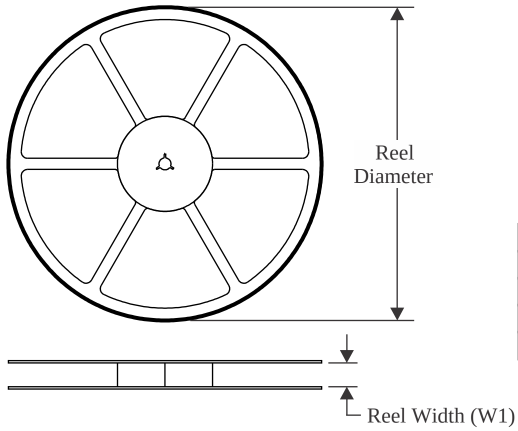
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

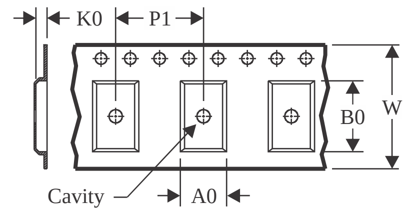
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

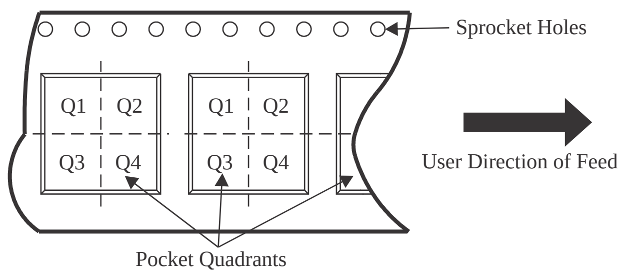


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

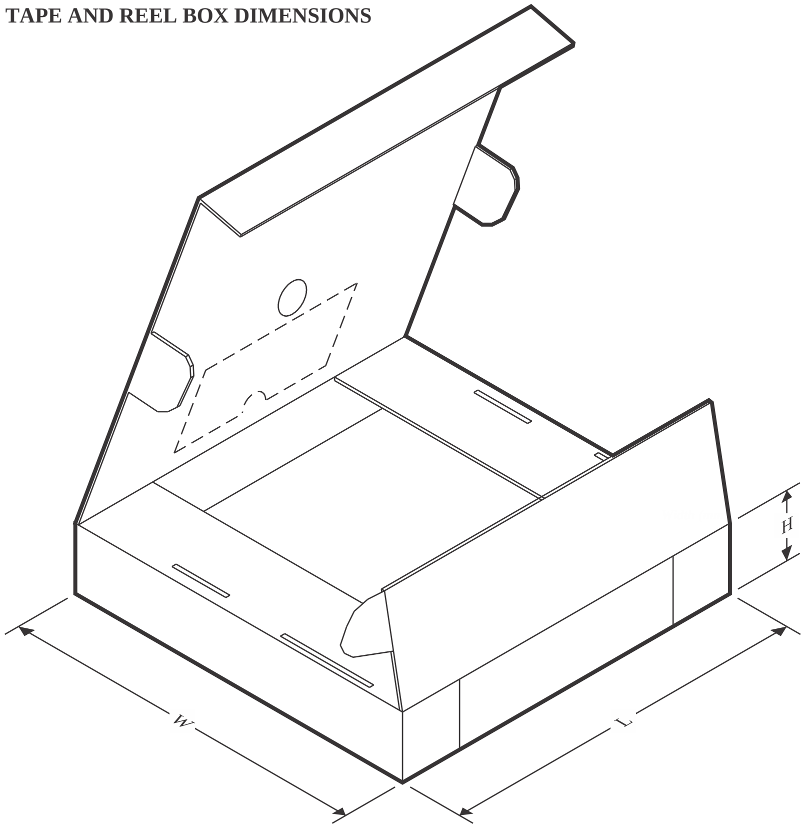
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53353DQPR	LSON-CLIP	DQP	22	2500	330.0	15.4	5.3	6.3	1.8	8.0	12.0	Q1
TPS53353DQPR	LSON-CLIP	DQP	22	2500	330.0	12.4	5.3	6.3	1.8	8.0	12.0	Q1
TPS53353DQPRG4	LSON-CLIP	DQP	22	2500	330.0	12.4	5.3	6.3	1.8	8.0	12.0	Q1
TPS53353DQPT	LSON-CLIP	DQP	22	250	180.0	12.4	5.3	6.3	1.8	8.0	12.0	Q1

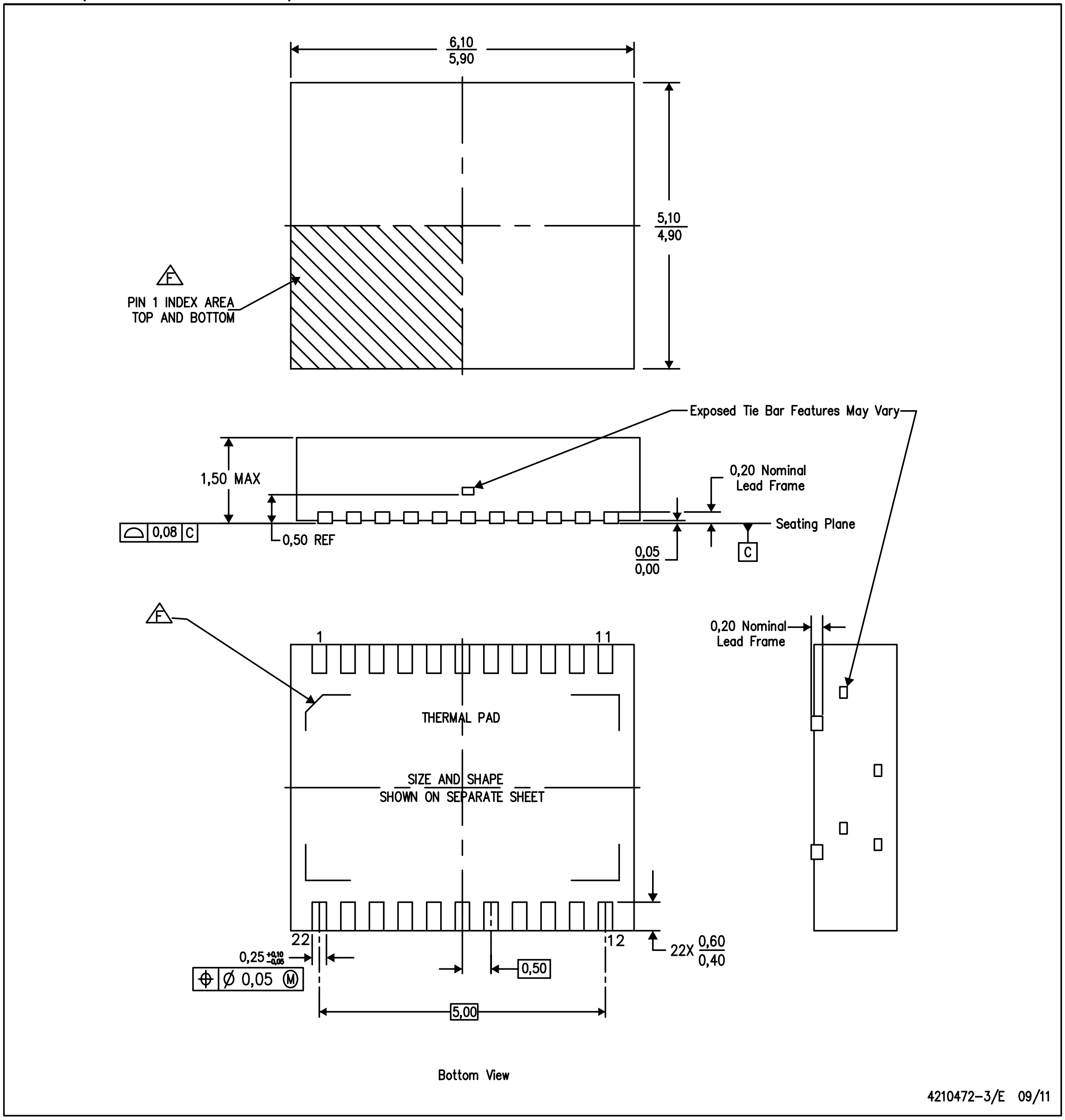
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53353DQPR	LSON-CLIP	DQP	22	2500	336.6	336.6	41.3
TPS53353DQPR	LSON-CLIP	DQP	22	2500	346.0	346.0	33.0
TPS53353DQPRG4	LSON-CLIP	DQP	22	2500	346.0	346.0	33.0
TPS53353DQPT	LSON-CLIP	DQP	22	250	210.0	185.0	35.0

DQP (R–PSON–N22) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

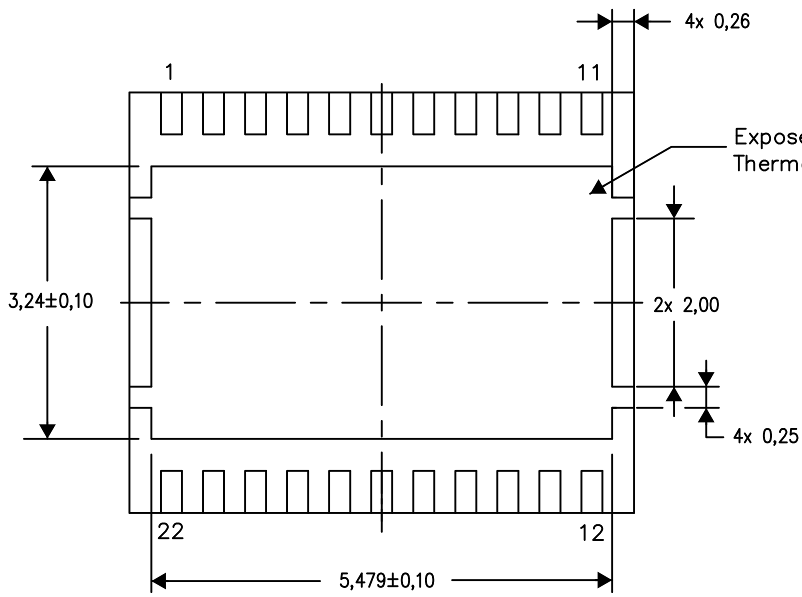
DQP (R–PSON–N22) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



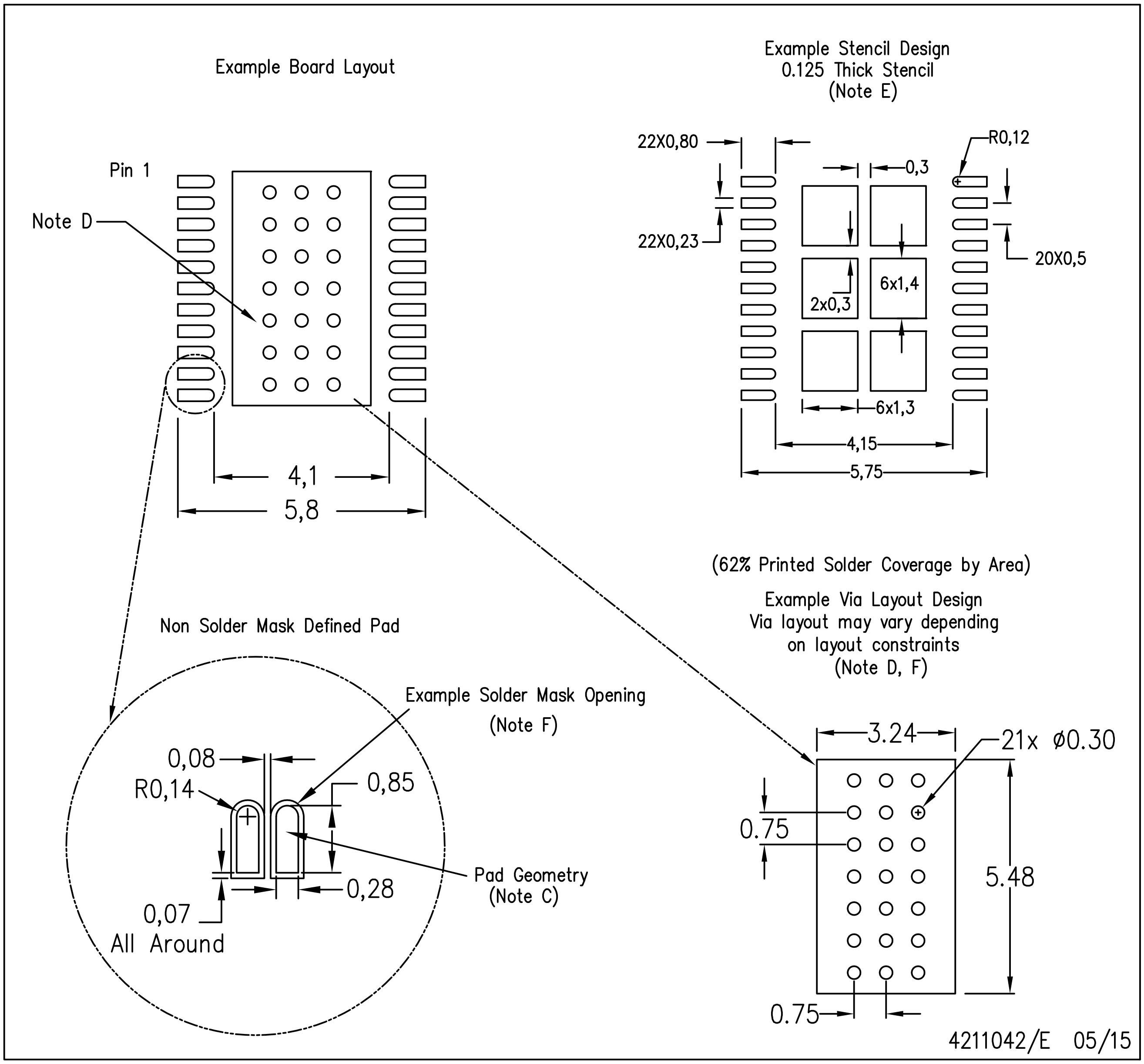
Bottom View

Exposed Thermal Pad Dimensions

4211024–3/H 08/15

NOTE: All linear dimensions are in millimeters

DQP (R–PSON–N22) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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