具有集成式 3A、40V 电源开关的 TPS61500 高亮度 LED 驱动器

1 特性

- 输入电压范围为 2.9V 至 18V
- 3A、40V 内部电源开关
  - 四个由 5V 输入供电的 3W LED
  - 八个由 12V 输入供电的 3W LED
- 高效电源转换：效率高达 93%
- 可由外部电阻器设置的频率范围：200kHz 至 2.2MHz
- 用户定义的软启动至满负载
- 可编程过压保护
- 模拟和纯 PWM 亮度调节
- 14 引脚 HTSSOP 封装 - 带 PowerPAD™

2 应用

- 监视器背光
- 1W 或 3W 高亮度 LED

3 说明

TPS61500 是一款具有集成式 3A、40V 电源开关的单片开关稳压器。它是适用于高亮度 1W 或 3W LED 的理想驱动器。该器件具有宽输入电压范围，可支持输入电压来自多节电池或者 5V 或 12V 稳压电源轨的应用。

通过外部传感器电阻器 R3 来设置 LED 电流，通过电流模式 PWM（脉宽调制）控制环路将反馈电压调节至 200mV，如*典型应用电路* 中所示。该器件支持通过模拟和纯 PWM 调光方法来实现 LED 亮度控制。将一个电容器连接至 DIMC 引脚可以配置要用于模拟调光的器件，LED 电流以与外部 PWM 信号的占空比成比例的方式进行变化。将 DIMC 引脚悬空可针对纯 PWM 调光对器件进行配置，此时平均 LED 电流是 PWM 信号的占空比乘以设定的 LED 电流。
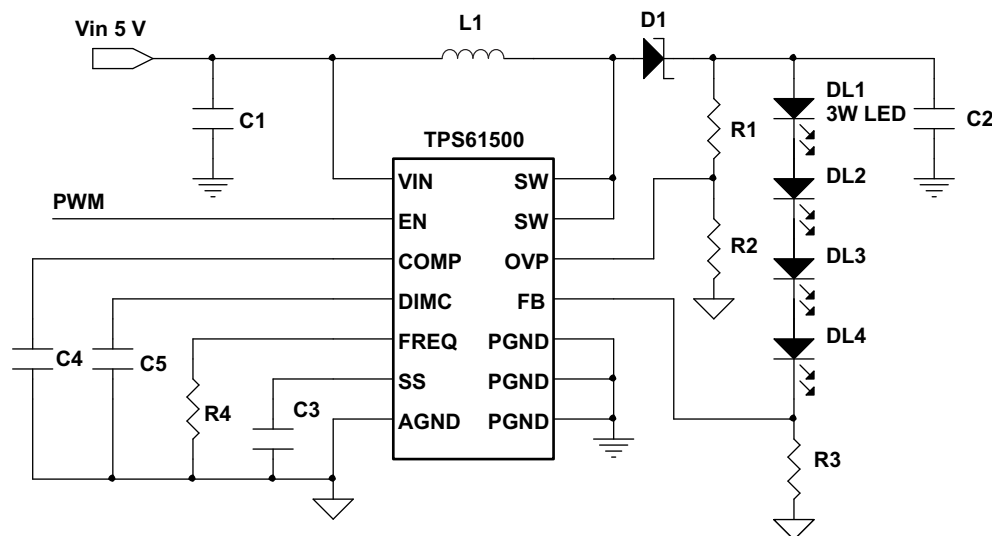
该器件 具有 用于在启动期间限制浪涌电流的可编程软启动功能，并且具有其他内置保护 功能，如逐脉冲过流限制、过压保护和热关断。TPS61500 采用带 PowerPAD 的 14 引脚 HTSSOP 封装。

器件信息[1]

器件型号	封装	封装尺寸（标称值）
TPS61500	HTSSOP (14)	5.00mm × 4.40mm

[1] 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用电路

目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision E (March 2018) to Revision F	**Page**
• 仅有编辑更改，无技术性修订 1	

Changes from Revision D (June 2017) to Revision E	**Page**
• 已更改 在*典型应用电路* 中将 R3 的接地符号从"PGND"更改成了"AGND" 1	
• Changed ground symbol of R3 change from PGND to AGND in *Figure 7* 12	
• Changed ground symbol of R3 change from PGND to AGND in *Figure 11* 17	

Changes from Revision C (March 2015) to Revision D	**Page**
• Changed "Analog and PWM dimming frequency" to "PWM dimming frequency" in ROC table; add separate row for "Analog dimming frequency".. 4	
• Added sentence at end of *Analog Dimming Method* 11	

Changes from Revision B (March 2012) to Revision C	**Page**
• 已添加 添加了 *引脚配置和功能* 部分、*ESD 额定值* 表、*特性 说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 1	

Changes from Revision A (February 2012) to Revision B	**Page**
• 将"订购信息"表中的"封装标记"从"TPS61500PWP"更改成了"61500".. 1	

Changes from Original (December 2008) to Revision A	**Page**
• Replaced the *Dissipation Ratings* Table with *Thermal Information*.. 4	

5 Pin Configuration and Functions

PWP Package
14-Pin HTSSOP With Thermal Pad
Top View
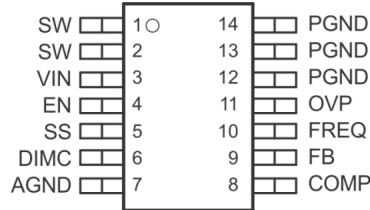
Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	7	I	Signal ground of the IC
COMP	8	O	Output of the transconductance error amplifier. An external RC network is connected to this pin.
DIMC	6	I	Analog and PWM dimming method option pin. A capacitor connected to the pin to set the time constant of reference for analog dimming. Float this pin for PWM dimming.
EN	4	I	Enable pin. When the voltage of this pin falls below the enable threshold for more than 10 ms, the IC turns off. This pin is also used for PWM signal input for LED brightness dimming.
FB	9	I	Feedback pin for positive voltage regulation. A resistor connects to this pin to program LED current.
FREQ	10	O	Switch frequency program pin. An external resistor is connected to this pin. See *Application Information* for information on how to size the FREQ resistor.
OVP	11	I	Overvoltage protection for LED driver. The voltage is 1.229 V. Using a resistor divider can program the threshold of OVP.
PGND	12-14	I	Power ground of the IC. It is connected to the source of the PWM switch.
SS	5	O	Soft start programming pin. A capacitor between the SS pin and GND pin programs soft-start timing. See *Application and Implementation* for information on how to size the SS capacitor
SW	1, 2	I	This is the switching node of the IC. Connect SW to the switched side of the inductor.
Thermal Pad	—	—	Solder the thermal pad to the analog ground. If possible, use thermal via to connect to top and internal ground plane layers for ideal power dissipation.
VIN	3	I	The input pin to the IC. Connect VIN to a supply voltage between 2.9 V and 18 V. It is acceptable for the voltage on the pin to be different from the boost power stage input for applications requiring voltage beyond V_{IN} range.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

	MIN	MAX	UNIT
Supply voltages on pin VIN[2]	−0.3	20	V
Voltages on pins EN[2]	−0.3	20	V
Voltage on pin FB, FREQ and COMP, OVP[2]	−0.3	3	V
Voltage on pin DIMC, SS[2]	−0.3	7	V
Voltage on pin SW[2]	−0.3	40	V
Continuous power dissipation	See *Thermal Information*		
Operating junction temperature	−40	150	°C
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.9		18	V
V_O	Output voltage	V_{IN}		38	V
L	Inductor[1]	4.7		47	μH
C_I	Input capacitor	4.7		—	μF
C_O	Output capacitor	4.7		10	μF
Cdim	Analog dimming capacitor[2]	0.1		—	μF
PWM	PWM dimming frequency[3]	200		1000	Hz
	Analog dimming frequency[3]	200		40 000	
T_A	Operating ambient temperature	−40		85	°C
T_J	Operating junction temperature	−40		125	°C

(1) The inductance value depends on the switching frequency and end applications. While larger values may be used, values between 4.7 μH and 47 μH have been successfully tested in various applications. Refer to *Selecting the Inductor* for details.
(2) The Cdim with the internal resistor (25 kΩ typical) forms a RC filter that generates the FB reference voltage according to the duty cycle of PWM signal. To optimize the RC filter and reduce the output ripple, the value larger than 0.1 μF of Cdim is recommended.
(3) When analog dimming, the maximum PWM frequency is set by on the RC filter to optimize the output ripple. When PWM dimming, the PWM frequency is set by the device loop response.

6.4 Thermal Information

THERMAL METRIC[1]		TPS61500	UNIT
		PWP (HTSSOP)	
		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	45.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	29.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

FSW = 1.2 MHz (Rfreq = 80 kΩ), Vin = 3.6 V, CRTL = Vin, T_A = –40°C to +85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{IN}	Input voltage range		2.9		18	V
I_Q	Operating quiescent current into VIN	Device PWM switching without load, V_{IN} = 3.6 V			3.5	mA
I_{SD}	Shutdown current	EN = GND, V_{IN} = 3.6 V			1.5	µA
V_{UVLO}	Undervoltage lockout threshold	V_{IN} falling		2.5	2.7	V
V_{hys}	Undervoltage lockout hysteresis			130		mV
ENABLE AND REFERENCE CONTROL						
V_{enh}	EN logic high voltage	V_{IN} = 2.9 V to 18 V	1.2			V
V_{enl}	EN logic low voltage	V_{IN} = 2.9 V to 18 V			0.4	V
R_{en}	EN pulldown resistor		400	800	1600	kΩ
T_{off}	Shutdown delay, SS discharge	EN high to low	10			ms
VOLTAGE AND CURRENT CONTROL						
V_{REF}	Voltage feedback regulation voltage		195	200	205	mV
I_{FB}	Voltage feedback input bias current				200	nA
V_{EA_OFF}	Error amplifier offset		–10	0	10	mV
I_{sink}	COMP pin sink current	V_{FB} = V_{REF} + 200 mV, V_{COMP} = 1 V		40		µA
I_{source}	COMP pin source current	V_{FB} = V_{REF} –200 mV, V_{COMP} = 1 V		40		µA
V_{CCLP}	COMP pin clamp voltage	High clamp		3		V
		Low clamp		0.75		
V_{CTH}	COMP pin threshold	Duty cycle = 0%		0.95		V
G_{ea}	Error amplifier transconductance		240	340	440	µmho
R_{ea}	Error amplifier output resistance			10		MΩ
f_{ea}	Error amplifier crossover frequency			500		kHz

Electrical Characteristics (continued)

FSW = 1.2 MHz (Rfreq = 80 kΩ), Vin = 3.6 V, CRTL = Vin, T_A = −40°C to +85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FREQUENCY						
f_S	Oscillator frequency	Rfreq = 480 kΩ Rfreq = 80 kΩ Rfreq = 40 kΩ	0.16 1.0 1.76	0.21 1.2 2.2	0.26 1.4 2.64	MHz
D_{max}	Maximum duty cycle	Rfreq = 80 kΩ	89%	93%		
V_{FREQ}	FREQ pin voltage			1.229		V
T_{min_on}	Minimum on pulse width	Rfreq = 80 kΩ		60		ns
R_{dim_fil}	Dimming filter resistance			25		kΩ
POWER SWITCH						
$R_{DS(ON)}$	N-channel MOSFET on-resistance	$V_{IN} = V_{GS}$ = 3.6 V		0.13	0.25	Ω
		$V_{IN} = V_{GS}$ = 3 V			0.3	
I_{LN_NFET}	N-channel leakage current	V_{DS} = 40 V, T_A = 25°C			1	μA
OC, OVP and SS						
I_{LIM}	N-Channel MOSFET current limit	D = D_{max}	3	3.8	5	A
I_{SS}	Soft-start bias current	Vss = 0 V		6		μA
V_{OVP}	Overvoltage protection threshold		1.192	1.229	1.266	V
V_{OVP_hys}	Overvoltage protection hysteresis			40		mV
THERMAL SHUTDOWN						
$T_{shutdown}$	Thermal shutdown threshold			160		°C
$T_{hysteresis}$	Thermal shutdown threshold hysteresis			15		°C

6.6 Typical Characteristics

Table 1. Table of Graphs

		FIGURE
Efficiency	V_{IN} = 5 V, 4 LEDs, 8 LEDs, 10 LEDs	Figure 1
Efficiency	V_{IN} = 5 V, 12 V; V_{OUT} = 8 LEDs	Figure 2
FB voltage accuracy	vs Temperature	Figure 3
Switch current limit	vs Duty cycle	Figure 4
Switch current limit	vs Temperature	Figure 5

Circuit of *Typical Application Circuit* ; L1 = D104C2-10 μH; D1 = SS3P6L-E3/86A, R4 = 80 kΩ, C4 = 470 nF, C2 = 10 μF, LED = OSRAM LCW W5SM, I_{LED} = 400 mA; unless otherwise noted.
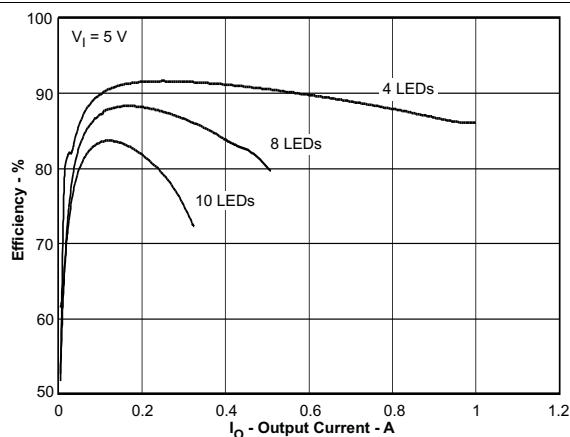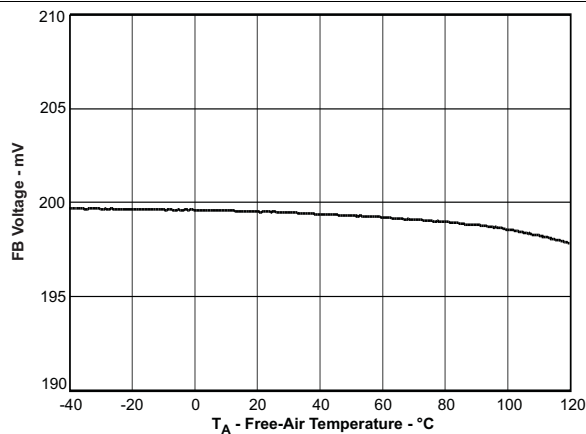

Figure 1. Efficiency
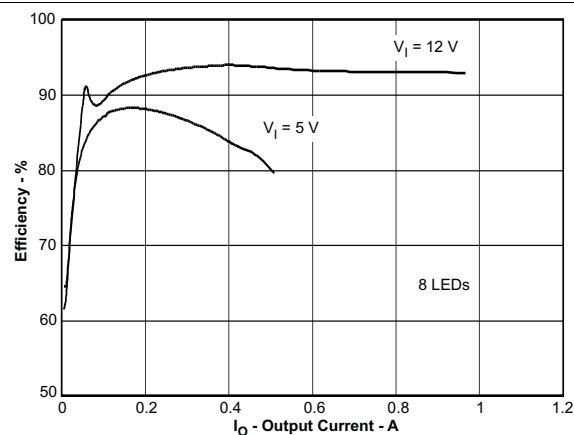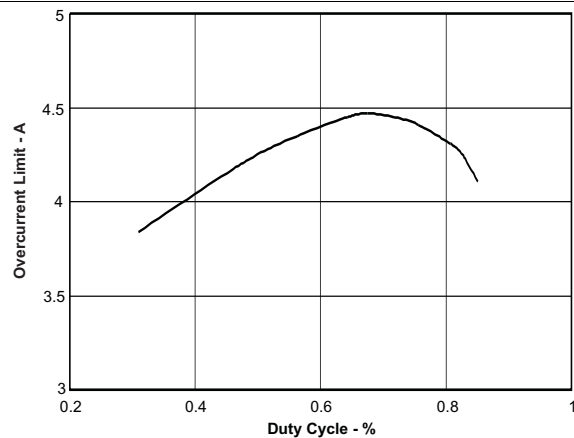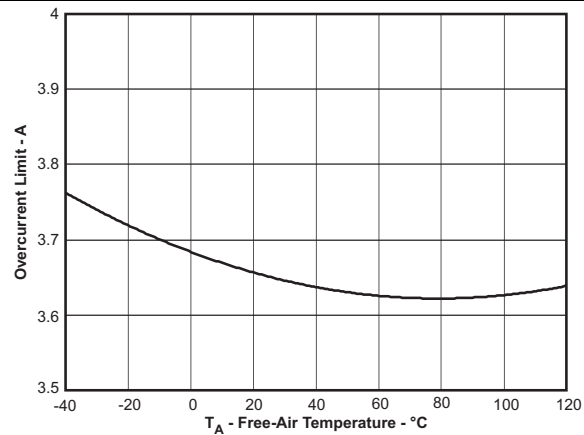

Figure 2. Efficiency

Figure 3. FB Voltage Accuracy

Figure 4. Switch Current Limit

Circuit of *Typical Application Circuit* ; L1 = D104C2-10 μH; D1 = SS3P6L-E3/86A, R4 = 80 kΩ, C4 = 470 nF, C2 = 10 μF, LED = OSRAM LCW W5SM, I_{LED} = 400 mA; unless otherwise noted.

Figure 5. Switch Current Limit

7 Detailed Description

7.1 Overview

The TPS61500 integrates a 3-A, 40-V low side switch FET for driving up to 10 high-brightness LEDs in series. The device regulates the FB pin voltage at 200 mV with current mode pulse width modulation (PWM) control, and the LED current is sensed through a low-value resistor in series with LEDs.

The PWM control circuitry turns on the switch at the beginning of each switching cycle. The input voltage is applied across the inductor and stores the energy as inductor current ramps up. During this portion of the switching cycle, the load current is provided by the output capacitor. When the inductor current rises to the threshold set by the error amplifier output, the power switch turns off and the external Schottky diode is forward biased. The inductor transfers stored energy to replenish the output capacitor and supply the load current. This operation repeats each switching cycle. As shown in *Functional Block Diagram*, the duty cycle of the converter is determined by the PWM control comparator which compares the error amplifier output and the current signal. The switching frequency is programmed by the external resistor.

A ramp signal from the oscillator is added to the current ramp. This slope compensation is necessary to avoid sub-harmonic oscillation that is intrinsic to the current mode control at duty cycle higher than 50%. The feedback loop regulates the FB pin to a reference voltage through an error amplifier. The output of the error amplifier is connected to the COMP pin. An external compensation network is connected to the COMP pin to optimize the feedback loop for stability and transient response.

7.2 Functional Block Diagram
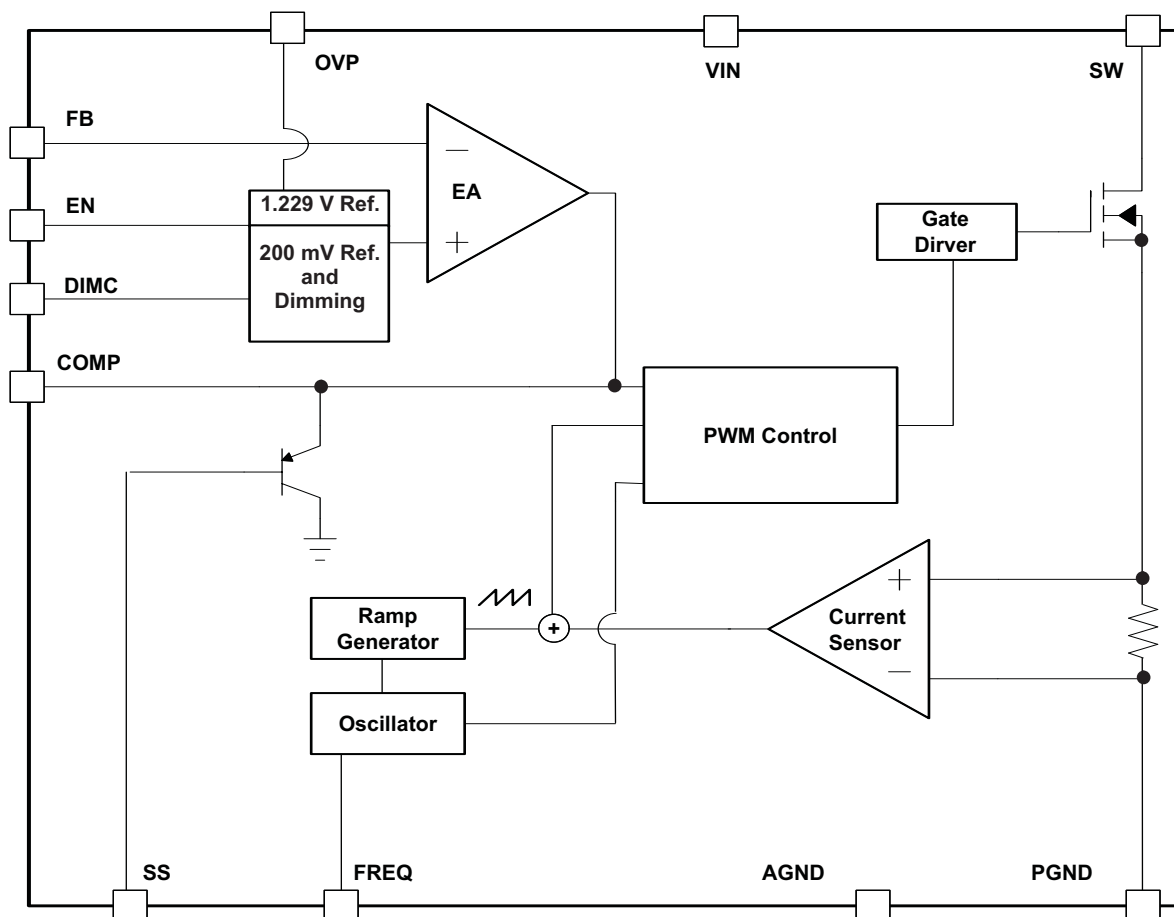
7.3 Feature Description

7.3.1 Switching Frequency

The switch frequency is determined by a resistor connected to the FREQ pin of the TPS61500. Do not leave this pin open. A resistor must always be connected for proper operation. See Table 2 and Figure 6 for resistor values and corresponding frequencies.

Table 2. Switching Frequency vs External Resistor

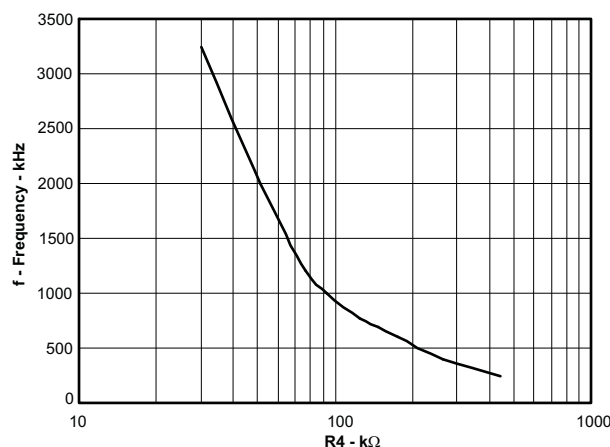| R4 (kΩ)	f$_{SW}$ (kHz)
443	240
256	400
176	600
80	1200
51	2000

Figure 6. Switching Frequency vs External Resistor

Increasing switching frequency reduces the value of external capacitors and inductors, but also reduces the power conversion efficiency. The user must set the frequency for compromise between efficiency and solution size.

7.3.2 Soft Start

The TPS61500 has a built-in soft-start circuit that significantly reduces the start-up current spike and output voltage overshoot. When the device is enabled, an internal bias current (typically 6 μA) charges a capacitor (C3) on the SS pin. The voltage at the capacitor clamps the output of the internal error amplifier that determines the duty cycle of PWM control, thereby the input inrush current is eliminated. Once the capacitor reaches 1.8 V, the soft-start cycle is completed, and the soft-start voltage no longer clamps the error amplifier output. Refer to Figure 14 and Figure 10 for the soft-start waveform. A 47-nF capacitor eliminates the output overshoot and reduces the peak inductor current for most applications.

When the EN is pulled low for 10 ms, the IC enters shutdown, and the SS capacitor discharges through a 5-kΩ resistor for the next soft start.

7.3.3 Enable and Thermal Shutdown

The TPS61500 enters shutdown when the EN voltage is less than 0.4 V for more than 10 ms. In shutdown, the input supply current for the device is less than 1.5 μA (maximum). The EN pin has an internal 800-kΩ pulldown resistor to disable the device when it is floating.

An internal thermal shutdown turns off the device when the typical junction temperature of 160°C is exceeded. The device restarts when the junction temperature drops by 15°C.

7.3.4 Undervoltage Lockout (UVLO)

An undervoltage lockout prevents mis-operation of the device at input voltages below typical 2.5 V. When the input voltage is below the undervoltage threshold, the device remains off and the internal switch FET is turned off. The undervoltage lockout threshold is set below minimum operating voltage of 2.9 V to avoid any transient VIN dip triggering the UVLO and causing the device to reset. For the input voltages between UVLO threshold and 2.9 V, the device maintains its operation, but the specifications are not ensured.

7.3.5 Overvoltage Protection

When the FB pin is shorted to ground or an LED fails open circuit, the output voltage can increase to potentially damaging voltages. To present the device and the output capacitor from exceeding the maximum voltage rating, utilize the OVP pin with an external resistor divider to program an OVP threshold, as shown in the typical application. The OVP pin is set at 1.229 V, and the OVP threshold should be higher than the normal operating output voltage.

7.4 Device Functional Modes

7.4.1 PWM Dimming Method

LED brightness is controlled by peak LED current and duty cycle of external PWM signal. See Figure 11, Figure 12, and Figure 13, for the PWM dimming operating and linearity. Additional external switch FETs connect/disconnect LED string during PWM on/off period, shown in Figure 7. Simultaneously, the TPS61500 samples and holds the COMP voltage to speed up LED current regulation during the on period. Because the device and the external switch FETs must have several hundred microseconds to regulate the LED current, the frequency and minimum duty cycle of the PWM signal are application dependent. For example, 2% is the minimum duty cycle for a 200-Hz PWM signal.

The PWM dimming method offers better control of color because current through LED is kept constant each cycle.

7.4.2 Analog Dimming Method

When capacitor C5 is connected to the DIMC pin, the FB regulation voltage is scaled proportional to the external PWM signal's duty cycle; therefore, it achieves LED brightness change, shown in Figure 7. The relationship between the duty cycle and LED current is given by Equation 1:

$$I_{LED} = \frac{V_{FB}}{R3} \times Duty$$

where

- Duty is the duty cycle of the PWM signal.   (1)

The device chops up the internal 200-mV reference voltage at the duty cycle of the PWM signal. The pulsed reference voltage is then filtered by a low pass filter that is composed of an internal 25-kΩ resistor and the external capacitor C5. The output of the filter is connected to the error amplifier as the reference voltage for the FB pin. Therefore, although a PWM signal is used for brightness dimming, only the LED DC current is modulated. This eliminates the audible noise that often occurs when the LED current is pulsed during PWM dimming. Unlike other methods for filtering the PWM signal, the device analog dimming method is independent of the PWM logic voltage level which often has large variations.

For optimum performance, TI recommends that the value of C5 be as large as possible to provide adequate filtering for the PWM frequency. For example, when the PWM frequency is 5-kHz, C5 equal to 1 μF is sufficient. The recommended minimum PWM on time at start-up is 200 μs. After start-up, TI recommends a minimum PWM duty cycle of 1%.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS61500 integrates a 3-A, 40-V low-side switch FET for driving up to 10 high brightness LEDs in series. The device regulates the FB pin voltage at 200 mV with current mode PWM control, and the LED current is sensed through a low value resistor in series with LEDs. The TPS61500 supports analog and pure PWM dimming methods for LED brightness control. Connecting a capacitor to the DIMC pin configures the device to be used for analog dimming, and the LED current varies proportional to the duty cycle of an external PWM signal. Floating the DIMC pin configures the device for pure PWM dimming with the average LED current being the PWM signal's duty cycle times a set LED current.

8.2 Typical Applications

8.2.1 Analog Dimming Method
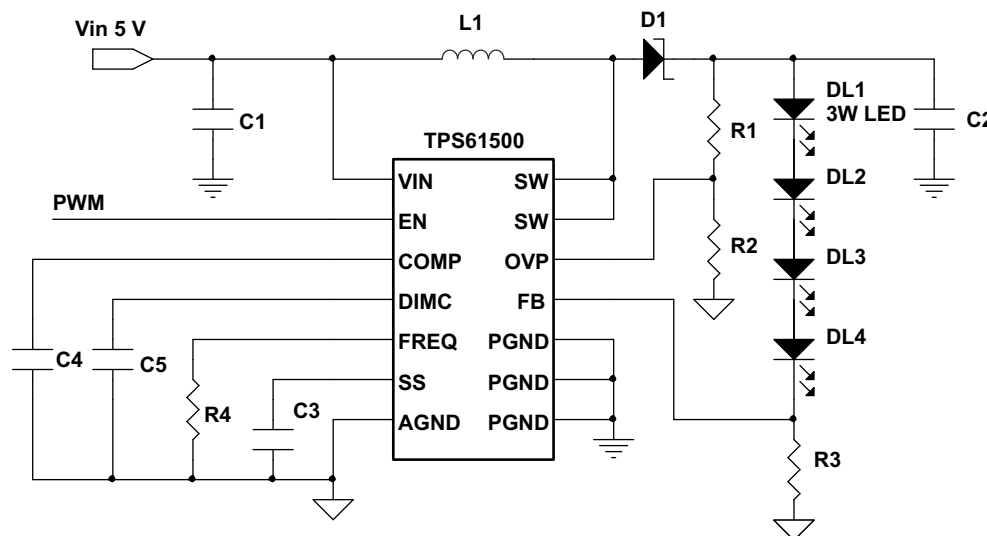
Figure 7. Analog Dimming Method

8.2.1.1 Design Requirements

Table 3. Design Parameters

PARAMETERS	VALUES
Input voltage	5 V ± 20%
LED forward voltage	3.5 V
LED current	400 mA
Number of LEDs	4
Dimming method	Analog

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Programming the Overvoltage Protection

Select the values of R1 and R2 according to Equation 2.

$$V_{OVP} = 1.229 \text{ V} \times \left(\frac{R1}{R2} + 1 \right)$$

(2)

For example, the total forward voltage of four 3-W LED is 14V, then use R1 of 120 k and R2 of 10 k to program the threshold of 16 V. In the OVP mode, the device regulates the output voltage at the OVP threshold.

When the fault is clear and the OVP pin voltage falls 40 mV below 1.229 V, IC resumes the output regulation for LED current.

8.2.1.2.2 Programming the LED Current

LED current can be determined by the value of the feedback resistor R3 and the FB pin regulation voltage of 200 mV as shown in Equation 3:

$$I_{LED} = \frac{V_{FB}}{R3}$$

(3)

The output current tolerance depends on the FB accuracy and the current sensor resistor accuracy.

8.2.1.2.3 Implementing Dimming

The TPS61500 provides two LED current dimming methods.
- Floating the DIMC pin, an external PWM signal via the EN pin, providing pure PWM dimming method.
- Connecting a capacitor larger than 100-nF to the DIMC pin, an external PWM signal via the EN pin, providing analog dimming. In this application, a 1-μF capacitor is connected to the DIMC pin.

8.2.1.2.4 Computing the Maximum Output Current

The overcurrent limit in a boost converter limits the maximum input current and thus maximum input power for a given input voltage. Maximum output power is less than maximum input power due to power conversion losses. Therefore, the current limit setting, input voltage, output voltage and efficiency can all change maximum current output. The current limit clamps the peak inductor current; therefore, the ripple has to be subtracted to derive maximum DC current. The ripple current is a function of switching frequency, inductor value and duty cycle. Equation 4 and Equation 5 take into account of all the above factors for maximum output current calculation.

$$I_p = \frac{1}{\left[L \times Fs \times \left(\frac{1}{Vout + Vf - Vin} + \frac{1}{Vin} \right) \right]}$$

where
- I_p = inductor peak-to-peak ripple
- L = inductor value
- Vf = Schottky diode forward voltage
- Fs = switching frequency
- V_{out} = output voltage = $\Sigma V_{LEDs} + V_{REF}$

(4)

$$I_{LED\_max} = \frac{Vin \times \left(I_{lim} - I_p/2 \right) \times \eta}{Vout}$$

where
- I_{LED_max} = maximum LED current from the boost converter
- I_{lim} = overcurrent limit
- V_{LED} = LED forward voltage at I_{LED}
- η = efficiency estimate based on similar applications

(5)

For instance, when V_{IN} is 12 V, 8 LEDs output is equivalent to V_{OUT} of 24 V, the inductor is 10 μH, the Schottky forward voltage is 0.4 V, and the switching frequency is 1.2 MHz; then the maximum output current is approximately 1 A in typical condition.

8.2.1.2.5 Selecting the Inductor

The selection of the inductor affects steady state operation as well as transient behavior and loop stability. These factors make it the most important component in power regulator design. There are three important inductor specifications, inductor value, DC resistance, and saturation current. Considering inductor value alone is not enough.

Inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can falls to some percentage of its 0-A value depending on how the inductor vendor defines saturation current.

Using an inductor with a smaller inductance value forces discontinuous PWM where the inductor current ramps down to zero before the end of each switching cycle. This reduces the maximum output current of the boost converter, causes large input voltage ripple and reduces efficiency. In general, large inductance value provides much more output and higher conversion efficiency. Small inductance value can give better the load transient response. For these reasons, TI recommends a 4.7-µH to 22-µH inductor value range. Table 4 lists the recommended inductor for the TPS61500.

Meanwhile, the TPS61500 can program the switching frequency. Normally, small inductance value is suitable for high frequency and vice versa. The device has built-in slope compensation to avoid sub-harmonic oscillation associated with current mode control. If the inductor value is lower than 4.7 µH, the slope compensation may not be adequate, and the loop can be unstable. Therefore, customers should verify the inductor in their application if it is different from the recommended values.

Table 4. Recommended Inductors for TPS61500

PART NUMBER	L (µH)	DCR MAX (mΩ)	SATURATION CURRENT (A)	SIZE (L × W × H mm)	VENDOR[1]
D104C2	10	44	3.6	10.4 × 10.4 × 4.8	TOKO
VLF10040	15	42	3.1	10.0 × 9.7 × 4.0	TDK
CDRH105RNP	22	61	2.9	10.5 × 10.3 × 5.1	Sumida
MSS1038	15	50	3.8	10.0 × 10.2 × 3.8	Coilcraft

(1)   See *Third-Party Products* disclaimer.

8.2.1.2.6 Selecting the Schottky Diode

The high switching frequency of the TPS61500 demands a high-speed rectification for optimum efficiency. Ensure that the diode's average and peak current rating exceed the average output current and peak inductor current. In addition, reverse breakdown voltage of the diode must exceed the switch FET rating voltage of 40 V. TI recommends the VISHAY SS3P6L-E3/86A the TPS61500 device. The power dissipation of the diode package must be larger than the $I_{OUT(max)} \times V_D$

8.2.1.2.7 Selecting the Compensation Capacitor and Resistor

The TPS61500 has an external compensation, COMP pin, which allows the loop response to be optimized for each application. The COMP pin is the output of the internal error amplifier. An external ceramic capacitor, C4, is connected to the COMP pin to stabilize the feedback loop. Use 470 nF for C4.

8.2.1.2.8 Selecting the Input and Output Capacitor

The output capacitor is selected mainly to meet the requirements for the output ripple and loop stability. This ripple voltage is related to the capacitor capacitance and its equivalent series resistance (ESR). Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by

$$C_{out} = \frac{(V_{out} - V_{in})I_{out}}{V_{out} \times Fs \times V_{ripple}}$$

where

- V_{ripple} = peak-to-peak output ripple (6)

The additional output ripple component caused by ESR is calculated using:

$$V_{ripple\_ESR} = I_{out} \times R_{ESR}$$

(7)

Due to its low ESR, V_{ripple_ESR} can be neglected for ceramic capacitors, but must be considered if tantalum or electrolytic capacitors are used.
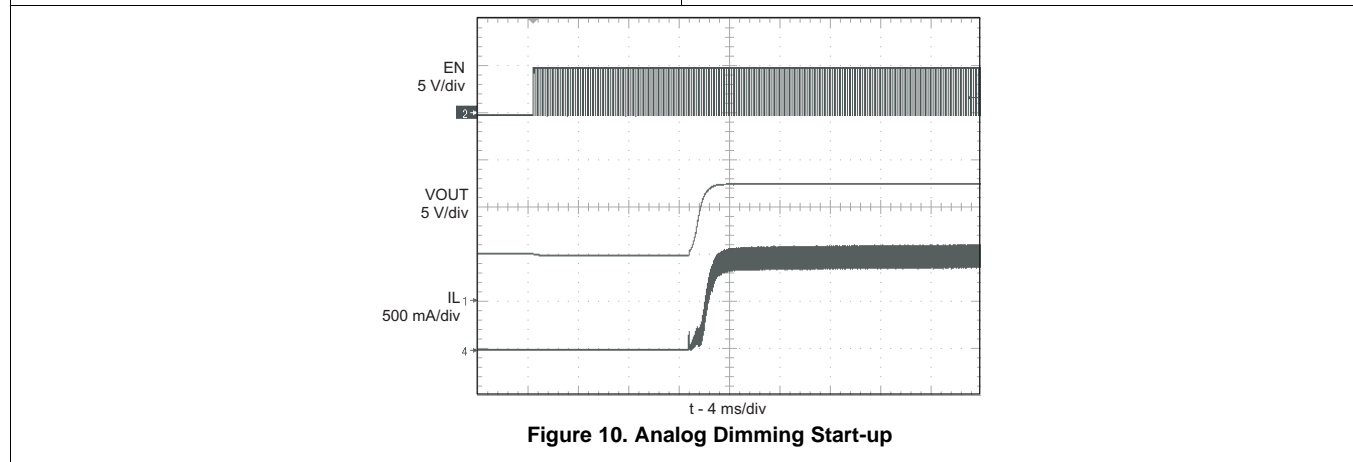
Take care when evaluating a ceramic capacitor's derating under DC bias, aging and AC signal. For example, larger form factor capacitors (in 1206 size) have their self-resonant frequencies in the range of the switching frequency; thus, the effective capacitance is significantly lower. The DC bias can also significantly reduce capacitance. Ceramic capacitors can loss as much as 50% of its capacitance at its rated voltage. Therefore, leave margin on the voltage rating to ensure adequate capacitance at the required output voltage.

TI recommends a capacitor in the range of 1 µF to 4.7 µF for input side. The output requires a capacitor in the range of 1 µF to 10 µF. The output capacitor affects the loop stability of the boost regulator. If the output capacitor is below the range, the boost regulator can potentially become unstable.

The popular vendors for high-value ceramic capacitors are:

*   **TDK** (http://www.component.tdk.com/components.php)
*   **Murata** (http://www.murata.com/cap/index.html)

8.2.1.3 Application Curves

Figure 8. Analog Dimming

Figure 9. Analog Dimming Linearity

Figure 10. Analog Dimming Start-up

8.2.2 Pure PWM Dimming Method
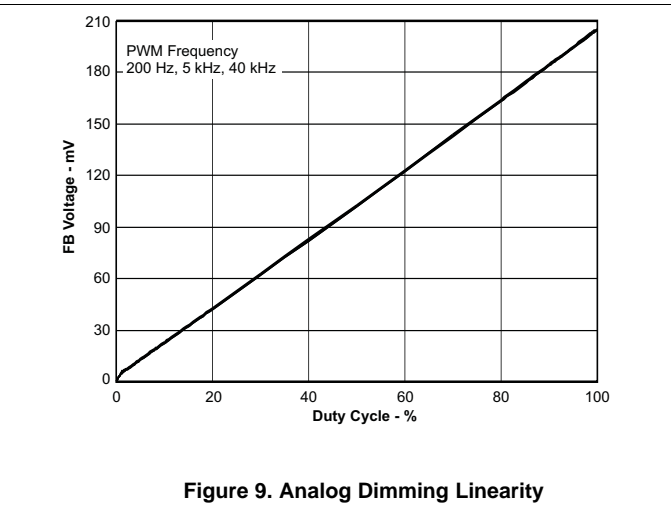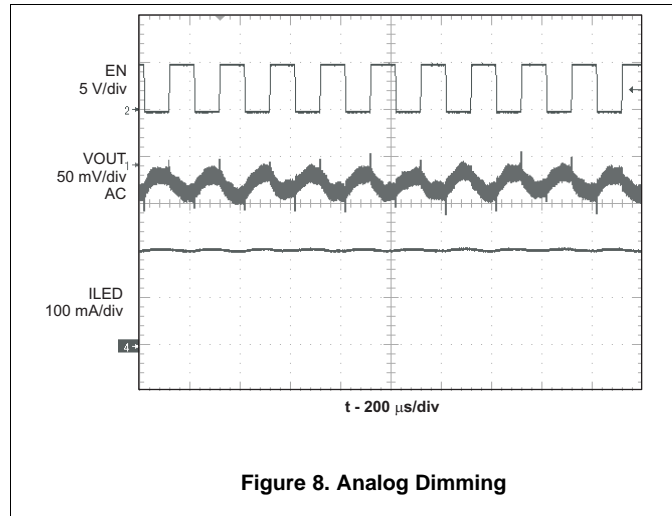
Figure 11. Pure PWM Dimming Method
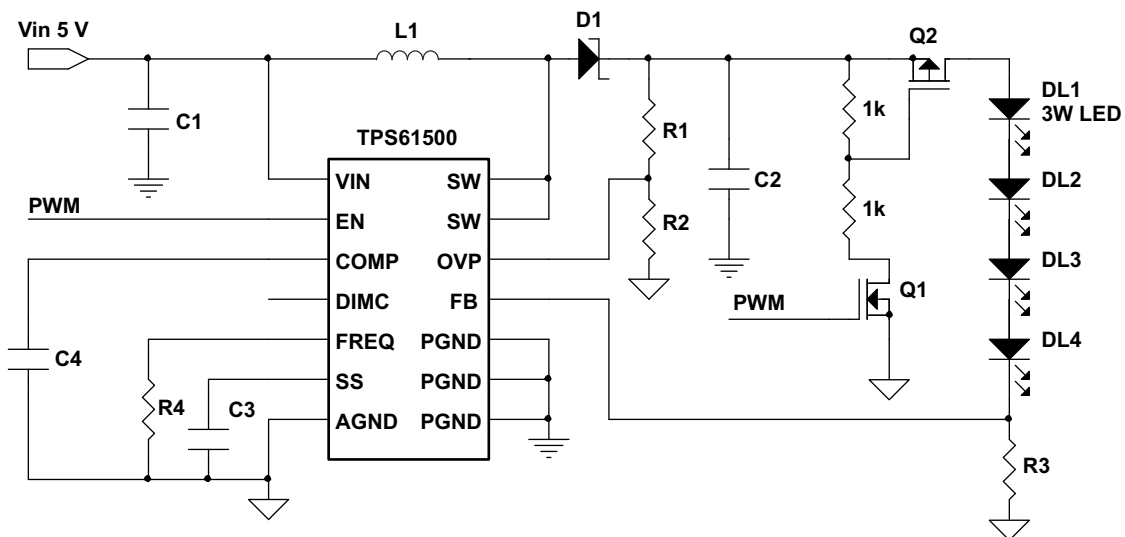
8.2.2.1 Design Requirements

Table 5. Design Parameters

PARAMETERS	VALUES
Input voltage	5 V ± 20%
LED forward voltage	3.5 V
LED current	400 mA
Number of LEDs	4
Dimming method	PWM

8.2.2.2 Detailed Design Procedure

Refer to *Detailed Design Procedure* in the *Analog Dimming Method* section.

8.2.2.3 Application Curves

Figure 12. PWM Dimming

Figure 13. PWM Dimming Linearity

Figure 14. PWM Dimming Start-up
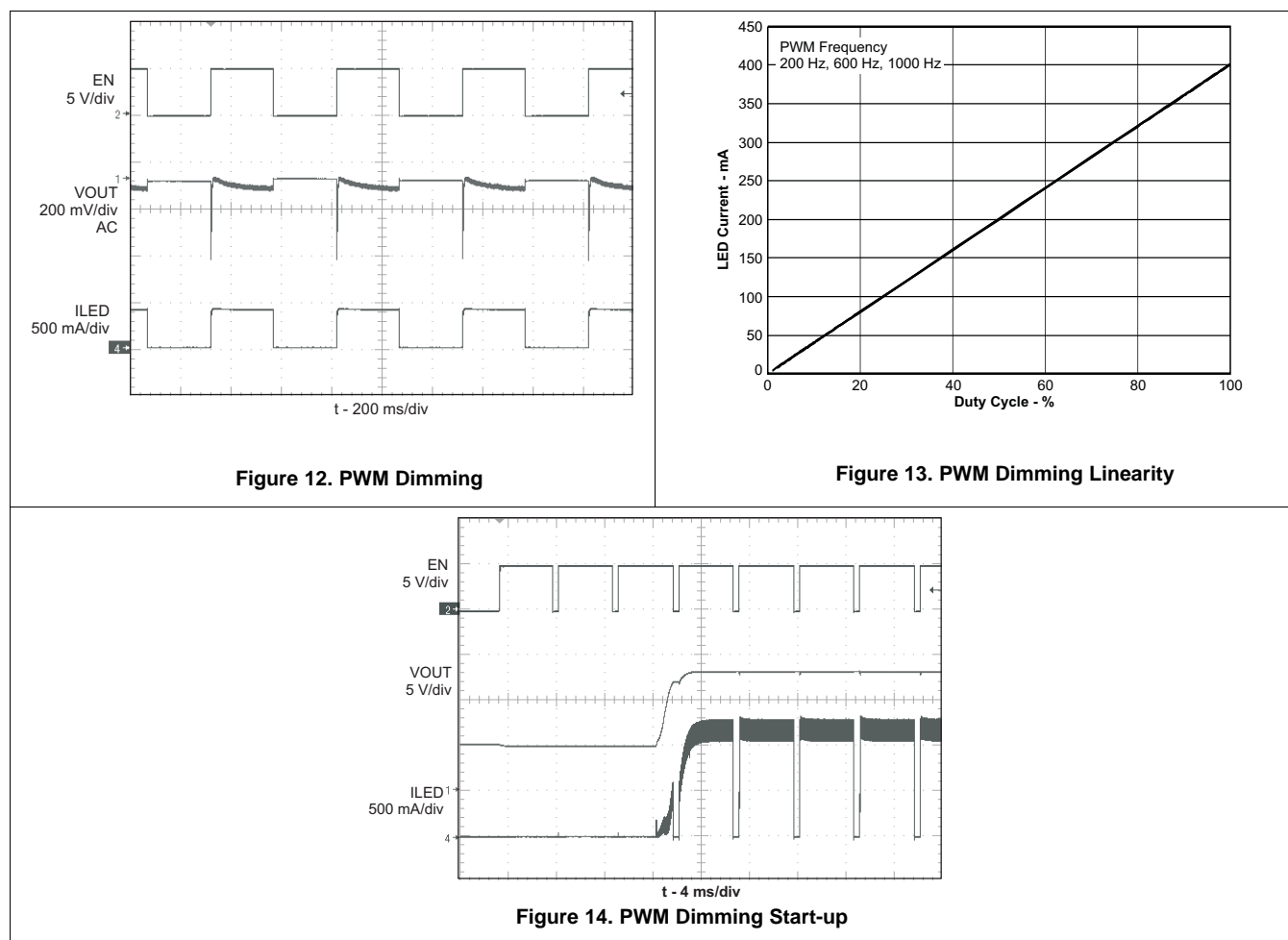
9 Power Supply Recommendations

The TPS61500 is designed to operate from an input voltage supply range between 2.9 V and 18 V. The power supply to the TPS61500 must have a current rating according to the supply voltage, output voltage, and output current of the TPS61500.

10 Layout

10.1 Layout Guidelines

As for all switching power supplies, especially those running at high switching frequency and high currents, layout is an important design step. If layout is not carefully done, the regulator could suffer from instability as well as noise problems. To maximize efficiency, switch rise and fall times are very fast. To prevent radiation of high frequency noise (for example, EMI), proper layout of the high frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin and always use a ground plane under the switching regulator to minimize interplane coupling. The high current path including the switch, Schottky diode, and output capacitor, contains nanosecond rise and fall times and must be kept as short as possible. In order to reduce the input supply ripple, the input capacitor must be close both to the VIN and GND pins.

10.2 Layout Example
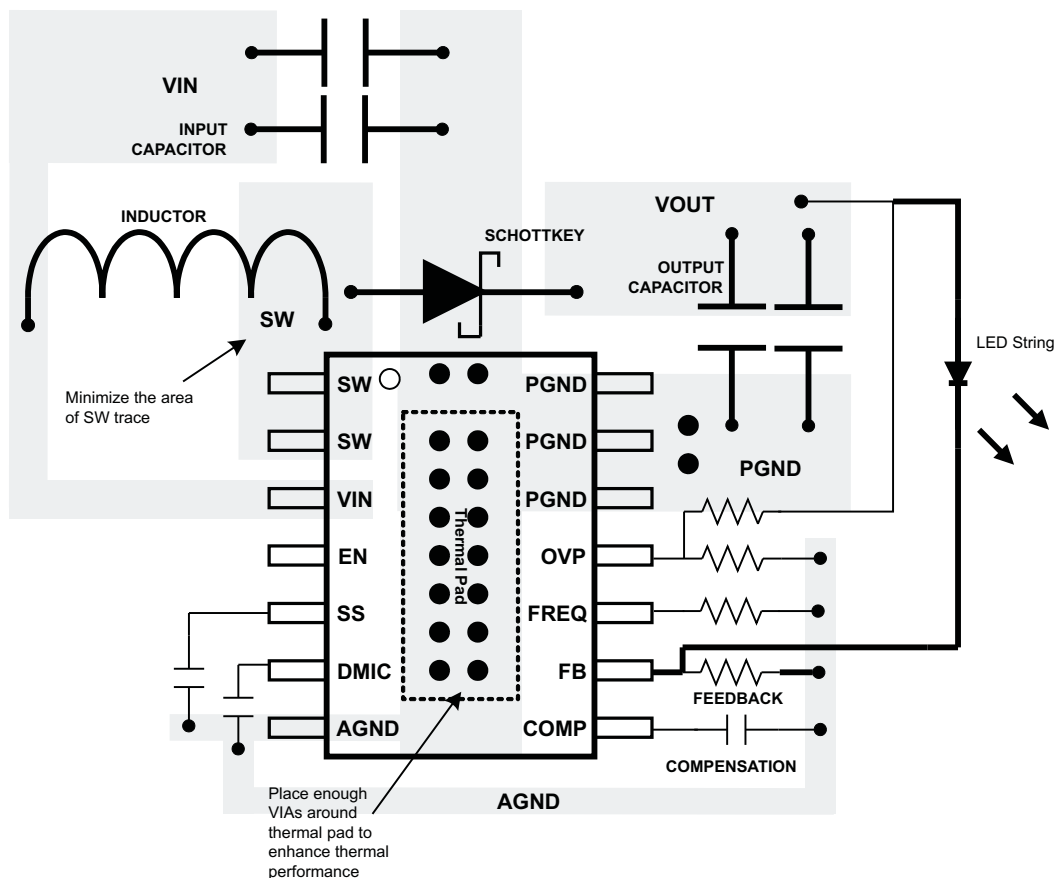
Figure 15. Recommended Layout Example

10.3 Thermal Considerations

As mentioned before, the maximum device junction temperature must be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation of the TPS61500. Calculate the maximum allowable dissipation, P_D (maximum), and keep the actual dissipation less than or equal to P_D (maximum). The maximum-power-dissipation limit is determined using Equation 8:

$$P_{D(max)} = \frac{125°C - T_A}{R_{\theta JA}}$$

where

- T_A is the maximum ambient temperature for the application
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient given in *Thermal Information* (8)

The TPS61500 comes in a thermally enhanced TSSOP package. This package includes a thermal pad that improves the thermal capabilities of the package. The $R_{\theta JA}$ of the TSSOP package greatly depends on the PCB layout.

11 器件和文档支持

11.1 器件支持

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11.1.3 社区资源

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11.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61500PWP	ACTIVE	HTSSOP	PWP	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	61500	Samples
TPS61500PWPR	ACTIVE	HTSSOP	PWP	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	61500	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61500PWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61500PWPR	HTSSOP	PWP	14	2000	350.0	350.0	43.0

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS61500PWP	PWP	HTSSOP	14	90	530	10.2	3600	3.5

PWP 14

PowerPAD TSSOP - 1.2 mm max height

4.4 x 5.0, 0.65 mm pitch

This image is a representation of the package family, actual package may vary.
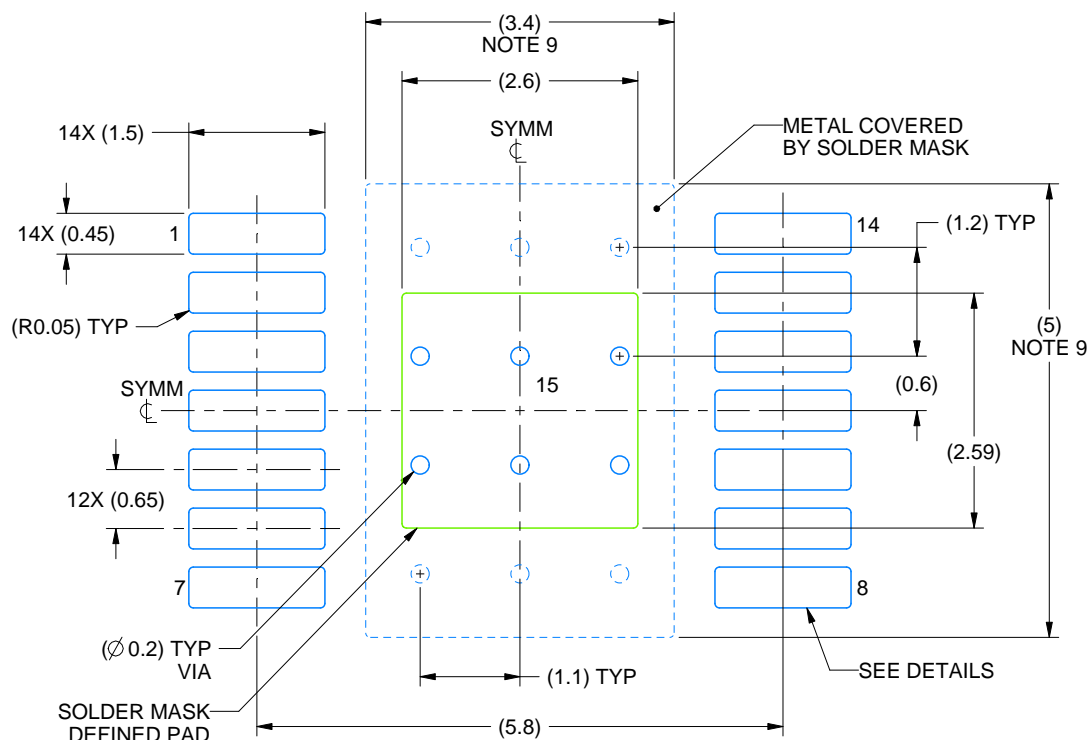Refer to the product data sheet for package details.

4224995/A

PWP0014K

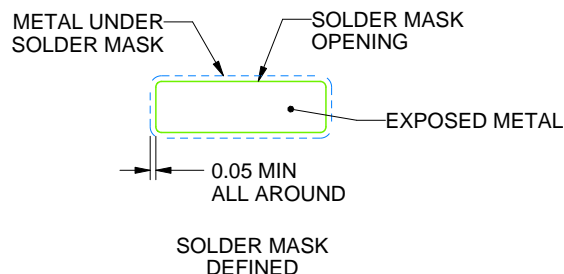PowerPAD™ TSSOP - 1.2 mm max height

6.6
6.2 TYP

A

PIN 1 INDEX
AREA

14

12X 0.65

2X

3.9

5.1
4.9
NOTE 3

1

7

8

B

4.5
4.3

14X 0.30
0.19

⊕ 0.1 Ⓜ C A B

C

0.1 C

SEATING
PLANE

SEE DETAIL A

(0.15) TYP

THERMAL
PAD

2X (0.6)
NOTE 5

2X (0.4)
NOTE 5

7

8

2.59
1.89

15

1

14

2.6
1.9

0.25

GAGE PLANE

0°-8°

0.75
0.50

1.2 MAX

0.15
0.05

DETAIL A
TYPICAL

4229706/A   06/2023

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

PWP0014K

14X (1.5)

14X (0.45)   1

(R0.05) TYP

SYMM

12X (0.65)

7

(Ø 0.2) TYP
VIA

SOLDER MASK
DEFINED PAD

(3.4)
NOTE 9

(2.6)

SYMM

METAL COVERED
BY SOLDER MASK

14   (1.2) TYP

(5)
NOTE 9

15

(0.6)

(2.59)

(1.1) TYP

(5.8)

8

SEE DETAILS

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

**NON-SOLDER MASK
DEFINED**

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

**SOLDER MASK
DEFINED**
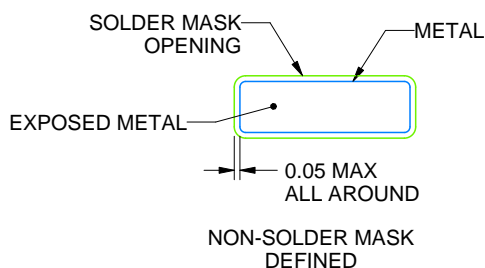
SOLDER MASK DETAILS
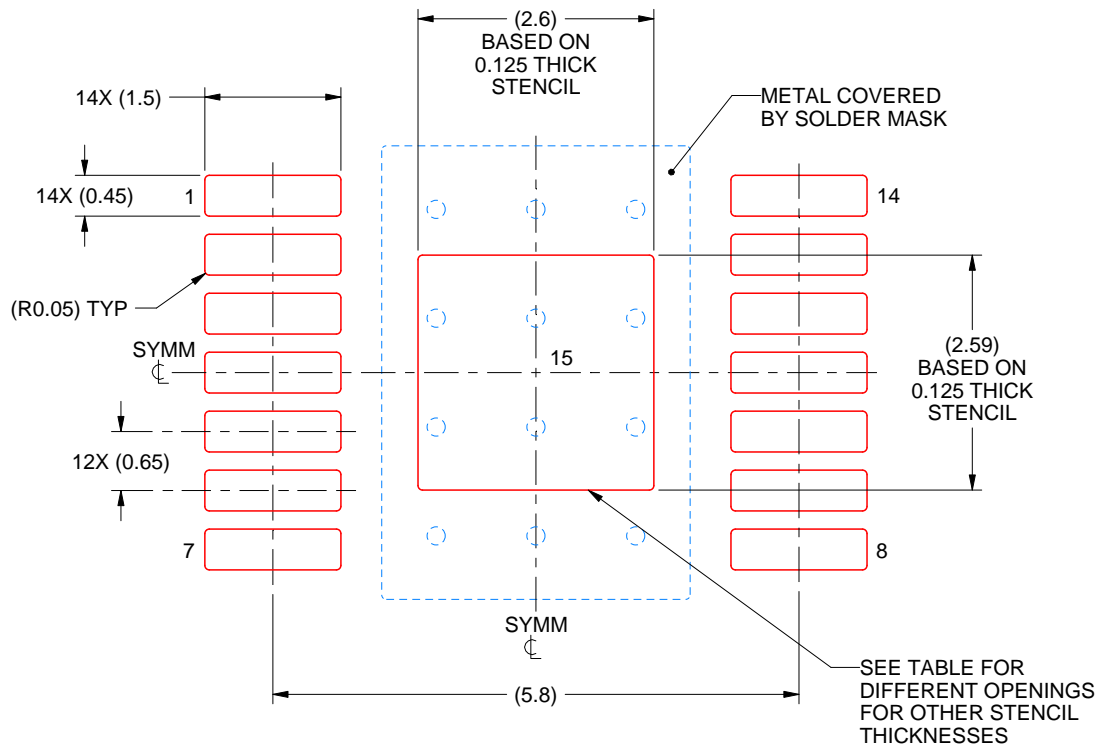
4229706/A   06/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

(2.6)
BASED ON
0.125 THICK
STENCIL

METAL COVERED
BY SOLDER MASK

14X (1.5)

14X (0.45)   1

(R0.05) TYP

SYMM

14

15

(2.59)
BASED ON
0.125 THICK
STENCIL

12X (0.65)

7

8

SYMM

SEE TABLE FOR
DIFFERENT OPENINGS
FOR OTHER STENCIL
THICKNESSES

(5.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 2.90
0.125	2.60 X 2.59 (SHOWN)
0.15	2.37 X 2.36
0.175	2.20 X 2.19

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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