具有 25µA 静态电流的 TPS7A6201-Q1 300mA、40V 低压降稳压器

1 特性

- 符合面向汽车 应用的 AEC-Q100 标准：
  - 温度等级 1：-40°C 至 125°C，T_A
  - 结温范围：–40°C 至 150°C，T_J
- 低压降：
  - 在 I_{OUT} = 150mA 时为 300mV
- 7V 至 40V 的宽输入电压范围，瞬态电压高达 45V
- 最大输出电流为 300mA
- 超低静态电流：
  - 轻负载时 $I_{QUIESCENT}$ = 25µA（典型值）
  - EN = 低电平时 I_{SLEEP} < 2µA
- 2.5V 至 7V 可调节输出电压
- 低 ESR 陶瓷输出稳定电容器
- 集成故障保护：
  - 短路和过流保护
  - 热关断
- 低输入电压跟踪
- 耐热增强型电源封装：
  - 5 引脚 TO-263（KTT、D2PAK）

2 应用

- 汽车音响主机
- 电池管理系统 (BMS)
- 混合仪表组

3 说明

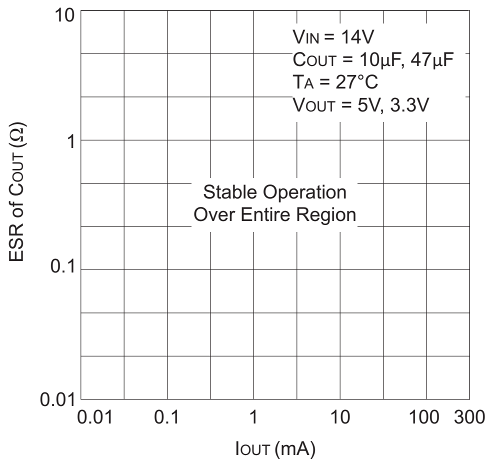
TPS7A6201-Q1 是一款低压降线性稳压器，专为在轻负载应用中实现低功耗和小于 25µA 的静态电流而 设计。该器件 具有 集成式过流保护功能，采用的设计甚至在使用低 ESR 陶瓷输出电容器时也可实现稳定工作。可使用外部电阻器对此输出电压进行编程。此低压跟踪特性便于使用更小的输入电容器，并且可能在冷启动情况下无需使用升压转换器。凭借这些 特性，此器件非常适合用于各种汽车应用的 电源。

器件信息(1)

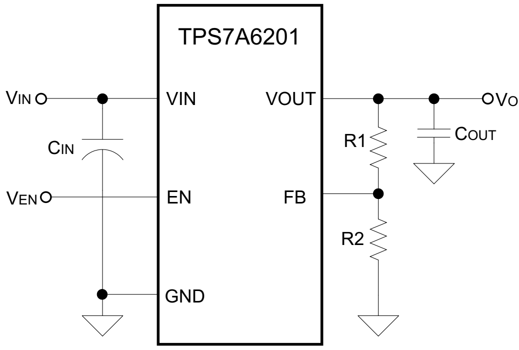
器件型号	封装	封装尺寸（标称值）
TPS7A6201-Q1	TO-263 (5)	10.16mm × 8.42mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型稳压器稳定性



应用原理图



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision D (May 2018) to Revision E	**Page**
• 已更改 将 AEC-Q100 *特性* 项目符号更改为符合新标准	1
• 已更改 将整个文档中的输入电压范围从 11V 更改为 7V	1
• 已更改 *更改了应用* 部分	1
• Added footnote to V_{IN} row in *Recommended Operating Conditions* table	4
• Added footnote to V_{IN} row in *Electrical Characteristics* table	4
• Deleted *Dissipation Ratings* table	5

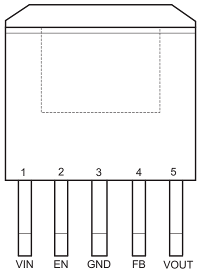
Changes from Revision C (July 2016) to Revision D	**Page**
• 已更改 将 4V 更改为 11V（位于第四个*特性* 项目符号）	1
• 已更改 将*可编程* 变更为*可调节*（位于*输出电压 特性* 项目符号）	1
• Changed V_{IN}, V_{EN} parameter row in *Recommended Operating Conditions* table: separated V_{IN} and V_{EN} into different rows, changed V_{IN} minimum specification from 4 V to 11 V	4
• Changed V_{IN} parameter minimum specification from 4 V to 11 V in *Electrical Characteristics* table	4
• Changed 4 V to 11 V in *Input voltage range* row of *Design Parameters* table	14
• Changed 4 V to 11 V in first sentence of *Power Supply Recommendations* section	15

Changes from Revision B (March 2012) to Revision C	**Page**
• 添加了 *ESD 额定值* 表、*特性 说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分	1
• 删除了*订购信息* 表，请参阅数据表末尾的 POA	1
• Changed *Thermal Information* table	4

Changes from Revision A (December 2011) to Revision B	**Page**
• Added value to test conditions field in Regulated Output Voltage 6.1 (I_{OUT} = 10 mA to 300 mA, V_{IN}= V_{OUT} + 1 V to 16 V)	4

5 Pin Configuration and Functions

KTT Package
5-Pin TO-263
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VIN	I	Input voltage pin: The unregulated input voltage is supplied to this pin. A bypass capacitor shall be connected between VIN pin and GND pin to dampen input line transients.
2	EN	I	Enable pin: This is a high voltage tolerant input pin with an internal pulldown. A high input to this pin activates the device and turns the regulator ON. This input can be connected to VIN terminal for self bias applications. If this pin is not connected, the device stays disabled.
3	GND	I/O	Ground pin: This is signal ground pin of the IC.
4	FB	I	Feedback pin: This pin is used to connect external resistors to ground to program the output voltage.
5	VOUT	O	Regulated output voltage pin: This is a regulated output voltage pin with a limitation on maximum output current. An external resistor divider is connected at this pin to program the output voltage. To achieve stable operation and prevent oscillation, an external output capacitor (C_{OUT}) with low ESR shall be connected between this pin and GND pin.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}, V_{EN}	Unregulated inputs(2)	–0.3	45	V
V_{OUT}	Regulated output		7	V
V_{FB}	Feedback voltage	–0.3	7	V
T_{OP}	Operating ambient temperature	–40	125	°C
T_{LEAD}	Lead temperature (soldering, 10 s)		260	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to GND.
(2) Absolute maximum voltage for duration less than 480 ms.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)(2)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) Tested in accordance with JEDEC Standard 22, Test Method A114-A (100-pF capacitor discharged through a 1.5-kΩ resistor into each pin).

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{IN}	Unregulated input voltage	7 (1)	40	V
V_{EN}	Enable pin voltage	4	40	V
T_J	Operating junction temperature	–40	150	°C

(1) V_{IN} can go down to 4 V for 130 ms or less and remain functional. If V_{IN} is less than 7 V for longer than 130 ms, then some devices may turn off until the input voltage rises above 7 V.

6.4 Thermal Information

THERMAL METRIC (1)			TPS7A6201-Q1 KTT (TO-263) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	High-K (2)	30.2	°C/W
		Low-K (3)	34.4	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		38.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		7.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter		3.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter		7.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		1.5	°C/W
θ_{JP}	Thermal impedance junction to exposed pad KTT (D2PAK) package		10.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The thermal data is based on JEDEC standard high K profile – JESD 51-5. The copper pad is soldered to the thermal land pattern. Also correct attachment procedure must be incorporated.
(3) The thermal data is based on JEDEC standard low K profile – JESD 51-3. The copper pad is soldered to the thermal land pattern. Also correct attachment procedure must be incorporated.

6.5 Electrical Characteristics

V_{IN} = 14 V, T_J = –40ºC to 150ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE (VIN PIN)						
V_{IN}	Input voltage		7 (1)		40	V
$I_{QUIESCENT}$	Quiescent current	V_{IN} = 8.2 V to 18 V, V_{EN} = 5 V, I_{OUT} = 0.01 mA to 0.75 mA		25	40	µA
I_{SLEEP}	Sleep/shutdown current	V_{IN} = 8.2 V to 18 V, V_{EN} < 0.8 V, I_{OUT} = 0 mA (no load), T_A = 125°C			3	µA
$V_{IN-UVLO}$	Undervoltage lockout voltage	Ramp V_{IN} down until output is turned OFF		3.16		V
$V_{IN(POWERUP)}$	Power-up voltage	Ramp V_{IN} up until output is turned ON		3.45		V
ENABLE INPUT (EN PIN)						
V_{IL}	Logic input low level		0		0.8	V
V_{IH}	Logic input high level		2.5		40	V
REGULATED OUTPUT VOLTAGE (VOUT PIN)						
V_{REF}	Internal Reference Voltage	I_{OUT} = 10 mA to 300 mA, V_{IN}= V_{OUT} + 1 V to 16 V	–2%		2%	
$\Delta V_{LINE-REG}$	Line regulation	V_{IN} = 6 V to 28 V, I_{OUT} = 10 mA, V_{OUT} = 7 V			15	mV
		[V_{IN} = 6 V to 28 V, I_{OUT} = 10 mA, V_{OUT} = 3.3 V] (2)			20	
$\Delta V_{LOAD-REG}$	Load regulation	I_{OUT} = 10 mA to 300 mA, V_{IN}= 14 V, V_{OUT} = 7 V			25	mV
		[I_{OUT} = 10 mA to 300 mA,V_{IN} = 14 V, V_{OUT} = 3.3 V] (2)			35	

(1) V_{IN} can go down to 4 V for 130 ms or less and remain functional. If V_{IN} is less than 7 V for longer than 130 ms, then some devices may turn off until the input voltage rises above 7 V.
(2) Specified by design – not tested.

Electrical Characteristics (continued)

V_{IN} = 14 V, T_J = –40ºC to 150ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DROPOUT}$ (3)	Dropout voltage (V_{IN} – V_{OUT})	I_{OUT} = 250 mA			500	mV
		I_{OUT} = 150 mA			300	
R_{SW} (2)	Switch resistance	VIN to VOUT resistance			2	Ω
I_{OUT}	Output current	V_{OUT} in regulation	0		300	mA
I_{CL}	Output current limit	V_{OUT} = 0 V (VOUT pin is shorted to ground)	350		1000	mA
PSRR (2)	Power supply ripple rejection	$V_{IN\text{-}RIPPLE}$ = 0.5 Vpp, I_{OUT} = 300 mA, frequency = 100 Hz, V_{OUT} = 5 V and V_{OUT} = 3.3 V		60		dB
		$V_{IN\text{-}RIPPLE}$ = 0.5 Vpp, I_{OUT} = 300 mA, frequency = 150 kHz, V_{OUT} = 5 V and V_{OUT} = 3.3 V		30		
OPERATING TEMPERATURE RANGE						
T_J	Operating junction temperature		–40		150	ºC
$T_{SHUTDOWN}$	Thermal shutdown trip point			165		ºC
T_{HYST}	Thermal shutdown hysteresis			10		ºC

(3) This test is done with V_{OUT} is in regulation and V_{IN} – V_{OUT} parameter is measured when V_{OUT} (programmed output voltage, for example, 5 V or 3.3 V) drops by 100 mV at specified loads.

6.6 Typical Characteristics

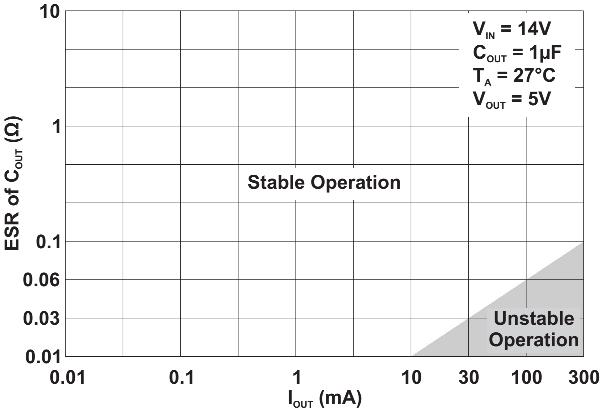


Figure 1. ESR vs Load Current

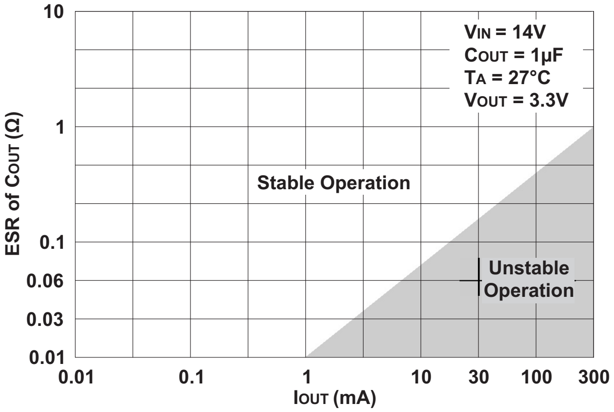


Figure 2. ESR vs Load Current

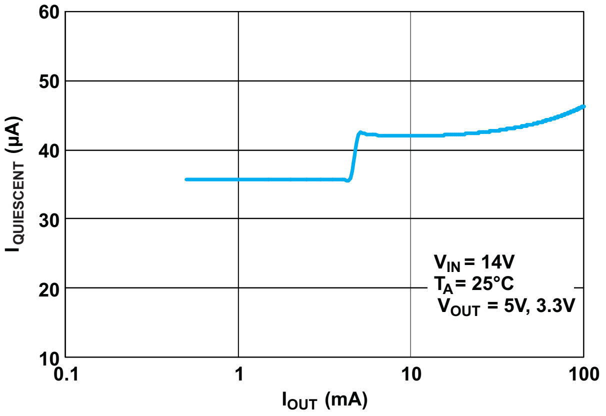


Figure 3. Quiescent Current vs Load Current

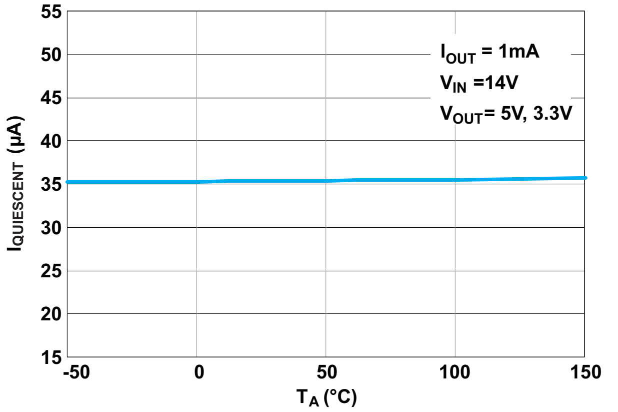


Figure 4. Quiescent Current vs Ambient Air Temperature

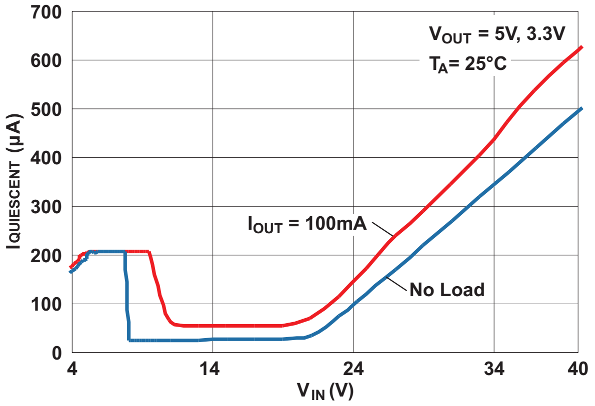
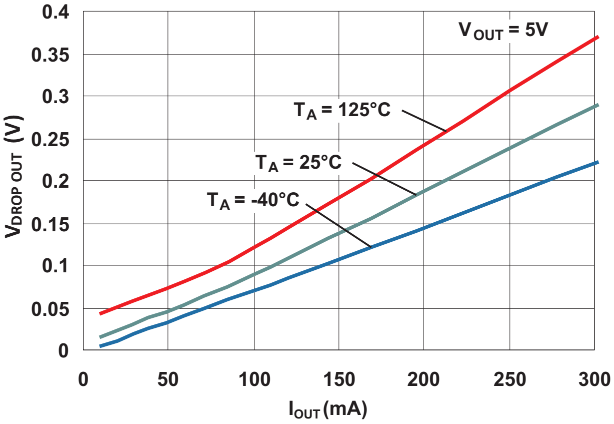


Figure 5. Quiescent Current vs Input Voltage



Dropout voltage is measured when the output voltage drops by 100 mV from the regulated output voltage level. (For example, if output voltage is programmed to be 5 V, the dropout voltage is measured when the output voltage drops down to 4.9 V from 5 V.)

Figure 6. Drop Out Voltage vs Load Current

Typical Characteristics (continued)

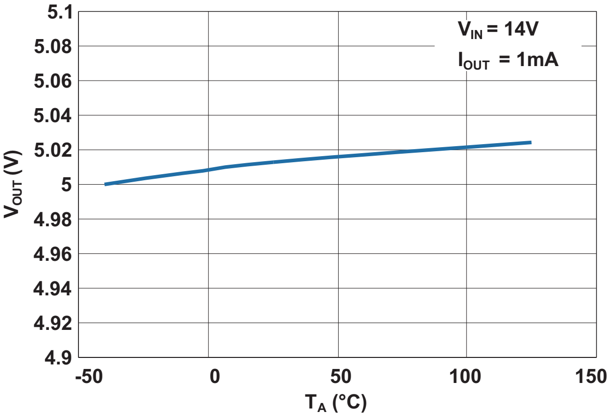


Figure 7. Output Voltage vs Ambient Air Temperature (V_{OUT} Programmed to 5 V)

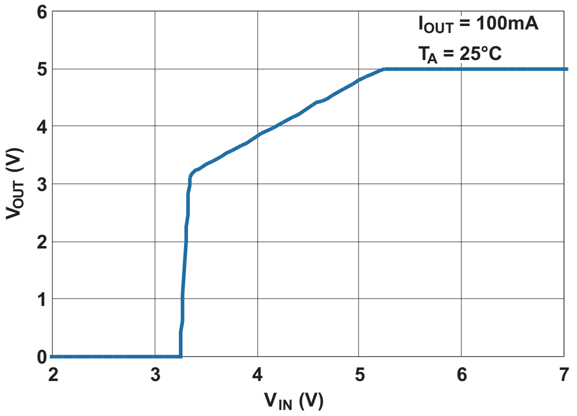


Figure 8. Output Voltage vs Input Voltage (V_{OUT} Programmed to 5 V)

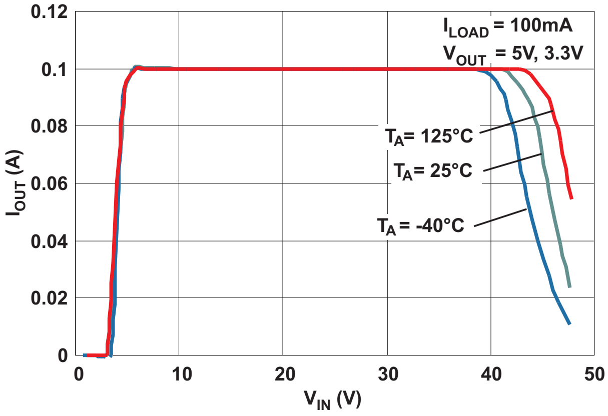


Figure 9. Output Current vs Input Voltage

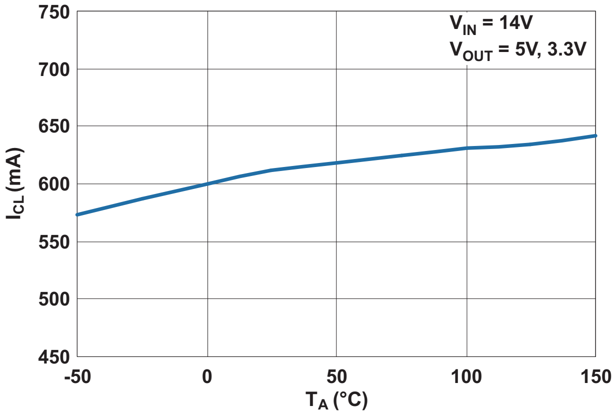


Figure 10. Output Current Limit vs Ambient Air Temperature

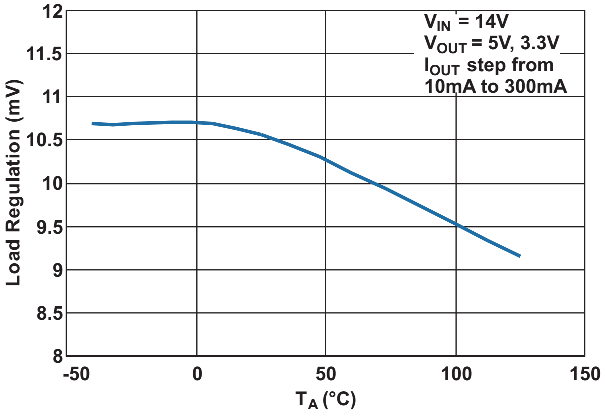


Figure 11. Load Regulation vs Ambient Air Temperature

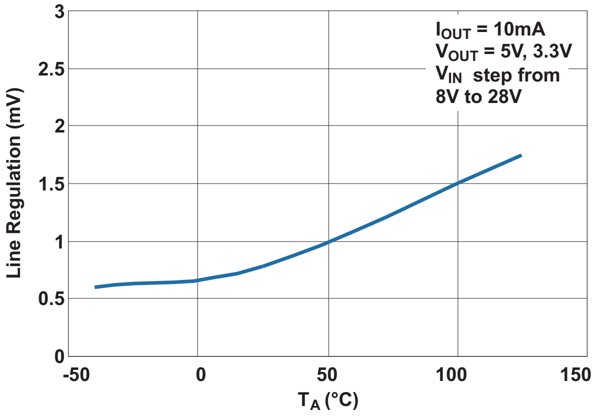


Figure 12. Line Regulation vs Ambient Air Temperature

Typical Characteristics (continued)

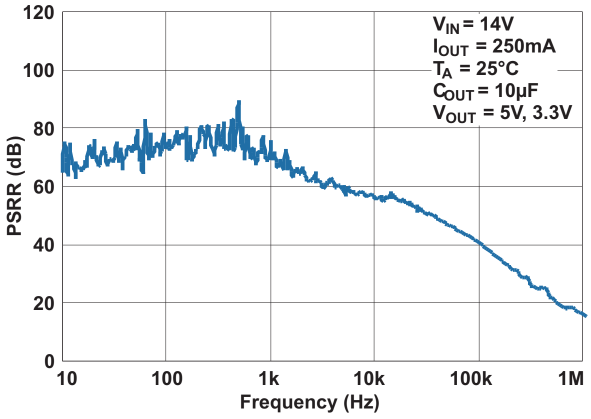


Figure 13. PSRR at Heavy Load Current

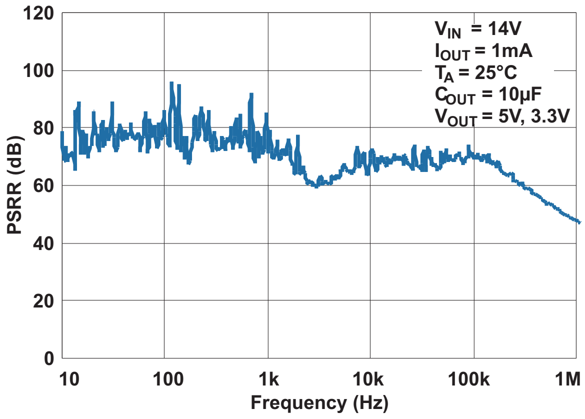


Figure 14. PSRR at Light Load Current

7 Detailed Description

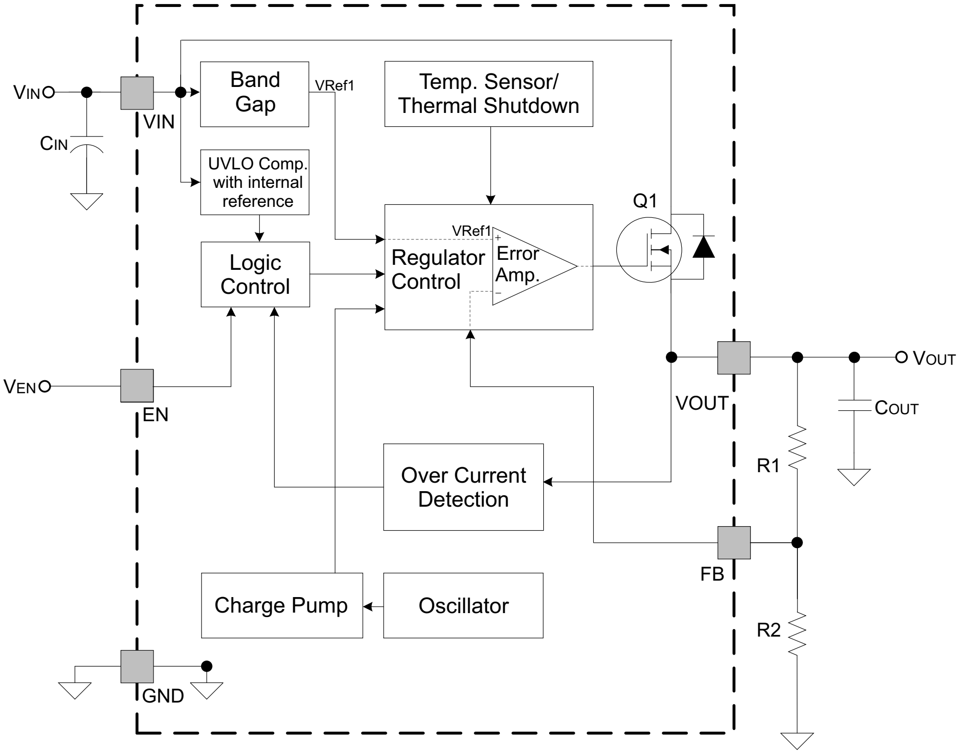
7.1 Overview

The TPS7A6201-Q1 device is a monolithic, low-dropout linear voltage regulator with programmable output voltage and integrated fault protection. This voltage regulator is designed for low power consumption and quiescent current less than 25 µA in light-load applications.

This device is available in the 5-pin package option TO-263 (D2PAK/TO-263).

The following section describes the features of TPS7A6201-Q1 voltage regulator in detail.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power Up

During power up, the regulator incorporates a protection scheme to limit the current through pass element and output capacitor. When the input voltage exceeds a certain threshold ($VIN_{(POWERUP)}$) level, the output voltage begins to ramp up as shown in Figure 15.

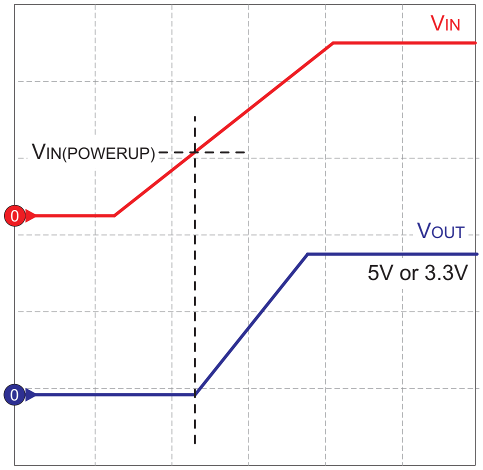


Figure 15. Power-Up Operation

7.3.2 Adjustable Output Voltage

The regulated output voltage (V_{OUT}) can be programmed by connecting external resistors to FB pin. Calculate the feedback resistor values using Equation 1.

$$V_{OUT} = V_{REF}\left[1 + \frac{R1}{R2}\right]$$

where

- V_{OUT} = desired output voltage
- V_{REF} = reference voltage (V_{REF} = 1.23 V typically)
- R1, R2 = feedback resistors (see the *Functional Block Diagram*) (1)

The overall tolerance of the regulated output voltage depends on the tolerance of internal reference voltage and external feedback resistors, and is given by Equation 2.

$$tol_{V_{OUT}} = tol_{V_{REF}} + \left[\frac{R1}{R1 + R2}\right]\left[tol_{R1} + tol_{R2}\right]$$

where

- tol_{VOUT} = tolerance of output voltage
- tol_{VREF} = tolerance of internal reference voltage (tol_{VREF} = ±1.5% typically)
- tol_{R1},tol_{R2} = tolerance of feedback resistors R1, R2 (2)

For a tighter tolerance on V_{OUT}, select lower-value feedback resistors. TI recommends selecting feedback resistors such that the sum of R1 and R2 is between 20 kΩ and 200 kΩ.

7.3.3 Enable Input

This device has a high-voltage-tolerant EN pin that can be used to enable and disable a device from an external microcontroller or a digital control circuit. A high input to this pin activates the device and turns the regulator on. This input can also be connected to V_{IN} terminal for self bias applications. An internal pulldown resistor is connected to this pin; therefore, if this pin is left unconnected, the device stays disabled.

Feature Description (continued)

7.3.4 Charge Pump Operation

This device has an internal charge pump which turns on or off depending on the input voltage and the output current. The charge pump switching circuitry shall not cause conducted emissions to exceed required thresholds on the input voltage line. For a given output current, the charge pump stays on at lower input voltages and turns off at higher input voltages. The charge pump switching thresholds are hysteretic. Figure 16 and Figure 17 shows typical switching thresholds for the charge pump at light (I_{OUT} < ~2 mA) and heavy (I_{OUT} > ~2 mA) loads respectively.

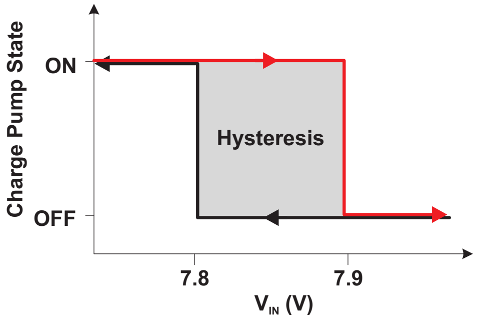


Figure 16. Charge Pump Operation at Light Loads

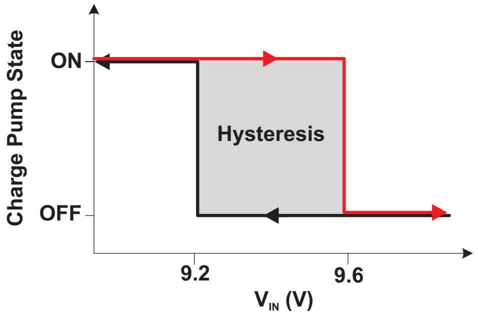


Figure 17. Charge Pump Operation at Heavy Loads

7.3.5 Undervoltage Shutdown

This device has an integrated undervoltage lockout (UVLO) circuit to shut down the output if the input voltage (V_{IN}) falls below an internally fixed UVLO threshold level ($V_{IN\text{-}UVLO}$); see Figure 18. This ensures that the regulator is not latched into an unknown state during low input voltage conditions. The regulator normally powers up when the input voltage exceeds the $V_{IN(POWERUP)}$ threshold.

7.3.6 Low Voltage Tracking

At low-input voltages, the regulator drops out of regulation, and the output voltage tracks input minus a voltage based on the load current and switch resistance (see Figure 18). This allows for a smaller input capacitor and can possibly eliminate the need of using a boost convertor during cold crank conditions.

Feature Description (continued)

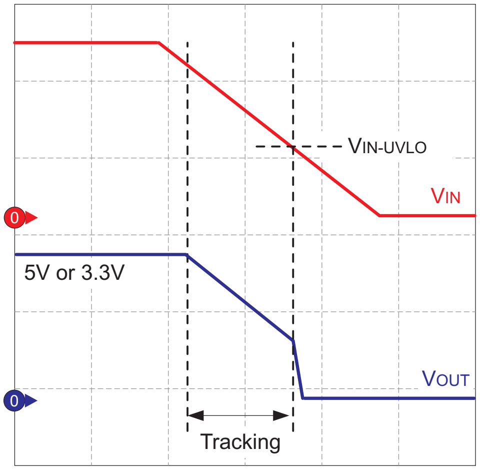


Figure 18. Low Voltage Tracking Operation

7.3.7 Integrated Fault Protection

The device features integrated fault protection, making it ideal for use in automotive applications. To keep the device in safe area of operation during certain fault conditions, internal current-limit protection and current-limit foldback are used to limit the maximum output current. This protects the device from excessive power dissipation. For example, during a short-circuit condition on the output, current through the pass element is limited to I_{CL} to protect the device from excessive power dissipation.

7.3.8 Thermal Shutdown

The device incorporates a thermal shutdown (TSD) circuit as protection from overheating. For continuous normal operation, the junction temperature must not exceed the TSD trip point. If the junction temperature exceeds the TSD trip point, the output is turned off. When the junction temperature falls below TSD trip point, the output is turned on again, as shown in Figure 19.

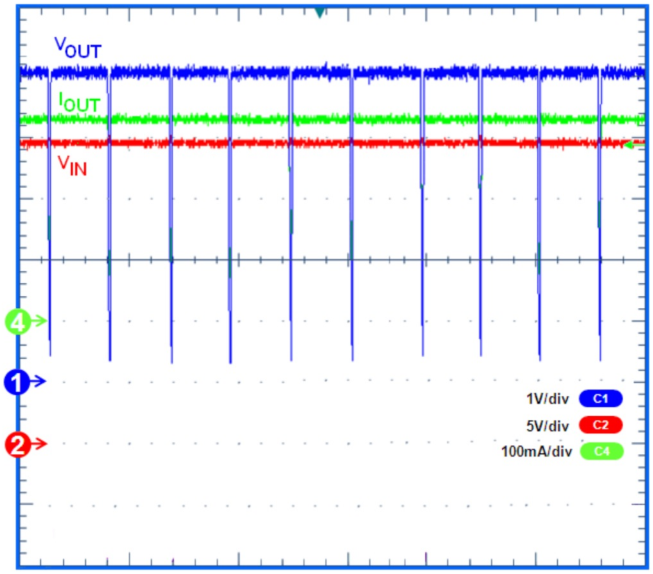


Figure 19. Thermal Cycling Waveform for TPS7A6201-Q1 (V_{IN} = 24 V, I_{OUT} = 300 mA, V_{OUT} = 5 V)

7.4 Device Functional Modes

7.4.1 Low Power Mode

At light loads and high-input voltages (V_{IN}> approximately 8 V such that charge pump is off) the device operates in low power mode, and the quiescent current consumption is reduced to 25 µA (typical) as shown in Table 1.

Table 1. Typical Quiescent Current Consumption

I_{OUT}	CHARGE PUMP ON	CHARGE PUMP OFF
I_{OUT} < approximately 2 mA (Light load)	250 µA	25 µA (Low Power Mode)
I_{OUT} > approximately 2 mA (Heavy load)	280 µA	70 µA

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS7A6201-Q1 is a low-dropout linear voltage regulator designed for low power consumption and quiescent current less than 25 µA in light-load applications.

8.2 Typical Application

Figure 20 shows the typical application circuit for the TPS7A6201-Q1 device. Depending upon an end application, different values of external components may be used. To program the output voltage, feedback resistors (R1 and R2) must be carefully selected. Using small resistors results in higher current consumption, whereas, using very large resistors impacts the sensitivity of the regulator. Therefore, TI recommends selecting feedback resistors such that the sum of R1 and R2 is between 20 kΩ and 200 kΩ. Also, the overall tolerance of the regulated output voltage depends on the tolerance of the internal reference voltage and external feedback resistors.

A larger output capacitor may be required during fast load steps to prevent output from temporarily dropping down. TI recommends a low-ESR ceramic capacitor with a dielectric of type X5R or X7R. Additionally, a bypass capacitor can be connected at the output to decouple high-frequency noise as per the end application.

Example: If the desired regulated output voltage is 5 V, upon selecting R2, R1 can be calculated using Equation 1 (and vice versa). Knowing V_{REF} = 1.23 V (typical), V_{OUT} = 5 V, and selecting R2 = 20 kΩ, R1 is calculated to be 61.3 kΩ.

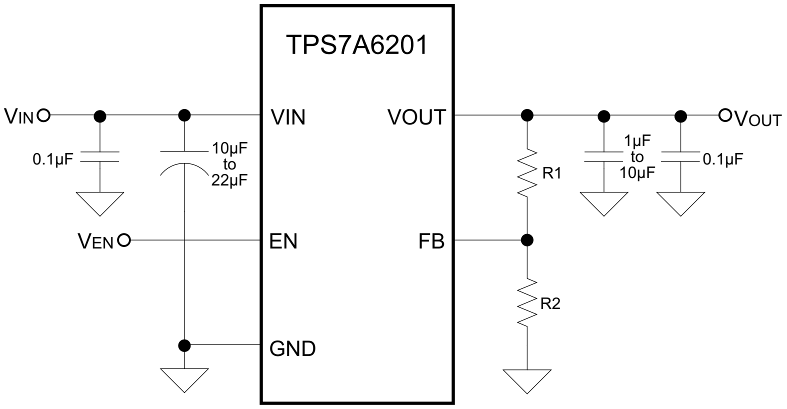


Figure 20. Typical Application Schematic for TPS7A6201-Q1

8.2.1 Design Requirements

Table 2 lists the design parameters for this example.

Table 2. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range	7 V to 40 V
Output voltage	5 V
Output current rating	200 mA
Output capacitor range	10 µF to 47 µF
Output capacitor ESR range	10 mΩ to 10 Ω

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Output current rating
- Input capacitor
- Output capacitor

8.2.2.1 Input Capacitor

The device requires an input bypass capacitor, the value of which depends on the application. The typical recommended value for the bypass capacitor is 10 µF. The voltage rating must be greater than the maximum input voltage.

8.2.2.2 *Output Capacitor*

The device requires an output capacitor to stabilize the output voltage. TI recommends selecting a capacitor between 10 µF and 47 µF with ESR range from 10 mΩ to 10 Ω.

8.2.2.3 *Feedback Resistor*

The regulated output voltage (VOUT) can be programmed by connecting external resistors to FB pin. Calculate the feedback resistor values using Equation 1 (R1 = 61.3K Ω, R2 = 20 K Ω).

8.2.3 Application Curve

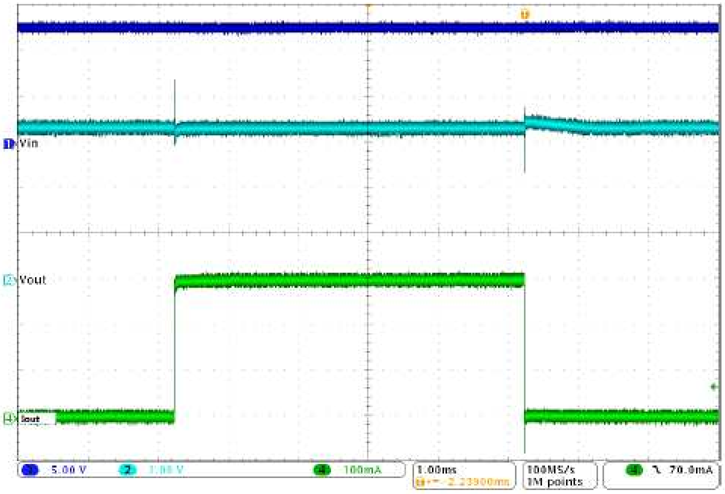


Figure 21. Load Transient Waveform

9 Power Supply Recommendations

Design of the device is for operation from an input voltage supply with a range from 7 V to 40 V. This input supply must be well regulated. If the input supply is located more than a few inches from the device, TI recommends adding an electrolytic capacitor with a value of 22 µF and a ceramic bypass capacitor at the input.

10 Layout

10.1 Layout Guidelines

For the LDO power supply, especially these high voltage and large current ones, layout is an important step. If layout is not carefully designed, the regulator could not deliver enough output current because of the thermal limitation. To improve the thermal performance of the device, and maximize the current output at high ambient temperature, TI recommends spreading the thermal pad as large as possible and place enough thermal vias on the thermal pad. Figure 25 provides an example layout.

10.1.1 Power Dissipation and Thermal Considerations

Calculate the power dissipated in the device using Equation 3.

$P_D = I_{OUT} \times (V_{IN} – V_{OUT)}) + I_{QUIESCENT} \times V_{IN}$

where

- P_D = continuous power dissipation
- I_{OUT} = output current
- V_{IN} = input voltage
- V_{OUT} = output voltage
- $I_{QUIESCENT}$ = quiescent current (3)

As $I_{QUIESCENT} << I_{OUT}$, therefore, the term $I_{QUIESCENT} \times V_{IN}$ in Equation 3 can be ignored.

For device under operation at a given ambient air temperature (T_A), calculate the junction temperature (T_J) Equation 4.

$T_J = T_A + (R_{\theta JA} \times P_D)$

where

- $R_{\theta JA}$ = junction to ambient air thermal impedance (4)

Calculate the rise in junction temperature due to power dissipation using Equation 5.

$$\Delta T = T_J – T_A = (R_{\theta JA} \times P_D) \quad (5)$$

For a given maximum junction temperature ($T_{J\text{-Max}}$), calculate the maximum ambient air temperature ($T_{A\text{-Max}}$) at which the device can operate using Equation 6.

$$T_{A\text{-Max}} = T_{J\text{-Max}} – (R_{\theta JA} \times P_D) \quad (6)$$

Example

If I_{OUT} = 100 mA, V_{OUT} = 5 V, V_{IN} = 14 V, $I_{QUIESCENT}$ = 250 µA, and $R_{\theta JA}$ = 30˚C/W, the continuous power dissipated in the device is 0.9 W. The rise in junction temperature due to power dissipation is 27˚C. For a maximum junction temperature of 150˚C, maximum ambient air temperature at which the device can operate is 123˚C.

For adequate heat dissipation, TI recommends soldering the thermal pad (exposed heat sink) to thermal land pad on the PCB. Doing this provides a heat conduction path from die to the PCB and reduces overall package thermal resistance. Figure 22 illustrates the power derating curves for the TPS7A6201-Q1 device in the KTT (TO-263) package..

Layout Guidelines (continued)

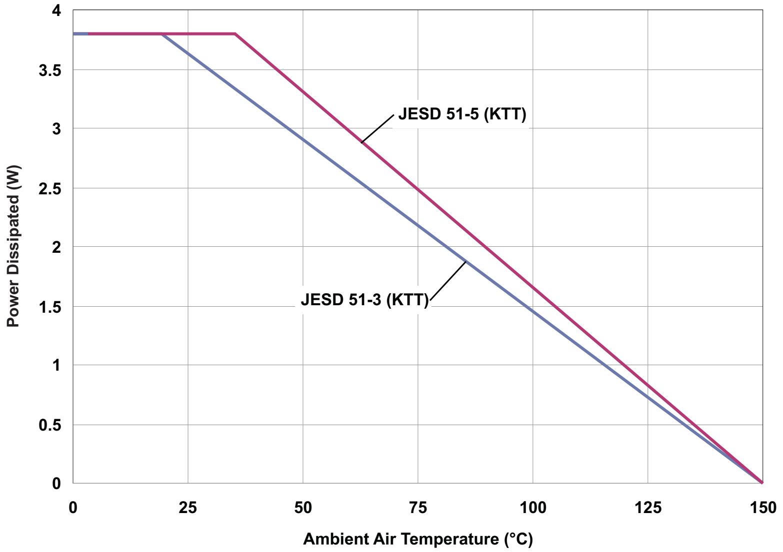
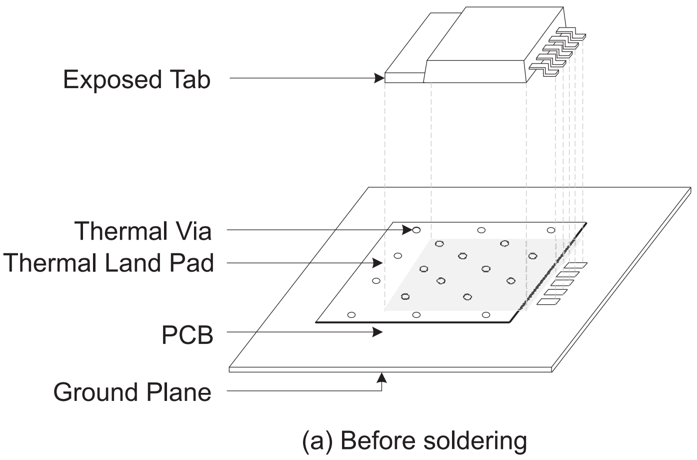
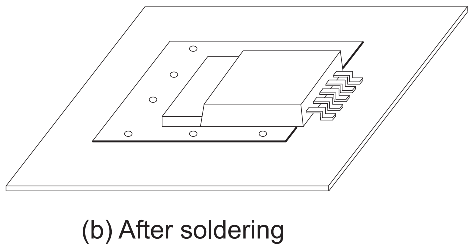


Figure 22. Power Derating Curves

For optimum thermal performance, TI recommends using a high-K PCB with thermal vias between ground plane and solder pad or thermal land pad. This is shown in Figure 23 (a) and (b). Furthermore, heat spreading capabilities of a PCB can be considerably improved by using a thicker ground plane and a thermal land pad with a larger surface area.



(a) Before soldering



(b) After soldering

Figure 23. Using Multilayer PCB and Thermal Vias for Adequate Heat Dissipation

Layout Guidelines (continued)

Keeping other factors constant, surface area of the thermal land pad contributes to heat dissipation only to a certain extent. Figure 24 shows a variation of $R_{\theta JA}$ with surface area of the thermal land pad (soldered to the exposed pad) for KTT package.

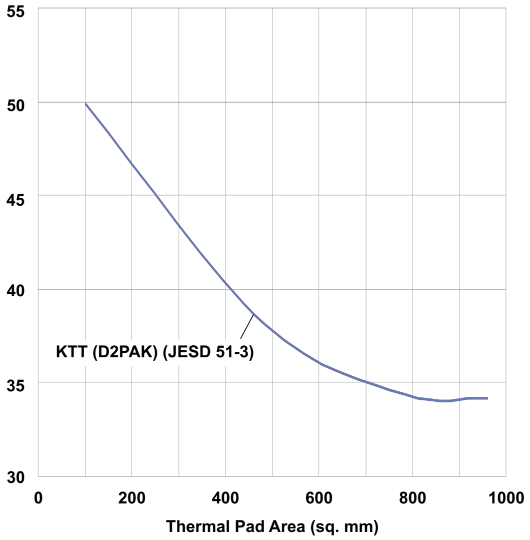


Figure 24. $R_{\theta JA}$ vs Thermal Pad Area

10.2 Layout Example

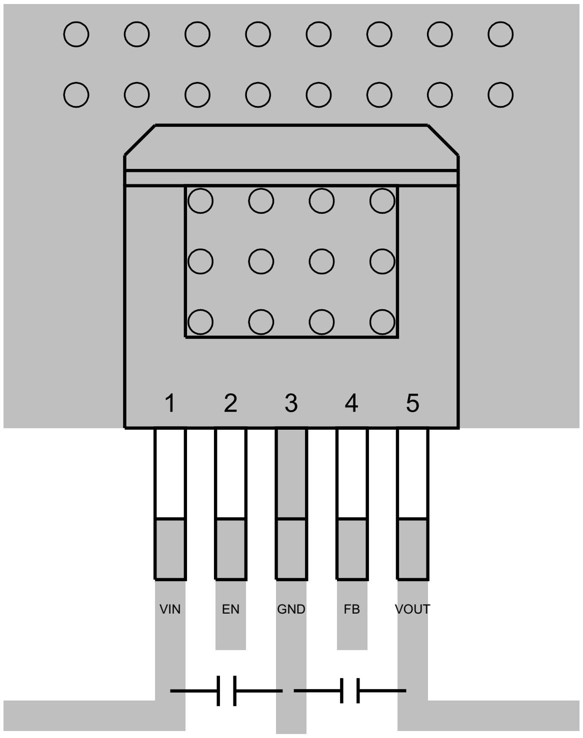


Figure 25. Layout Recommendation

11 器件和文档支持

11.1 接收文档更新通知

如需接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.2 社区资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.3 商标

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11.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

重要声明和免责声明

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PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A6201QKTTRQ1	ACTIVE	DDPAK/ TO-263	KTT	5	500	RoHS & Green	SN	Level-3-245C-168 HR	-40 to 125	7A6201Q1	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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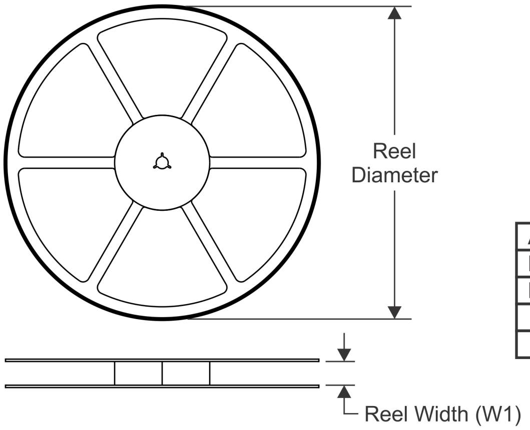
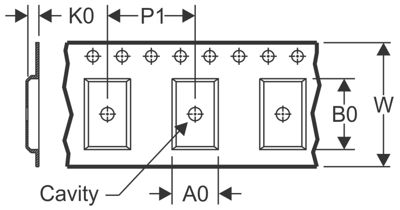
TAPE AND REEL INFORMATION

REEL DIMENSIONS

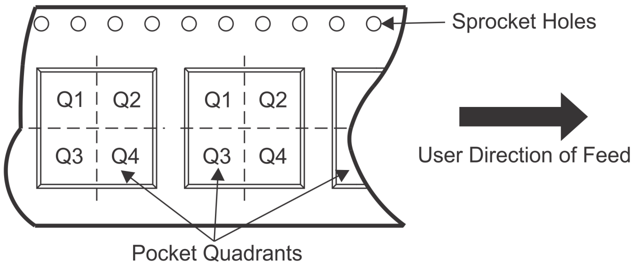


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

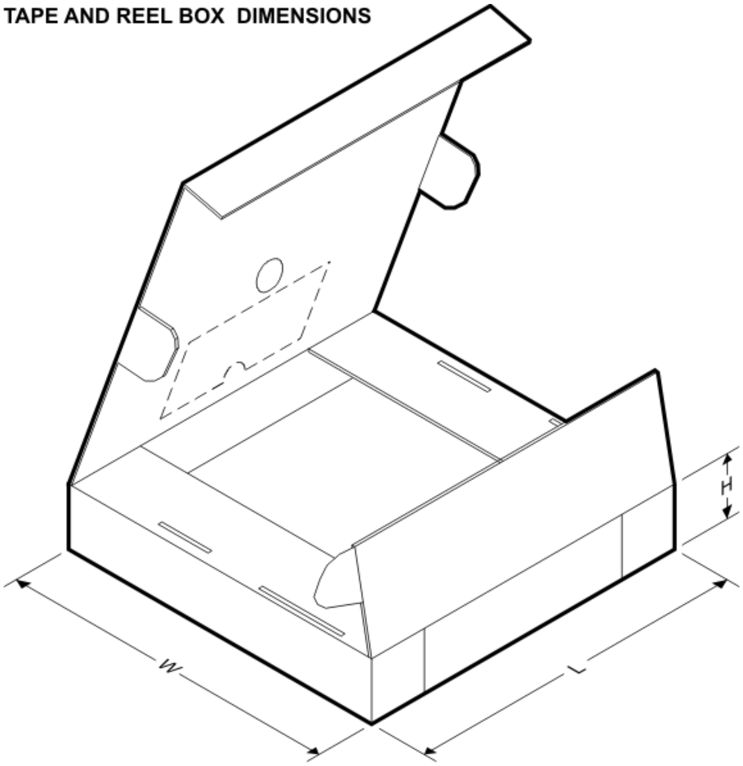
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A6201QKTTRQ1	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.8	4.9	16.0	24.0	Q2

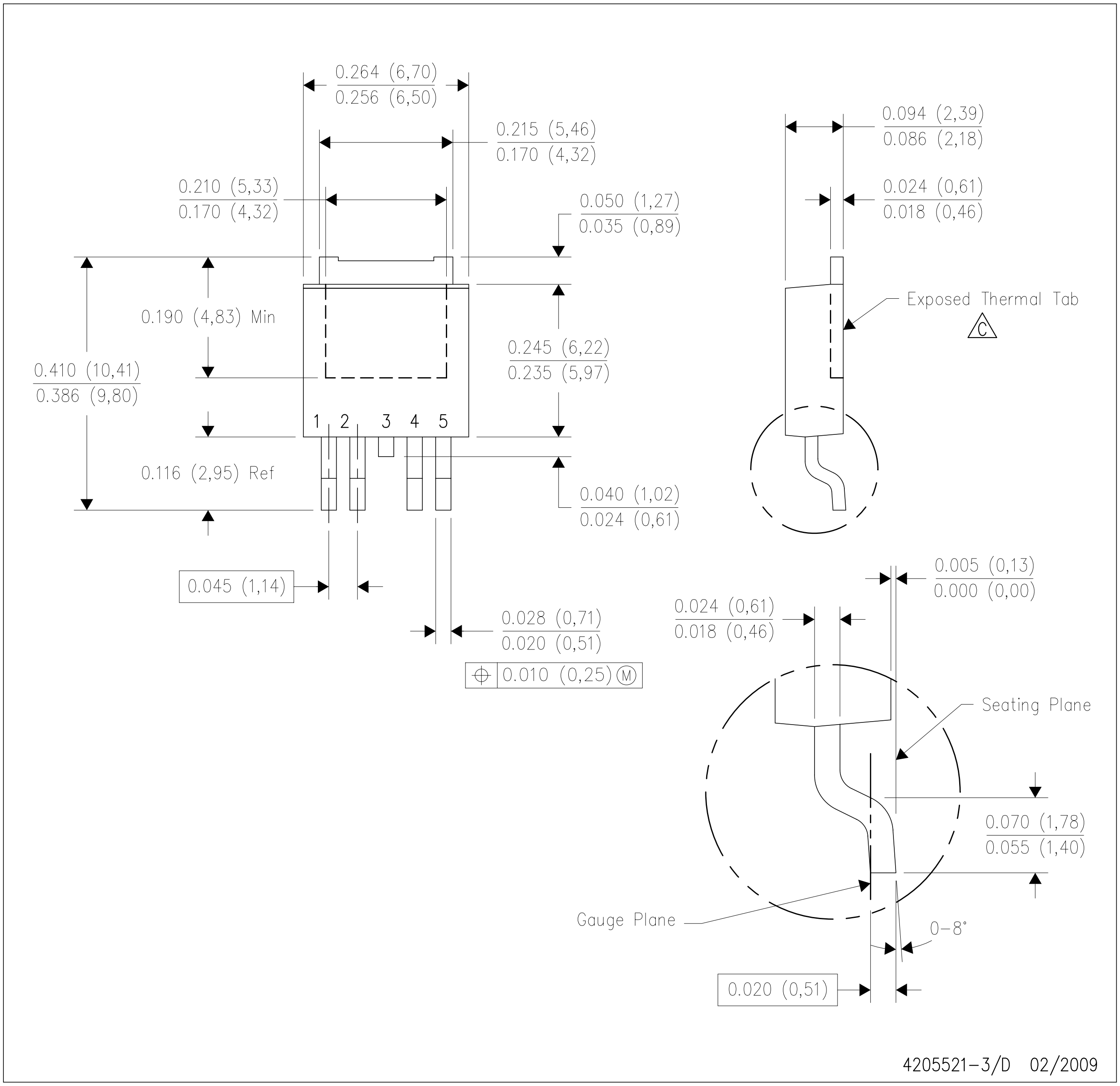
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

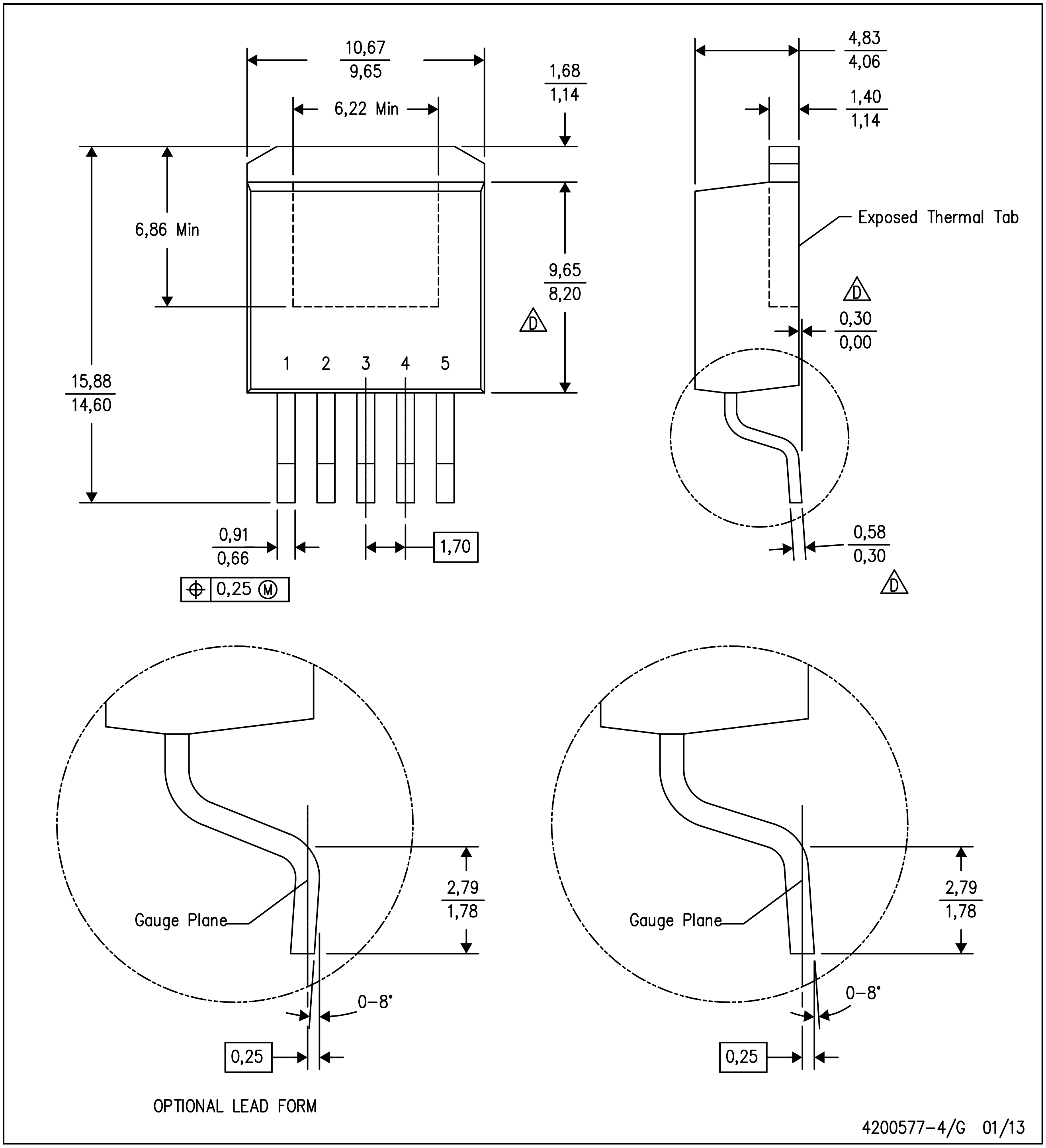
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A6201QKTTRQ1	DDPAK/TO-263	KTT	5	500	340.0	340.0	38.0

KVU (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



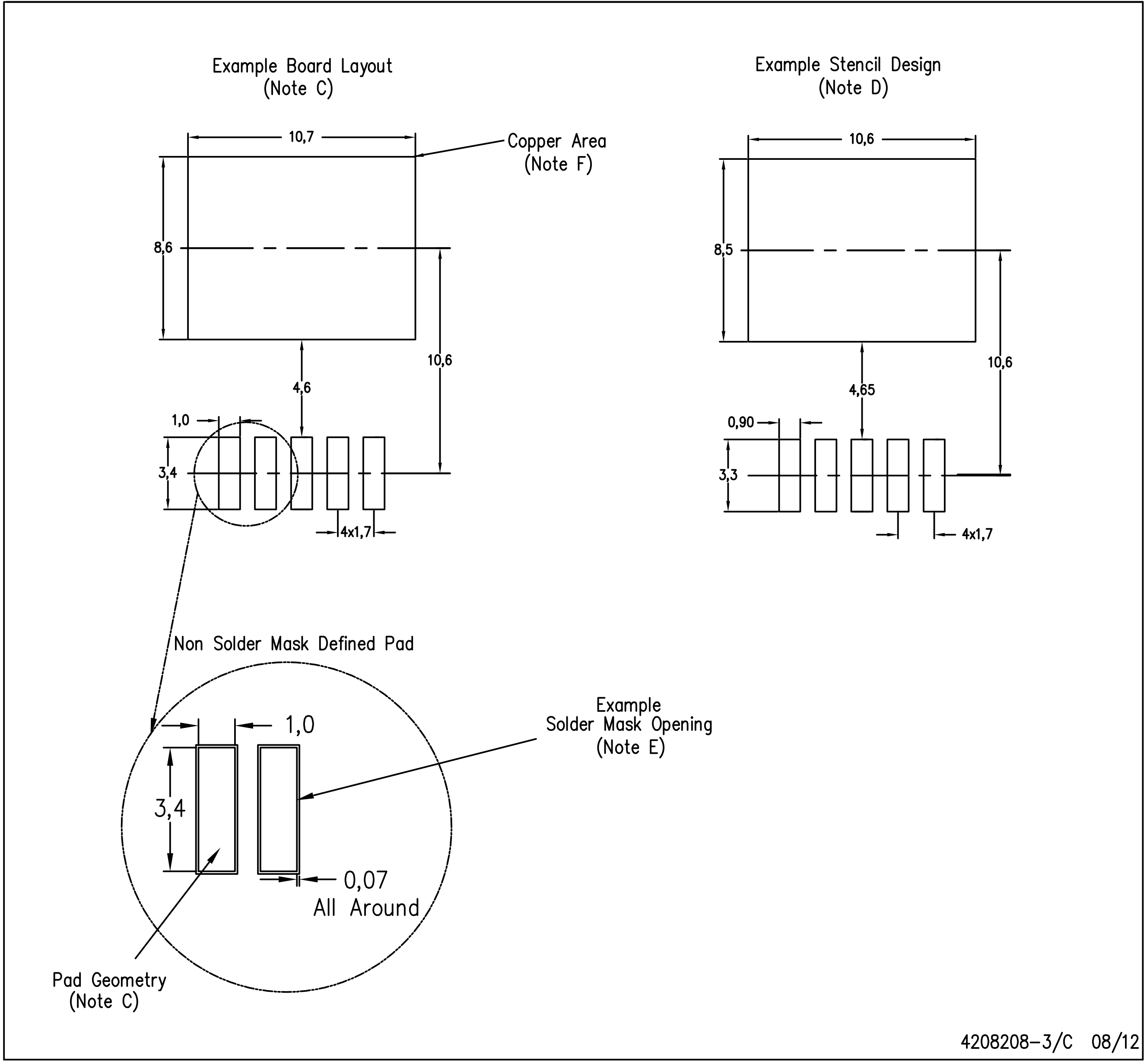
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C△ The center lead is in electrical contact with the exposed thermal tab.
- D. Body Dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.006 (0,15) per side.
- E. Falls within JEDEC TO–252 variation AD.

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
- D. Falls within JEDEC TO–263 variation BA, except minimum lead thickness, maximum seating height, and minimum body length.

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–SM–782 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
- F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

重要声明和免责声明

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