TSB81BA3E IEEE 1394b Three-Port Cable Transceiver/Arbiter

1 Features

- Fully Supports Provisions of IEEE P1394b Revision 1.33+ at 1-Gigabit Signaling Rates
- Fully Supports Provisions of IEEE 1394a-2000 and 1394-1995 Standard for High Performance Serial Bus
- Fully Interoperable With Firewire, i.LINK, and SB1394™, Implementation of IEEE Std 1394
- Provides Three Fully Backward Compatible, (1394a-2000 Fully Compliant) Bilingual P1394b Cable Ports at up to 800 Megabits per Second (Mbits/s)
- Provides Three 1394a-2000 Fully Compliant Cable Ports at 100/200/400 Mbits/s
- Full 1394a-2000 Support Includes:
  - Connection Debounce
  - Arbitrated Short Reset
  - Multispeed Concatenation
  - Arbitration Acceleration
  - Fly-By Concatenation
  - Port Disable/Suspend/Resume
  - Extended Resume Signaling for Compatibility With Legacy DV Devices
- Power-Down Features to Conserve Energy in Battery Powered Applications
- Low-Power Sleep Mode
- Fully Compliant With Open Host Controller Interface (HCI) Requirements
- Cable Power Presence Monitoring
- Cable Ports Monitor Line Conditions for Active Connection to Remote Node
- Register Bits Give Software Control of Contender Bit, Power Class Bits, Link Active Control Bit, and 1394a-2000 Features
- Data Interface to Link-Layer Controller Pin Selectable From 1394a-2000 Mode (2/4/8 Parallel Bits at 49.152 MHz) or 1394b Mode (8 Parallel Bits at 98.304 MHz)
- Interface to Link-Layer Controller Supports Low Cost TI Bus-Holder Isolation
- Interoperable With Link-Layer Controllers Using 3.3-V Supplies
- Interoperable With Other 1394 Physical Layers (PHYs) Using 1.8-V, 3.3-V, and 5-V Supplies
- Low Jitter, External Crystal Oscillator Provides Transmit and Receive Data at 100/200/400/800 Mbits/s, and Link-Layer Controller Clock at 49.152 MHz and 98.304 MHz
- Separate Bias (TPBIAS) for Each Port
- Low Cost, High Performance 80-Pin TQFP (PFP) Thermally Enhanced Package and 168-Pin ZAJ (BGA) Package
- Software Device Reset (SWR)
- Fail-Safe Circuitry Senses Sudden Loss of Power to the Device and Disables the Ports to Ensure That the TSB81BA3E Does Not Load the TPBIAS of Any Connected Device and Blocks any Leakage From the Port Back to Power Plane
- The TSB81BA3E Has a 1394a-2000 Compliant Common-Mode Noise Filter on the Incoming Bias Detect Circuit to Filter Out Cross-Talk Noise
- The TSB81BA3E Is Port Programmable to Force 1394a Mode to Allow Use of 1394a Connectors (1394b Signaling Must Not Be Put Across 1394a Connectors or Cables)
- Internal Voltage Regulator Option

2 Description

The TSB81BA3E provides the digital and analog transceiver functions needed to implement a three-port node in a cable-based IEEE 1394 network. Each cable port incorporates two differential line transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for packet reception and transmission. The TSB81BA3E is designed to interface with a link-layer controller (LLC), such as the TSB82AA2, TSB12LV21, TSB12LV26, TSB12LV32, TSB42AA4, TSB42AB4, TSB12LV01B, or TSB12LV01C. It also may be connected cable port to cable port to an integrated 1394 Link + PHY layer such as the TSB43AB2.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TSB81BA3E	HTQFP (80)	12.00 mm x 12.00 mm
	NFBGA (167)	12.00 mm x 12.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

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3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (October 2015) to Revision C **Page**

- Changed the ADDRESS column of Table 8 ... 27
- Changed the ADDRESS column of Table 10 ... 27

Changes from Revision A (May 2010) to Revision B **Page**

- Added *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Replaced the *Dissipation Ratings* with the *Thermal Information* ... 10
- Changed the Address column of Table 6 ... 24

Changes from Original (May 2009) to Revision A **Page**

- Universal change of the pin name from TESTW to VREG_PD ... 1
- Deleted paragraph form the TPBIASx pins in the *Pin Functions* table "When a port is configured as a Beta-mode port (B1, B2, B4...: ... 9

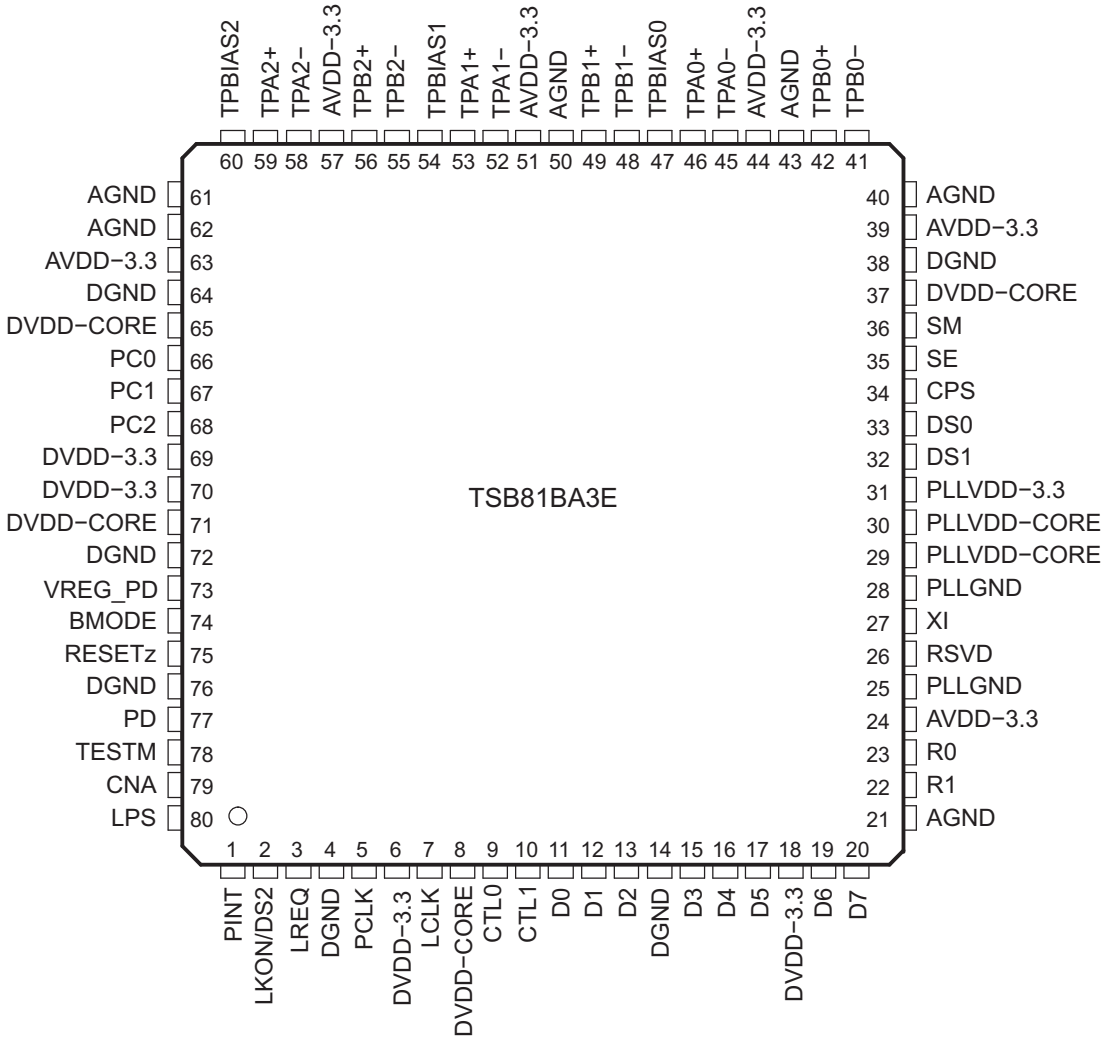
4 Description Continued

The TSB81BA3E can be powered by a single 3.3-V supply when the VREG_PD terminal (terminal 73 on the PFP package and terminal B7 on the ZAJ package) is tied to GND. VREG_PD enables the internal 3.3-V to 1.95-V regulator which provides the 1.95-V to the core. The When VREG_PD is pulled high to VDD through at least a 1-kΩ resistor the TSB81BA3E internal regulator is off and the device can be powered by two separate external regulated supplies: 3.3-V for the I/Os and 1.95-V for the core. The core voltage is supplied to the PLLVDD-CORE and DVDD-CORE terminals to the requirements in the recommended operating conditions (1.95-V nominal). The PLLVDD-CORE terminals must be separated from the DVDD-CORE terminals. The PLLVDD-CORE and the DVDD-CORE terminals must be decoupled with 1 uF capacitors to stabilze the respective supply. Additional 0.10 µF and 0.01 µF high-frequency bypass capacitors may also be used. The separation between DVDD-CORE and PLLVDD-CORE may be implemented by separate power supply rails, or by a single power supply rail, where the DVDD-CORE and PLLVDD-CORE are separated by a filter network to keep noise from the PLLVDD-CORE supply.

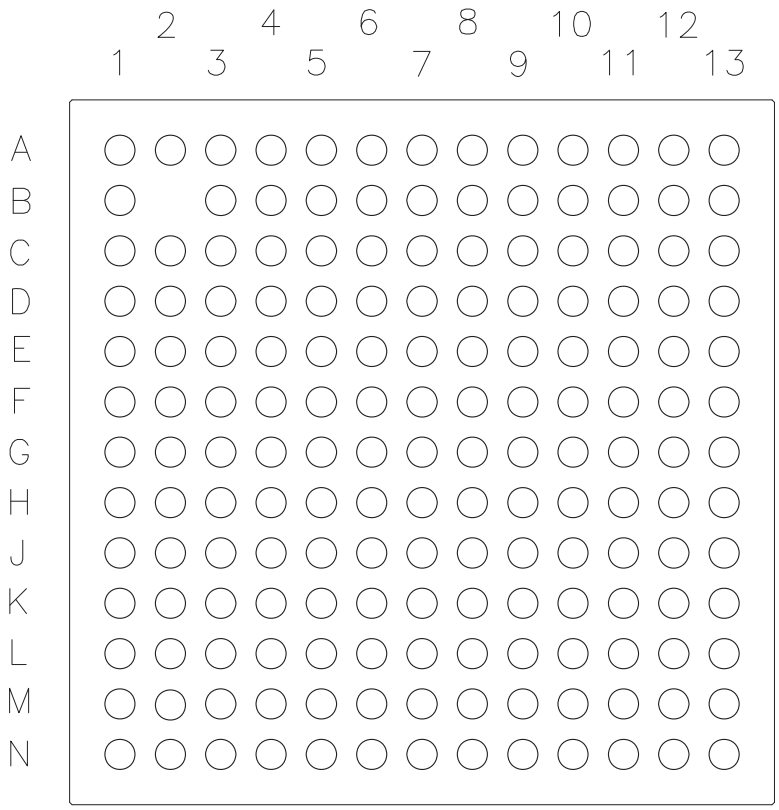
The TSB81BA3E requires an external 98.304-MHz crystal oscillator to generate a reference clock. The external clock drives an internal phase-locked loop (PLL), which generates the required reference signal. This reference signal provides the clock signals that control transmission of the outbound encoded information. A 49.152-MHz clock signal is supplied to the associated LLC for synchronization of the two devices and is used for resynchronization of the received data when operating the PHY-link interface in compliance with the IEEE 1394a-2000 standard. A 98.304-MHz clock signal is supplied to the associated LLC for synchronization of the two devices when operating the PHY-link interface in compliance with the IEEE P1394b standard. The power down (PD) function, when enabled by asserting the PD terminal high, stops operation of the PLL.

5 Pin Configuration and Function

PFP PACKAGE
(TOP VIEW)



ZAJ PACKAGE
(TOP VIEW)



Pin Functions

NAME	TYPE	PFP NO.	ZAJ NO.	I/O	DESCRIPTION
AGND(1)	Supply	21, 40, 43, 50, 61, 62	See DGND	–	Analog circuit ground terminals. These terminals must be tied together to the low-impedance circuit board ground plane.
AVDD-3.3	Supply	24, 39, 44, 51, 57, 63	M4, F10, H10, J10, E10	–	Analog circuit power terminals. A combination of high-frequency decoupling capacitors near each terminal is suggested, such as paralleled 0.1 µF and 0.001 µF. Lower frequency 10-µF filtering capacitors are also recommended. These supply terminals are separated from the PLLVDD-CORE, PLLVDD-3.3, DVDD-CORE, and DVDD-3.3 terminals internal to the device to provide noise isolation. The PLLVDD-3.3, AVDD, and DVDD-3.3 terminals must be tied together with a low dc impedance connection on the circuit board.
BMODE	CMOS	74	B6	I	Beta-mode input. This terminal determines the PHY-link interface connection protocol. When logic-high (asserted), the PHY-link interface complies with the 1394b-2002 B PHY-link interface. When logic-low (deasserted), the PHY-link interface complies with the legacy 1394a-2000 standard. When using an LLC such as the 1394b-2002 TSB82AA2, this terminal must be pulled high. When using an LLC such as the 1394a-2000 TSB12LV26, this terminal must be tied low. NOTE: The PHY-link interface cannot be changed between the different protocols during operation.
CNA	CMOS	79	A2	O	Cable not active output. This terminal is asserted high when there are no ports receiving incoming bias voltage. When any port receives bias, this terminal goes low.
CPS	CMOS	34	N9	I	Cable-power status input. This terminal is normally connected to cable power through a 400-kΩ resistor. This circuit drives an internal comparator that detects the presence of cable power. This transition from cable power sensed to cable power not sensed can be used to generate an interrupt to the LLC.
CTL0 CTL1	CMOS	9 10	F1 G1	I/O	Control I/Os. These bidirectional signals control communication between the TSB81BA3E and the LLC. Bus holders are built into these terminals.
D0-D7	CMOS	11, 12, 13, 15, 16, 17, 19, 20	H1, H2, J2, J1, K2, K1, L1, M1	I/O	Data I/Os. These are bidirectional data signals between the TSB82BA3 and the LLC. Bus holders are built into these terminals.
DGND(1)	Supply	4, 14, 38, 64, 72, 76	E5, F4, F5, F6, F7, F9, G4, G5, G6, G7, G8, G9, G10, H4, H5, H6, H7, H8, J4, J5, J6, J7, J8, K7, L7	–	Digital circuit ground terminals. These terminals must be tied together to the low-impedance circuit board ground plane.
DS0	CMOS	33	N8	I	Data-strobe-only mode for port 0. 1394a-only port 0 enable programming terminal. On hardware reset, this terminal allows the user to select whether port 0 acts like a 1394b bilingual port (terminal at logic 0) or as a 1394a-2000-only port (terminal at logic 1). Programming is accomplished by tying the terminal low through a 1-kΩ or less resistor (to enable 1394b bilingual mode) or high through a 1-kΩ or less resistor (to enable 1394a-2000-only mode). A bus holder is built into this terminal.
DS1	CMOS	32	M7	I	Data-strobe-only mode for port 1. 1394a-only port 1 enable programming terminal. On hardware reset, this terminal allows the user to select whether port 1 acts like a 1394b bilingual port (terminal at logic 0) or as a 1394a-2000-only port (terminal at logic 1). Programming is accomplished by tying the terminal low through a 1-kΩ or less resistor (to enable 1394b bilingual mode) or high through a 1-kΩ or less resistor (to enable 1394a-2000-only mode). A bus holder is built into this terminal.
DVDD-CORE	Supply	8, 37, 65, 71	D9, K9, D8	–	Digital core circuit power terminals. A combination of high-frequency decoupling capacitors near each terminal is suggested, such as paralleled 0.1 µF and 0.001 µF. An additional 1-µF capacitor is required for voltage regulation. These supply terminals are separated from the DVDD-3.3, PLLVDD-CORE, PLLVDD-3.3, and AVDD terminals internal to the device to provide noise isolation.

(1) All AGND and DGND terminals are internally tied together in the ZAJ package.

Pin Functions (continued)

NAME	TYPE	PFP NO.	ZAJ NO.	I/O	DESCRIPTION
DVDD-3.3	Supply	6, 18, 69, 70	E4, K5, K6	–	Digital 3.3-V circuit power terminals. A combination of high-frequency decoupling capacitors near each terminal is suggested, such as paralleled 0.1 µF and 0.001 µF. Lower-frequency 10-µF filtering capacitors are also recommended. The DVDD-3.3 terminals must be tied together at a low-impedance point on the circuit board. These supply terminals are separated from the PLLVDD-CORE, PLLVDD-3.3, DVDD-CORE, and AVDD terminals internal to the device to provide noise isolation. The PLLVDD-3.3, AVDD, and DVDD-3.3 terminals must be tied together with a low dc impedance connection on the circuit board.
LCLK	CMOS	7	G2	I	Link clock. Link-provided 98.304-MHz clock signal to synchronize data transfers from link to the PHY when the PHY-link interface is in the 1394b mode. A bus holder is built into this terminal.
LKON/DS2	CMOS	2	D2	I/O	Link-on output/Data-strobe-only input for port 2. This terminal may be connected to the link-on input terminal of the LLC through a 1-kΩ resistor if the link-on input is available on the link layer. Data-strobe-only mode for port 2. 1394a-only port 0 enable programming terminal. On hardware reset, this terminal allows the user to select whether port 2 acts like a 1394b bilingual port (terminal at logic 0) or as a 1394a-2000-only port (terminal at logic 1). Programming is accomplished by tying the terminal low through a 1-kΩ or less resistor to enable 1394b bilingual mode or high through a 1-kΩ or less resistor to enable 1394a-2000-only mode. A bus holder is built into this terminal. After hardware reset, this terminal is the link-on output, which notifies the LLC or other power-up logic to power up and become active. The link-on output is a square wave signal with a period of approximately 163 ns (8 PCLK cycles) when active. The link-on output is otherwise driven low, except during hardware reset when it is high impedance. The link-on output is activated if the LLC is inactive (the LPS input inactive or the LCtrl bit cleared) and when one: a. The PHY receives a link-on PHY packet addressed to this node. b. The PEI (port-event interrupt) register bit is 1. c. Any of the CTOI (configuration-timeout interrupt), CPSI (cable-power-status interrupt), or STOI (state-time-out interrupt) register bits is 1 and the RPIE (resuming-port interrupt enable) register bit is also 1. d. The PHY is power-cycled and the power class is 0 through 4. Once activated, the link-on output is active until the LLC becomes active (both the LPS input active and the LCtrl bit set). The PHY also deasserts the link-on output when a bus-reset occurs unless the link-on output is otherwise active because one of the interrupt bits is set (that is, the link-on output is active due solely to the reception of a link-on PHY packet). In the case of power-cycling the PHY, the LKON signal must stop after 167 µs if the preceding conditions have not been met. NOTE: If an interrupt condition exists, which otherwise would cause the link-on output to be activated if the LLC were inactive, then the link-on output is activated when the LLC subsequently becomes inactive.

Pin Functions (continued)

NAME	TYPE	PFP NO.	ZAJ NO.	I/O	DESCRIPTION
LPS	CMOS	80	D3	I	Link power status input. This terminal monitors the active/power status of the link-layer controller (LLC) and controls the state of the PHY-LLC interface. This terminal must be connected to either the V_{DD} supplying the LLC through an approximately 1-kΩ resistor or to a pulsed output that is active when the LLC is powered. A pulsed signal must be used when an isolation barrier exists between the LLC and PHY (see Figure 8). The LPS input is considered inactive if it is sampled low by the PHY for more than an LPS_RESET time (~2.6 µs), and is considered active otherwise (that is, asserted steady high or an oscillating signal with a low time less than 2.6 µs). The LPS input must be high for at least 22 ns to be observed as high by the PHY. When the TSB81BA3E detects that the LPS input is inactive, it places the PHY-LLC interface into a low-power reset state. In the reset state, the CTL (CTL0 and CTL1) and D (D0 to D7) outputs are held in the logic 0 state and the LREQ input is ignored; however, the PCLK output remains active. If the LPS input remains low for more than an LPS_DISABLE time (~26 µs), then the PHY-LLC interface is put into a low-power disabled state in which the PCLK output is also held inactive. The LLC state that is communicated in the self-ID packet is considered active only if both the LPS input is active and the LCtrl register bit is set to 1. The LLC state that is communicated in the self-ID packet is considered inactive if either the LPS input is inactive or the LCtrl register bit is cleared to 0.
LREQ	CMOS	3	E1	I	LLC request input. The LLC uses this input to initiate a service request to the TSB81BA3E. A bus holder is built into this terminal.
PC0 PC1 PC2	CMOS	66 67 68	C11 A9 B8	I	Power class programming inputs. On hardware reset, these inputs set the default value of the power class indicated during self-ID. Programming is done by tying the terminals high through a 1-kΩ or smaller resistor or by tying directly to ground through a 1-kΩ or smaller resistor. Bus holders are built into these terminals.
PCLK	CMOS	5	F2	O	PHY clock. Provides a 98.304-MHz clock signal, synchronized with data transfers, to the LLC when the PHY-link interface is operating in the 1394b mode (BMODE asserted). PCLK output provides a 49.152-MHz clock signal, synchronized with data transfers, to the LLC when the PHY-link interface is in legacy 1394a-2000 (BMODE input deasserted).
PD	CMOS	77	B3	I	Power-down input. A high on this terminal turns off all internal circuitry except the cable-active monitor circuits, which control the CNA output. Asserting the PD input high also activates an internal pulldown on the $\overline{\text{RESET}}$ terminal to force a reset of the internal control logic.
PINT	CMOS	1	E3	O	PHY interrupt. The PHY uses this output to serially transfer status and interrupt information to the link when PHY-link interface is in the 1394b mode. A bus holder is built into this terminal.
PLLGND	Supply	25, 28	F8, N4	–	PLL circuit ground terminals. These terminals must be tied together to the low-impedance circuit board ground plane.
PLLVDD-CORE	Supply	29, 30	N6	–	PLL core circuit power terminals. A combination of high-frequency decoupling capacitors near each terminal is suggested, such as paralleled 0.1 µF and 0.001 µF. An additional 1-µF capacitor is required for voltage regulation. The PLLVDD-CORE terminals must be separate from the DVDD-CORE terminals. These supply terminals are separated from the DVDD-CORE, DVDD-3.
PLLVDD-3.3	Supply	31	N7	–	PLL 3.3-V circuit power terminal. A combination of high-frequency decoupling capacitors near the terminal are suggested, such as paralleled 0.1 µF and 0.001 µF. Lower frequency 10-µF filtering capacitors are also recommended. This supply terminal is separated from the DVDD-CORE, DVDD-3.3, PLLVDD-CORE, and AVDD-3.3 terminals internal to the device to provide noise isolation. The DVDD-3.3 terminals must be tied together at a low-impedance point on the circuit board. The PLLVDD-3.3, AVDD-3.3, and DVDD-3.3 terminals must be tied together with a low dc impedance connection.

Pin Functions (continued)

NAME	TYPE	PFP NO.	ZAJ NO.	I/O	DESCRIPTION
$\overline{\text{RESET}}$	CMOS	75	A6	I	Logic reset input. Asserting this terminal low resets the internal logic. An internal pullup resistor to V_{DD} is provided so only an external delay capacitor is required for proper power-up operation (see *power-up reset* in the *Applications Information* section). The $\overline{\text{RESET}}$ terminal also incorporates an internal pulldown, which is activated when the PD input is asserted high. This input is otherwise a standard logic input, and can also be driven by an open-drain-type driver.
RSVD	Osc Out	26	M5	O	This terminal must normally be left unconnected. When this terminal is probed, the terminal shows a 98.304-MHz signal. If this is perceived as an EMI problem, then the terminal may be pulled to ground through a 10-kΩ resistor. However, this causes an increase of up to 340 µA in device current consumption.
R0 R1	Bias	23 22	N3 N2	–	Current setting resistor terminals. These terminals are connected to a precision external resistance to set the internal operating currents and cable driver output currents. A resistance of 6.34 kΩ, ±1%, is required to meet the IEEE Std 1394-1995 output voltage limits.
SE	CMOS	35	M10	I	Test control input. This input is used in the manufacturing test of the TSB81BA3E. For normal use this terminal must be pulled low either through a 1-kΩ resistor to GND or directly to GND.
SM	CMOS	36	N10	I	Test control input. This input is used in the manufacturing test of the TSB81BA3E. For normal use this terminal must be pulled low either through a 1-kΩ resistor to GND or directly to GND.
TESTM	CMOS	78	A3	I	Test control input. This input is used in the manufacturing test of the TSB81BA3E. For normal use this terminal must be pulled high through a 1-kΩ resistor to V_{DD}.
VREG_PD	CMOS	73	B7	I	Voltage regulator power-down input. When asserted logic high, this pin will power-down the internal 3.3-V to 1.95-V regulator. For single 3.3-V supply operation, this pin should be tied to GND. If an external regulator is used to supply the 1.95-V PLLVDD-CORE and DVDD-CORE power rails this terminals should be pulled to Vcc through a 1-kΩ resistor to V_{DD}.
TPA0– TPA0+ TPB0– TPB0+	Cable	45 46 41 42	K13 J13 M13 L13	I/O	Port-0 twisted-pair differential-signal terminals. Board traces from each pair of positive and negative differential signal terminals must be kept matched and as short as possible to the external load resistors and to the cable connector. Request the S800 1394b layout recommendations document from your Texas Instruments representative.
TPA1– TPA1+ TPB1– TPB1+	Cable	52 53 48 49	F13 E13 H13 G13	I/O	Port-1 twisted-pair differential-signal terminals. Board traces from each pair of positive and negative differential signal terminals must be kept matched and as short as possible to the external load resistors and to the cable connector. Request the S800 1394b layout recommendations document from your Texas Instruments representative.
TPA2– TPA2+ TPB2– TPB2+	Cable	58 59 55 56	B13 A13 D13 C13	I/O	Port-2 twisted-pair differential-signal terminals. Board traces from each pair of positive and negative differential signal terminals must be kept matched and as short as possible to the external load resistors and to the cable connector. Request the S800 1394b layout recommendations document from your Texas Instruments representative.
TPBIAS0 TPBIAS1 TPBIAS2	Cable	47 54 60	J12 E12 A12	I/O	Twisted-pair bias output and signal detect input. This provides the 1.86-V nominal bias voltage needed for proper operation of the twisted-pair cable drivers and receivers, and for signaling to the remote nodes that there is an active cable connection in 1394a-2000 mode. Each of these terminals, except for an unused port, must be decoupled with a 1-µF capacitor to ground. For the unused port, this terminal can be left unconnected. Please request the S800 1394b layout recommendation documents from your TI representative.
XI	Osc In	27	N5	–	Oscillator input. This terminal connects to a 98.304-MHz low jitter external oscillator. The XI terminal is a 1.8-V CMOS input. Oscillator jitter must be 5 ps RMS or better. If only 3.3-V oscillators can be acquired, then great care must be taken to not introduce significant jitter by the means used to level shift from 3.3 V to 1.8 V. If a resistor divider is used, then a high current oscillator and low-value resistors must be used to minimize RC time constants. If a level-shifting circuit is used, then it must introduce very little jitter. Please see layout recommendations document.

6 Electrical Specfications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Supply voltage range(2)		–0.3	4	V
V_I	Input voltage range(2)		–0.5	V_{DD} + 0.5	V
V_O	Output voltage range at any output		–0.5	V_{DD} + 0.5	V
	Continuous total power dissipation		See Dissipation Ratings Table		
T_A	Operating free-air temperature	TSB81BA3E	0	70	°C
		TSB81BA3EI	–40	85	
T_{stg}	Storage temperature range		65	150	°C
	Lead temperature 1.6 mm (1/16 in) from case for 10 s			260	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground.

6.2 Thermal Information

THERMAL METRIC(1)			TSB81BA3E		UNIT
			PFP (HTQFP)	ZJA (NFBGA)	
			80 PINS	167 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	Low K JEDEC Test Board, 1s (single signal layer), no air flow	27.2	46.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	High K JEDEC Test Board 2s2p (double signal layer, double buried power plane)	8.9	23.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	Cu Cold Plate Measurement Process	11.1	27.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	EIA/JESD 51-8	0.3	0.45	°C/W
ψ_{JB}	Junction-to-board characterization parameter	EIA/JESD 51-2	11.0	27.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	EIA/JESD 51-6	0.3	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.3 Recommended Operating Conditions

			MIN	TYP(1)	MAX	UNIT
3.3 V_{DD}	Supply voltage	Source power node	3.0	3.3	3.6	V
		Nonsource power node	3.0(2)	3.3	3.6	
Core V_{DD}	Supply voltage		1.85	1.95	2.05	V
V_{IH}	High-level input voltage	LREQ, CTL0, CTL1, D0-D7, LCLK	2.6			V
		LKON/DS2, PC0, PC1, PC2, PD, BMODE	0.7 × V_{DD}			
		RESETz	0.6 × V_{DD}			
V_{IL}	Low-level input voltage	LREQ, CTL0, CTL1, D0-D7, LCLK			1.2	V
		LKON/DS2, PC0, PC1, PC2, PD, BMODE			0.2 × V_{DD}	
		RESETz			0.3 × V_{DD}	
V_{OD}	1394b Differential output voltage			700		mV
V_{CM}	1394b Common-mode output voltage			1.5		V
I_{DD}	Supply current in low power/suspend(3)	$V_{D\ D}$ = 3.3 V		4		mA
		$V_{D\ D}$ = 3 V		3		mA
$I_{OL/OH}$	Output current	CTL0, CTL1, D0-D7, CNA, LKON/DS2, PINT, and PCLK	–4		4	mA
I_O	Output current	TPBIAS outputs	–5.6		1.3	mA
T_A	Operating ambient temperature range	TSB81BA3E	0		70	°C
T_J	Junction temperature(4)	TSB81BA3E	0		105	°C
V_{ID}	1394b Differential input voltage	Cable inputs, during data reception	200		800	mV
V_{ID}	1394a Differential input voltage	Cable inputs, during data reception	118		260	mV
		Cable inputs, during arbitration	168		265	
V_{IC}	1394a Common-mode input voltage	TPB cable inputs, source power node	0.4706		2.515	V
		TPB cable inputs, nonsource power node	0.4706		2.015(2)	
t_{pu}	Power-up reset time	RESETz input	2(5)			ms
	Receive input jitter	TPA, TPB cable inputs, S100 operation			±1.08	ns
		TPA, TPB cable inputs, S200 operation			±0.5	
		TPA, TPB cable inputs, S400 operation			±0.315	
	Receive input skew	Between TPA and TPB cable inputs, S100 operation			±0.8	ns
		Between TPA and TPB cable inputs, S200 operation			±0.55	
		Between TPA and TPB cable inputs, S400 operation			±0.5	

(1) All typical values are at V_{DD} = 3.3 V and T_A = 25°C.
(2) For a node that does not source power, see Section 4.2.2.2 in IEEE 1394a-2000.
(3) The low power/suspend mode assumes that the device is not receiving packets and it is toning.
(4) The junction temperature reflects simulated conditions. The customer is responsible for verifying junction temperature.
(5) Time after valid clock received at PHY XI input terminal.

6.4 Electrical Characteristics, Driver

over recommended ranges of operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OD}	Differential output voltage	56 Ω, See Figure 1	172		265	mV
I_{DIFF}	Driver difference current, TPA+, TPA–, TPB+, TPB–	Drivers enabled, speed signaling off	–1.05 (1)		1.05 (1)	mA
I_{SP200}	Common-mode speed signaling current, TPB+, TPB–	S200 speed signaling enabled	–4.84 (2)		–2.53 (2)	mA
I_{SP400}	Common-mode speed signaling current, TPB+, TPB–	S400 speed signaling enabled	–12.4 (2)		–8.1 (2)	mA
V_{OFF}	Off-state differential voltage	Drivers disabled, See Figure 1			20	mV

(1) Limits defined as algebraic sum of TPA+ and TPA– driver currents. Limits also apply to TPB+ and TPB– algebraic sum of driver currents.
(2) Limits defined as absolute limit of each of TPB+ and TPB– driver currents.

6.5 Electrical Characteristics, Receiver

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Z_{ID}	Differential impedance	Drivers disabled	4	7		kΩ
					4	pF
Z_{IC}	Common-mode impedance	Drivers disabled	20			kΩ
					24	pF
V_{TH-R}	Receiver input threshold voltage	Drivers disabled	–30		30	mV
V_{TH-CB}	Cable bias detect threshold, TPBx cable inputs	Drivers disabled	0.6		1	V
V_{TH+}	Positive arbitration comparator threshold voltage	Drivers disabled	89		168	mV
$V_{TH–}$	Negative arbitration comparator threshold voltage	Drivers disabled	–168		–89	mV
$V_{TH-SP200}$	Speed signal threshold	TPBIAS-TPA common-mode voltage, drivers disabled	49		131	mV
$V_{TH-SP400}$	Speed signal threshold		314		396	mV

6.6 Electrical Characteristics, Device

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DD}	Supply current	3.3 V_{DD}	(1)			120	150	mA
		Core V_{DD}				79		
V_{TH}	Power status threshold, CPS input (2)		400-kΩ resistor (2)		4.7		7.5	V
V_{OH}	High-level output voltage, CTL0, CTL1, D0-D7, PCLK, LKON/DS2 outputs		V_{DD} = 3 to 3.6 V, I_{OH} = 4 mA		2.8			V
V_{OL}	Low-level output voltage, CTL0, CTL1, D0-D7, PCLK, LKON/DS2 outputs		I_{OL} = 4 mA				0.4	V
I_{BH+}	Positive peak bus holder current, D0-D7, CTL0-CTL1, LREQ		V_{DD} = 3.6 V, V_I = 0 V to V_{DD}		0.05		1	mA
$I_{BH–}$	Negative peak bus holder current, D0-D7, CTL0-CTL1, LREQ		V_{DD} = 3.6 V, V_I = 0 V to V_{DD}		–1.0		–0.05	mA
I_{OZ}	Off-state output current, CTL0, CTL1, D0-D7, LKON/DS2 I/Os		V_O = V_{DD} or 0 V	TSB81BA3E			±5	μA
				TSB81BA3EI			±20	
I_{IRST}	Pullup current, $\overline{RESET}$ input		V_I = 1.5 V or 0 V		–90		–20	μA
V_O	TPBIAS output voltage		At rated I_O current		1.665		2.015	V

(1) Repeat max packet (one port receiving maximum size isochronous packet–8192 bytes, sent on every isochronous interval, S800, data value of 0xCCCCCCCCh; two ports repeating; all ports with beta-mode connection), $V_{DD3.3}$ = 3.3 V, V_{DDCORE} = 1.95 V, T_A = 25°C.
(2) Measured at cable-power side of resistor.

6.7 Switching Characteristics

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	TP differential rise time, transmit		10% to 90%, At 1394 connector	0.5		1.2	ns
t_f	TP differential fall time, transmit		90% to 10%, At 1394 connector	0.5		1.2	ns
t_{su}	Setup time, CTL0, CTL1, D1-D7, LREQ to PCLK	1394a-2000	50% to 50%, See Figure 2	2.5			ns
t_h	Hold time, CTL0, CTL1, D1-D7, LREQ after PCLK	1394a-2000	50% to 50%, See Figure 2	0			ns
t_{su}	Setup time, CTL0, CTL1, D1-D7, LREQ to LCLK_PMC	1394b	50% to 50%, See Figure 2	2.5			ns
t_h	Hold time, CTL0, CTL1, D1-D7, LREQ after LCLK_PMC	1394b	50% to 50%, See Figure 2	0			ns
t_d	Delay time, PCLK to CTL0, CTL1, D1-D7, PINT	1394a-2000 and 1394b	50% to 50%, See Figure 3	0.5	7		ns

7 Parameter Measurement Information

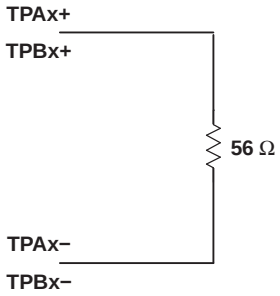


Figure 1. Test Load Diagram

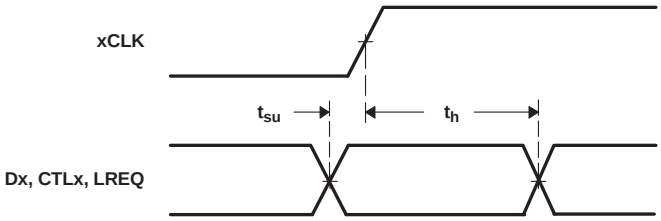


Figure 2. Dx, CTLx, LREQ Input Setup and Hold Time Waveforms

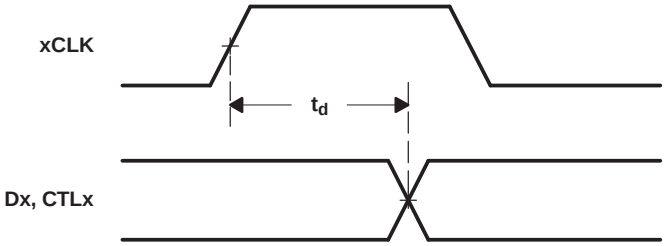


Figure 3. Dx and CTLx Output Delay Relative to xCLK Waveforms

8 Detailed Description

8.1 Overview

Data bits to be transmitted through the cable ports are received from the LLC on two-, four-, or eight-bit parallel paths (depending on the requested transmission speed and PHY-link interface mode of operation). They are latched internally, combined serially, encoded, and transmitted at 98.304, 196.608, 393.216, 491.52, or 983.04 Mbits/s (referred to as S100, S200, S400, S400B, or S800 speed, respectively) as the outbound information stream.

The PHY-link interface can follow either the IEEE 1394a-2000 protocol or the IEEE 1394b-2002 protocol. When using a 1394a-2000 LLC such as the TSB12LV26, the BMODE terminal must be deasserted. The PHY-link interface then operates in accordance with the legacy 1394a-2000 standard. When using a 1394b LLC such as the TSB82AA2, the BMODE terminal must be asserted. The PHY-link interface then conforms to the P1394b standard.

The cable interface can follow either the IEEE 1394a-2000 protocol or the 1394b protocol on all ports. The mode of operation is determined by the interface capabilities of the ports being connected. When any of the three ports is connected to a 1394a-2000 compliant device, the cable interface on that port operates in the 1394a-2000 data-strobe mode at a compatible S100, S200, or S400 speed. When a bilingual port is connected to a 1394b compliant node, the cable interface on that port operates per the P1394b standard at S400B or S800 speed. The TSB81BA3E automatically determines the correct cable interface connection method for the bilingual ports.

NOTE

The BMODE terminal does not select the cable interface mode of operation. The BMODE terminal selects the PHY-link interface mode of operation and affects the arbitration modes on the cable. When the BMODE terminal is deasserted, BOSS arbitration is disabled.

During packet reception the serial data bits are split into two-, four-, or eight-bit parallel streams (depending upon the indicated receive speed and the PHY-link interface mode of operation), resynchronized to the local system clock and sent to the associated LLC. The received data is also transmitted (repeated) on the other connected and active cable ports.

During packet reception the serial data bits are split into two-, four-, or eight-bit parallel streams (depending upon the indicated receive speed and the PHY-link interface mode of operation), resynchronized to the local system clock and sent to the associated LLC. The received data is also transmitted (repeated) on the other connected and active cable ports.

Both the twisted pair A (TPA) and the twisted pair B (TPB) cable interfaces incorporate differential comparators to monitor the line states during initialization and arbitration when connected to a 1394a-2000 compliant device. The outputs of these comparators are used by the internal logic to determine the arbitration status. The TPA channel monitors the incoming cable common-mode voltage. The value of this common-mode voltage is used during 1394a-mode arbitration and sets the speed of the next packet transmission. In addition, the TPB channel monitors the incoming cable common-mode voltage on the TPB pair for the presence of the remotely supplied twisted pair bias (TPBIAS) voltage.

When connected to a 1394a-2000 compliant node, the TSB81BA3E provides a 1.86-V nominal bias voltage at the TPBIAS terminal for port termination. The PHY contains three independent TPBIAS circuits (one for each port). This bias voltage, when seen through a cable by a remote receiver, indicates the presence of an active connection. This bias voltage source must be stabilized by an external filter capacitor of 1 µF.

The line drivers in the TSB81BA3E are designed to work with external 112-Ω termination resistor networks to match the 110-Ω cable impedance. One termination network is required at each end of a twisted-pair cable. Each network is composed of a pair of series-connected ~56-Ω resistors. The midpoint of the pair of resistors that are connected to the TPA terminals is connected to its corresponding TPBIAS voltage terminal. The midpoint of the pair of resistors that are directly connected to the TPB terminals is coupled to ground through a parallel RC network with recommended values of 5 kΩ and 270 pF. The values of the external line-termination resistors are designed to meet the standard specifications when connected in parallel with the internal receiver circuits. A precision external resistor connected between the R0 and R1 terminals sets the driver output current, along with other internal operating currents.

Overview (continued)

When the power supply of the TSB81BA3E is off while the twisted-pair cables are connected, the TSB81BA3E transmitter and receiver circuitry present a high-impedance signal to the cable that does not load the device at the other end of the cable.

When the TSB81BA3E is used without one or more of the ports brought out to a connector, the twisted-pair terminals of the unused ports must be terminated for reliable operation. For each unused port, the port must be forced to the 1394a-only mode (Data-Strobe-only mode), then the TPB+ and TPB– terminals can be tied together and then pulled to ground; or the TPB+ and TPB– terminals can be connected to the suggested normal termination network. The TPA+ and TPA– terminals of an unused port can be left unconnected. The TPBIAS terminal can be connected to a 1-μF capacitor to ground or left unconnected.

To operate a port as a 1394b bilingual port, the force data-strobe-only terminal for the port (DS0, DS1, or DS2) needs to be pulled to ground through a 1-kΩ resistor. The port must be operated in the 1394b bilingual mode whenever a 1394b bilingual or a 1394b beta-only connector is connected to the port. To operate the port as a 1394a-only port, the force data-strobe-only terminal (DS0, DS1, or DS2) needs to be pulled to 3.3 V V_{CC} through a 1-kΩ resistor. The only time the port must be forced to the data-strobe-only mode is if the port is connected to a 1394a connector (either 6 pin, which is recommended, or 4 pin). This mode is provided to ensure that 1394b Signaling is never sent across a 1394a cable.

The TESTM, VREG_PD, SE, and SM terminals are used to set up various manufacturing test conditions. For normal operation, the TESTM and VREG_PD terminals must be connected to V_{DD} through a 1-kΩ resistor. The SE and SM terminals must be tied to ground through a 1-kΩ resistor.

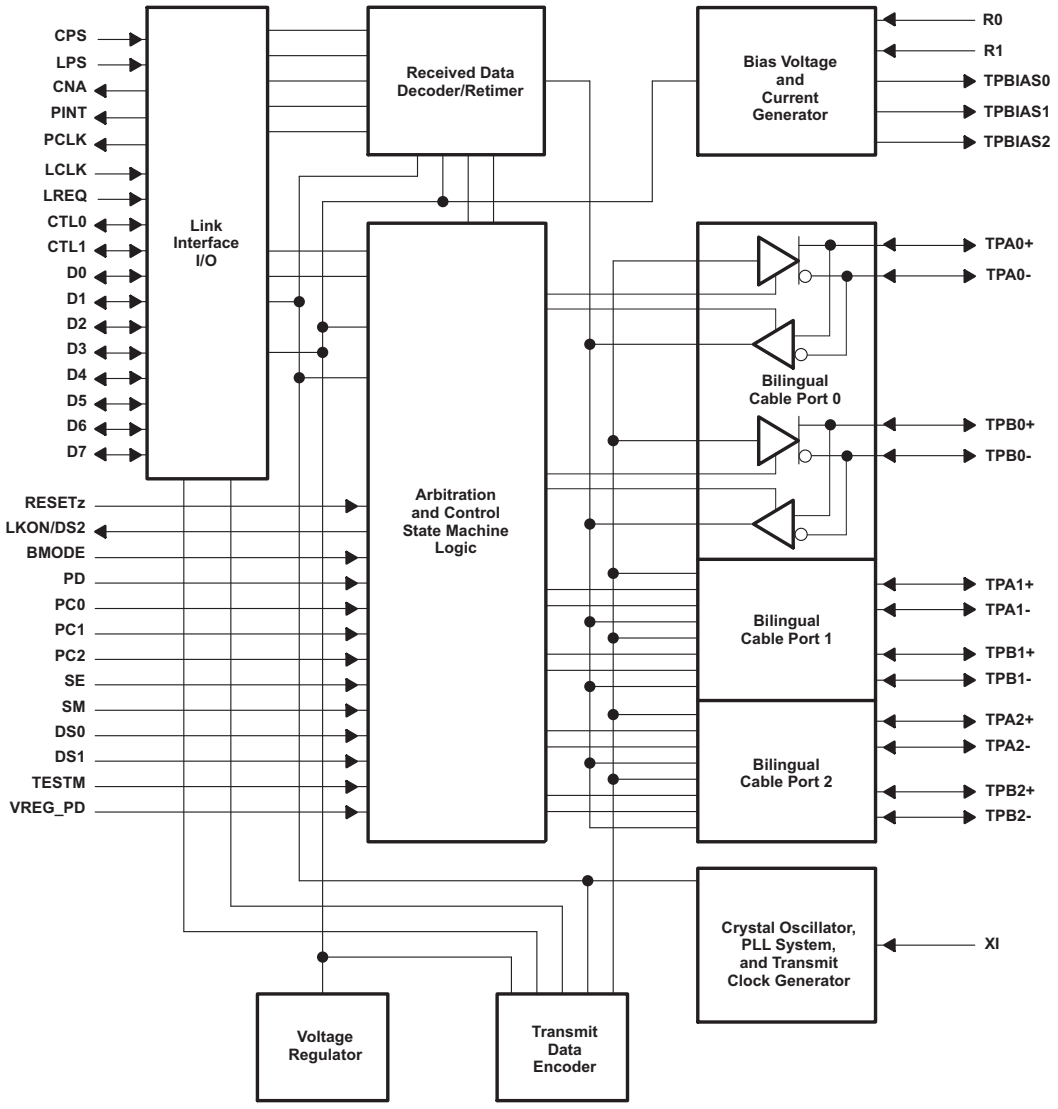
Three package terminals are used as inputs to set the default value for three configuration status bits in the self-ID packet. They may be pulled high through a 1-kΩ resistor or hardwired low as a function of the equipment design. The PC0, PC1, and PC2 terminals indicate the default power class status for the node (the need for power from the cable or the ability to supply power to the cable). The contender bit in the PHY register set indicates that the node is a contender either for the isochronous resource manager (IRM) or for the bus manager (BM). On the TSB81BA3E, this bit may only be set by a write to the PHY register set. If a node desires to be a contender for IRM or BM, then the node software must set this bit in the PHY register set.

The LPS (link power status) terminal works with the LKON/DS2 terminal to manage the power usage in the node. The LPS signal from the LLC is used with the LCtrl bit (see Table 4 and Table 5 in the *Application Information* section) to indicate the active/power status of the LLC. The LPS signal also resets, disables, and initializes the PHY-LLC interface (the state of the PHY-LCC interface is controlled solely by the LPS input regardless of the state of the LCtrl bit).

The LPS input is considered inactive if it remains low for more than the LPS_RESET time (see the LPS terminal definition) and is considered active otherwise. When the TSB81BA3E detects that the LPS input is inactive, the PHY-LLC interface is placed into a low-power reset state in which the CTL and D outputs are held in the logic 0 state and the LREQ input is ignored; however, the PCLK output remains active. If the LPS input remains low for more than the LPS_DISABLE time (see the LPS terminal definition), then the PHY-LLC interface is put into a low-power disabled state in which the PCLK output is also held inactive. The TSB81BA3E continues the necessary repeater functions required for normal network operation regardless of the state of the PHY-LLC interface. When the interface is in the reset or disabled state and the LPS input is again observed active, the PHY initializes the interface and returns to normal operation. The PHY-LLC interface is also held in the disabled state during hardware reset. When the LPS terminal is returned to an active state after being sensed as having entered the LPS_DISABLE time, the TSB81BA3E issues a bus reset. This broadcasts the node self-ID packet, which contains the updated L bit state (the PHY LLC now being accessible).

The PHY uses the LKON/DS2 terminal to notify the LLC to power up and become active. When activated, the output LKON/DS2 signal is a square wave. The PHY activates the LKON/DS2 output when the LLC is inactive and a wake-up event occurs. The LLC is considered inactive when either the LPS input is inactive, as described above, or the LCtrl bit is cleared to 0. A wake-up event occurs when a link-on PHY packet addressed to this node is received, or conditionally when a PHY interrupt occurs. The PHY deasserts the LKON/DS2 output when the LLC becomes active (both LPS sensed as active and the LCtrl bit set to 1). The PHY also deasserts the LKON/DS2 output when a bus reset occurs, unless a PHY interrupt condition exists, which would otherwise cause LKON/DS2 to be active. If the PHY is power cycled and the power class is 0 through 4, then the PHY asserts LKON/DS2 for approximately 167 μs or until both the LPS is active and the LCTRL bit is 1.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 TTL Input Data

The data inputs to the transmitter come from the graphics processor and consist of up to 24 bits of video information, a horizontal synchronization bit, a vertical synchronization bit, an enable bit, and a spare bit. The data can be loaded into the registers upon either the rising or falling edge of the input clock selectable by the CLKSEL pin. Data inputs are 1.8 V to 3.3 V tolerant for the TSB81BA3E and can connect directly to low-power, low-voltage application and graphic processors. The bit mapping is listed in Table 1.

Table 1. Pixel Bit Ordering

	RED	GREEN	BLUE
LSB	R0	G0	B0
	R1	G1	B1
	R2	G2	B2
4-bit MSB	R3	G3	B3
	R4	G4	B4

Feature Description (continued)

Table 1. Pixel Bit Ordering (continued)

	RED	GREEN	BLUE
6-bit MSB	R5	G5	B5
	R6	G6	B6
8-bit MSB	R7	G7	B7

8.3.2 LVDS Output Data

The pixel data assignment is listed in Table 2 for 24-bit, 18-bit, and 12-bit color hosts.

Table 2. Pixel Data Assignment

SERIAL CHANNEL	DATA BITS	8-BIT			6-BIT	4-BIT	
		FORMAT-1	FORMAT-2	FORMAT-3		NON-LINEAR STEP SIZE	LINEAR STEP SIZE
Y0	D0	R0D27	R2	R2	R0	R2	VCC
	D1	R1	R3	R3	R1	R3	GND
	D2	R2	R4	R4	R2	R0	R0
	D3	R3	R5	R5	R3	R1	R1
	D4	R4	R6	R6	R4	R2	R2
	D6	R5	R7	R7	R5	R3	R3
	D7	G0	G2	G2	G0	G2	VCC
Y1	D8	G1	G3	G3	G1	G3	GND
	D9	G2	G4	G4	G2	G0	G0
	D12	G3	G5	G5	G3	G1	G1
	D13	G4	G6	G6	G4	G2	G2
	D14	G5	G7	G7	G5	G3	G3
	D15	B0	B2	B2	B0	B2	VCC
	D18	B1	B3	B3	B1	B3	GND
Y2	D19	B2	B4	B4	B2	B0	B0
	D20	B3	B5	B5	B3	B1	B1
	D21	B4	B6	B6	B4	B2	B2
	D22	B5	B7	B7	B5	B3	B3
	D24	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
	D25	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
	D26	ENABLE	ENABLE	ENABLE	ENABLE	ENABLE	ENABLE
Y3	D27	R6	R0	GND	GND	GND	GND
	D5	R7	R1	GND	GND	GND	GND
	D10	G6	G0	GND	GND	GND	GND
	D11	G7	G1	GND	GND	GND	GND
	D16	B6	B0	GND	GND	GND	GND
	D17	B7	B1	GND	GND	GND	GND
	D23	RSVD	RSVD	GND	GND	GND	GND
CLKOUT	CLKIN	CLK	CLK	CLK	CLK	CLK	CLK

8.4 Device Functional Modes

8.4.1 Input Clock Edge

The transmission of data bits D0 through D27 occurs as each are loaded into registers upon the edge of the CLKIN signal, where the rising or falling edge of the clock may be selected via CLKSEL. The selection of a clock rising edge occurs by inputting a high level to CLKSEL, which is achieved by populating pull-up resistor to pull CLKSEL=high. Inputting a low level to select a clock falling edge is achieved by directly connecting CLKSEL to GND.

8.4.2 Low Power Mode

The TSB81BA3E can be put in low-power consumption mode by active-low input SHTDN#. Connecting pin SHTDN# to GND will inhibit the clock and shut off the LVDS output drivers for lower power consumption. A low-level on this signal clears all internal registers to a low-level. Populate a pull-up to VCC on SHTDN# to enable the device for normal operation.

8.4.3 1394b Port Interface Considerations

The TSB81BA3E has three 1394b cable ports that can operate at 100, 200, 400, or 800 Mbps. These ports are compliant with the IEEE Std 1394b-2002, standard. This section describes implementation considerations for the TSB81BA3E's 1394b cable ports.

- The cable not active (CNA) terminal is an output that reflects the state of the incoming 1394b cable port bias voltage. If no cable bias voltage is detected by the TSB81BA3E, then this output is asserted high. If the CNA terminal is not used, then it must be connected to GND through a 43-kΩ resistor.
- The cable power status (CPS) terminal is an input that drives an internal comparator for the purpose of detecting the presence of 1394b cable power. Normally, terminal CPS is connected to the 1394b cable power source through a 390-kΩ resistor. However, if this detection feature is not used, then CPS should be connected directly to GND.
- PC2, PC1, and PC0 are the power class programming inputs. These inputs are loaded into the power class field in the 1394b PHY base configuration registers. Since the binary value associated with the power class field is implementation specific, the system designer must reference the 1394b power class description table in the TSB81BA3E Data Manual to determine the appropriate PC2:0 input levels. Each terminal is connected to either GND or VDD_33 to specify the appropriate power class binary value. This connection may either be direct or through a weak resistor.
- Terminals R0 and R1 are provided to set the operating current of the cable driver. A 6.34-kΩ ±1% resistor is required to meet the IEEE Std. output voltage limits. One side of the resistor is connected to the R0 terminal and the other side of the resistor to the R1 terminal. Signal traces must be short to minimize noise coupling into the two terminals.
- TPAxP, TPAxN, TPBxP, TPBxN, and TPBIASx comprise the five major terminals associated with 1394b PHY port (Where x = Port#). TPAxP and TPAxN are the cable-A differential signals. TPBxP and TPBxN are the cable-B differential signals. TPBIASx provides the 1.86-V nominal bias required for proper 1394a driver/receiver operation and for active cable connection signaling to the remote node. The 1394b TPA and TPB differential pairs must follow the same routing guidelines as the PCI Express TX and RX differential pairs except for the differential impedance requirement of 110 ohms. For an unused port, all five terminals can be left as no connects. See the attached schematics for external circuit recommendations between the TSB81BA3E and 1394b cable connector.
- The TSB81BA3E is designed to use an external 98.304-MHz crystal oscillator connected to the XI terminal to provide the reference clock. This clock, in turn, drives a PLL circuit that generates the various clocks required for transmission and resynchronization of data at the S100 through S800 media data rates.

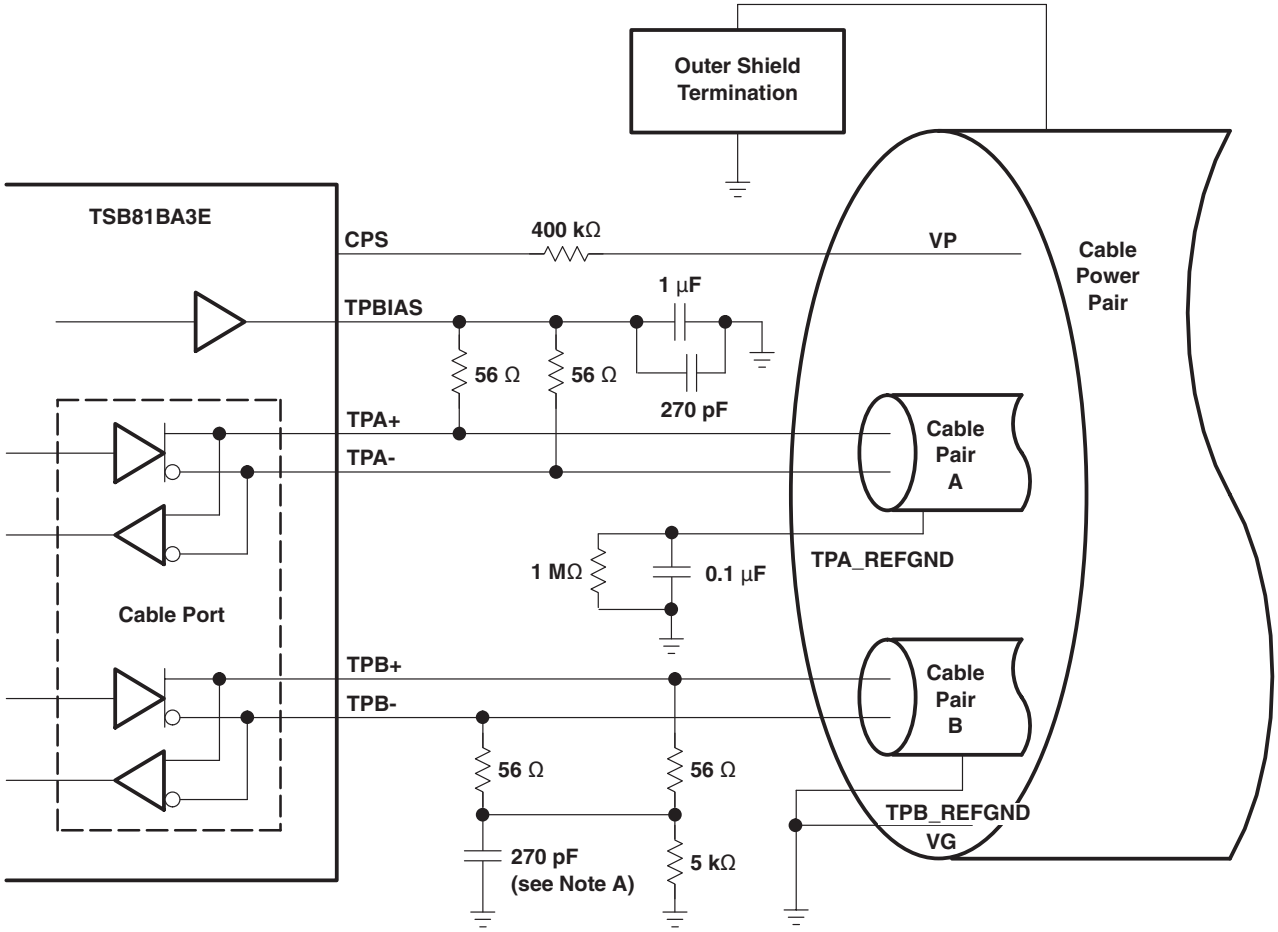
8.5 Programming

8.5.1 Power-Class

The PC0-PC2 terminals are programmed to set the default value of the power-class indicated in the pwr field (bits 21−23) of the transmitted self-ID packet. Descriptions of the various power-classes are given in Table 3. The default power-class value is loaded following a hardware reset, but is overridden by any value subsequently loaded into the Pwr_Class field in register 4.

Table 3. Power-Class Descriptions

PC0-PC2	DESCRIPTION
000	Node does not need power and does not repeat power
001	Node is self-powered and provides a minimum of 15 W to the bus.
010	Node is self-powered and provides a minimum of 30 W to the bus.
011	Node is self-powered and provides a minimum of 45 W to the bus.
100	Node can be powered from the bus and is using up to 3 W; no additional power is needed to enable the link. The node can also provide power to the bus. The amount of bus power that it provides can be found in the configuration ROM.
101	Reserved for future standardization.
110	Node is powered from the bus and uses up to 3 W. An additional 3 W is needed to enable the link.
111	Node is powered from the bus and uses up to 3 W. An additional 7 W is needed to enable the link.



NOTE A: The IEEE Std 1394- 1995 calls for a 250-pF capacitor, which is a nonstandard component value. A 270-pF capacitor is recommended.

Figure 4. Typical TP Cable Connections

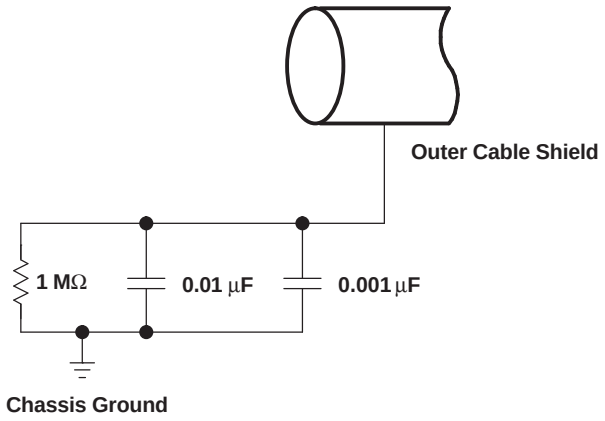


Figure 5. Typical DC-Isolated Outer Shield Termination

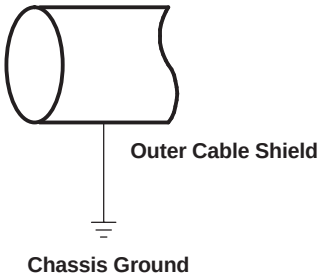


Figure 6. Non-DC-Isolated Outer Shield Termination

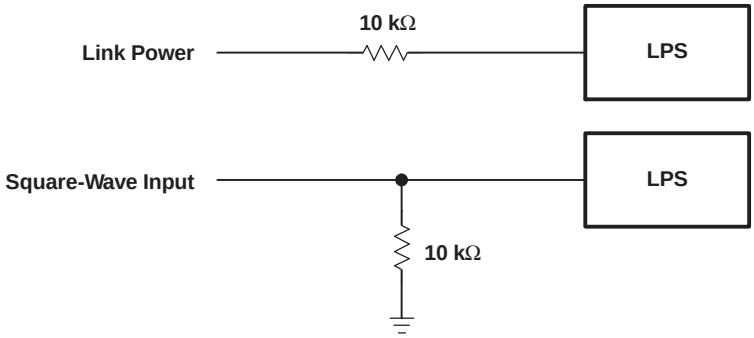


Figure 7. Nonisolated Connection Variations for LPS

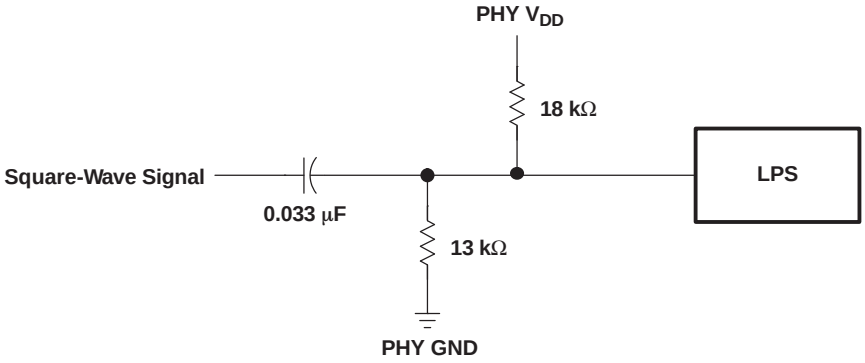


Figure 8. Isolated Circuit Connection for LPS

8.6 Register Maps

8.6.1 Internal Register Configuration

There are 16 accessible internal registers in the TSB81BA3E. The configuration of the registers at addresses 0h through 7h (the base registers) is fixed, while the configuration of the registers at addresses 8h through Fh (the paged registers) is dependent upon which 1 of 8 pages, numbered 0h through 7h, is currently selected. The selected page is set in base register 7h. Note that while this register set is compatible with 1394a--2000 register sets, some fields have been redefined and this register set contains additional fields.

Table 4 shows the configuration of the base registers, and Table 5 gives the corresponding field descriptions. The base register field definitions are unaffected by the selected page number.

A reserved register or register field (marked as Reserved or Rsvd in the following register configuration tables) is read as 0, but is subject to future usage. All registers in address pages 2 through 6 are reserved.

Table 4. Base Register Configuration

ADDRESS	BIT POSITION							
	0	1	2	3	4	5	6	7
0000	Physical ID						R	CPS
0001	RHB	IBR	Gap_Count					
0010	Extended (111b)			Num_Ports (0011b)				
0011	PHY_Speed (111b)			SREN	Delay (1111b)			
0100	LCtrl	C	Jitter (000b)			Pwr_Class		
0101	WDIE	ISBR	CTOI	CPSI	STOI	PEI	EAA	EMC
0110	Max Legacy SPD			BLINK	Bridge		Rsvd	
0111	Page_Select			Rsvd	Port_Select			

Table 5. Base Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
Physical ID	6	Rd	This field contains the physical address ID of this node determined during self-ID. The physical-ID is invalid after a bus reset until the self-ID has completed as indicated by an unsolicited register 0 status transfer from the PHY to the LLC.
R	1	Rd	Root. This bit indicates that this node is the root node. The R bit is reset to 0 by bus reset, and is set to 1 during tree-ID if this node becomes root.
CPS	1	Rd	Cable-power status. This bit indicates the state of the CPS input terminal. The CPS terminal is normally tied to serial bus cable power through a 400-kΩ resistor. A 0 in this bit indicates that the cable-power voltage has dropped below its threshold for ensured reliable operation.
RHB	1	Rd/Wr	Root-holdoff bit. This bit instructs the PHY to attempt to become root after the next bus reset. The RHB bit is reset to 0 by a hardware reset and is unaffected by a bus reset. If two nodes on a single bus have their root holdoff bit set, then the result is not defined. To prevent two nodes from having their root-holdoff bit set, this bit must only be written using a PHY configuration packet.
IBR	1	Rd/Wr	Initiate bus reset. This bit instructs the PHY to initiate a long (166-µs) bus reset at the next opportunity. Any receive or transmit operation in progress when this bit is set completes before the bus reset is initiated. The IBR bit is reset to 0 after a hardware reset or a bus reset. Care must be exercised when writing to this bit to not change the other bits in this register. It is recommended that whenever possible a bus reset be initiated using the ISBR bit and not the IBR bit.
Gap_Count	6	Rd/Wr	Arbitration gap count. This value sets the subaction (fair) gap, arb-reset gap, and arb-delay times. The gap count can be set either by a write to the register, or by reception or transmission of a PHY_CONFIG packet. The gap count is reset to 3Fh by hardware reset or after two consecutive bus resets without an intervening write to the gap count register (either by a write to the PHY register or by a PHY_CONFIG packet). **It is strongly recommended that this field only be changed using PHY configuration packets.**
Extended	3	Rd	Extended register definition. For the TSB81BA3E, this field is 111b, indicating that the extended register set is implemented.
Num_Ports	4	Rd	Number of ports. For the TSB81BA3E, this field indicates the number of ports implemented in the PHY. This field is 3.
PHY_Speed	3	Rd	PHY speed capability. For the TSB81BA3E, this field is no longer used. This field is 111b. Speeds for 1394b PHYs must be checked on a port-by-port basis.

Table 5. Base Register Field Descriptions (continued)

FIELD	SIZE	TYPE	DESCRIPTION
Delay	4	Rd	PHY repeater data delay. This field indicates the worst-case repeater data delay of the PHY, expressed as 144+ (delay × 20) ns. For the TSB81BA3E, this field is 02h. This value is the repeater delay for the S400B case, which is slower than the S800B or 1394a cases. Since the IEEE 1394B−2002 Std Phy register set only has a single field for the delay parameter, the slowest value is used. If a network uses only S800B or 1394a connections, then a delay value of 00h may be used. The worst case Phy repeater delay is 197 ns for S400B and 127 ns for S800B cable speeds (trained, raw bit speed).
LCtrl	1	Rd/Wr	Link-active status control. This bit controls the indicated active status of the LLC reported in the self-ID packet. The logical AND of this bit and the LPS active status is replicated in the L field (bit 9) of the self-ID packet. The LLC bit in the node self-ID packet is set active only if both the LPS input is active and the LCtrl bit is set. The LCtrl bit provides a software-controllable means to indicate the LLC self-ID active status in lieu of using the LPS input terminal. The LCtrl bit is set to 1 by hardware reset and is unaffected by bus reset. NOTE: The state of the PHY-LLC interface is controlled solely by the LPS input, regardless of the state of the LCtrl bit. If the PHY-LLC interface is operational as determined by the LPS input being active, then received packets and status information continue to be presented on the interface, and any requests indicated on the LREQ input are processed, even if the LCtrl bit is cleared to 0.
C	1	Rd/Wr	Contender status. This bit indicates that this node is a contender for the bus or isochronous resource manager. This bit is replicated in the c field (bit 20) of the self-ID packet. This bit is set to 0 on hardware reset. After hardware reset, this bit can only be set via a software register write. This bit is unaffected by a bus reset.
Jitter	3	Rd	PHY repeater jitter. This field indicates the worst-case difference between the fastest and slowest repeater data delay, expressed as (jitter+1) × 20 ns. For the TSB81BA3E, this field is 0.
Pwr_Class	3	Rd/Wr	Node power class. This field indicates this node power consumption and source characteristics and is replicated in the pwr field (bits 21–23) of the self-ID packet. This field is reset to the state specified by the PC0-PC2 input terminals upon a hardware reset, and is unaffected by a bus reset. See Table 3.
WDIE	1	Rd/Wr	Watchdog interrupt enable. This bit, if set to 1, enables the port event interrupt (PIE) bit to be set when resume operations begin on any port, or when any of the CTOI, CPSI, or STOI interrupt bits are set and the link interface is nonoperational. This bit is reset to 0 by hardware reset and is unaffected by bus reset.
ISBR	1	Rd/Wr	Initiate short arbitrated bus reset. This bit, if set to 1, instructs the PHY to initiate a short (1.3 μs) arbitrated bus reset at the next opportunity. This bit is reset to 0 by a bus reset. It is recommended that short bus reset is the only reset type initiated by software. IEC 61883-6 requires that a node initiate short bus resets to minimize any disturbance to an audio stream. NOTE: Legacy IEEE Std 1394-1995-compliant PHYs are not capable of performing short bus resets. Therefore, initiation of a short bus reset in a network that contains such a legacy device results in a long bus reset being performed.
CTOI	1	Rd/Wr	Configuration time-out interrupt. This bit is set to 1 when the arbitration controller times out during tree-ID start and might indicate that the bus is configured in a loop. This bit is reset to 0 by hardware reset or by writing a 1 to this register bit. If the CTOI and WDIE bits are both set and the LLC is or becomes inactive, then the PHY activates the LKON/DS2 output to notify the LLC to service the interrupt. NOTE: If the network is configured in a loop, then only those nodes that are part of the loop generate a configuration time-out interrupt. All other nodes instead time out waiting for the tree-ID and/or self-ID process to complete and then generate a state time-out interrupt and bus reset. This bit is only set when the bus topology includes 1394a nodes; otherwise, 1394b loop healing prevents loops from being formed in the topology.
CPSI	1	Rd/Wr	Cable power status interrupt. This bit is set to 1 when the CPS input transitions from high to low, indicating that cable power might be too low for reliable operation. This bit is reset to 1 by hardware reset. It can be cleared by writing a 1 to this register bit. If the CPSI and WDIE bits are both set and the LLC is or becomes inactive, then the PHY activates the LKON/DS2 output to notify the LLC to service the interrupt.
STOI	1	Rd/Wr	State time-out interrupt. This bit indicates that a state time-out has occurred (which also causes a bus reset to occur). This bit is reset to 0 by hardware reset or by writing a 1 to this register bit. If the STOI and WDIE bits are both set and the LLC is or becomes inactive, then the PHY activates the LKON/DS2 output to notify the LLC to service the interrupt.

Table 5. Base Register Field Descriptions (continued)

FIELD	SIZE	TYPE	DESCRIPTION
PEI	1	Rd/Wr	Port event interrupt. This bit is set to 1 on any change in the connected, bias, disabled, or fault bits for any port for which the port interrupt enable (PEI) bit is set. Additionally, if the resuming port interrupt enable (WDIE) bit is set, then the PEI bit is set to 1 at the start of resume operations on any port. This bit is reset to 0 by hardware reset, or by writing a 1 to this register bit.
EAA	1	Rd/Wr	Enable accelerated arbitration. This bit enables the PHY to perform the various arbitration acceleration enhancements defined in 1394a-2000 (ACK-accelerated arbitration, asynchronous fly-by concatenation, and isochronous fly-by concatenation). This bit is reset to 0 by hardware reset and is unaffected by bus reset. This bit has no effect when the device is operating in 1394b mode. NOTE: The use of accelerated arbitration is completely compatible with networks containing legacy IEEE Std 1394-1995 PHYs. The EAA bit is set only if the attached LLC is 1394a-2000-compliant. If the LLC is not 1394a-2000 or 1394b-2002-compliant, then the use of the arbitration acceleration enhancements can interfere with isochronous traffic by excessively delaying the transmission of cycle-start packets.
EMC	1	Rd/Wr	Enable multispeed concatenated packets. This bit enables the PHY to transmit concatenated packets of differing speeds in accordance with the protocols defined in 1394a-2000. This bit is reset to 0 by hardware reset and is unaffected by bus reset. This bit has no effect when the device is operating in 1394b mode. NOTE: The use of multispeed concatenation is completely compatible with networks containing legacy IEEE Std 1394-1995 PHYs. However, use of multispeed concatenation requires that the attached LLC be 1394a-2000 or 1394b-2002-compliant.
Max Legacy SPD	3	Rd	Maximum legacy-path speed. This field holds the maximum speed capability of any legacy node (1394a-2000 or 1394-1995-compliant) as indicated in the self-ID packets received during bus initialization. Encoding is the same as for the PHY_SPEED field (but limited to S400 maximum).
BLINK	1	Rd	Beta-mode link. This bit indicates that a Beta-mode-capable link is attached to the PHY. This bit is set by the BMODE input terminal on the TSB81BA3E.
Bridge	2	Rd/Wr	This field controls the value of the bridge (brdg) field in self-ID packet. The power reset value is 0. Details for when to set these bits are specified in the IEEE 1394.1 bridging specification.
Page_Select	3	Rd/Wr	Page_Select. This field selects the register page to use when accessing register addresses 8 through 15. This field is reset to 0 by a hardware reset and is unaffected by bus reset.
Port_Select	4	Rd/Wr	Port_Select. This field selects the port when accessing per-port status or control (for example, when one of the port status/control registers is accessed in page 0). Ports are numbered starting at 0. This field is reset to 0 by hardware reset and is unaffected by bus reset.

The port status page provides access to configuration and status information for each of the ports. The port is selected by writing 0 to the Page_Select field and the desired port number to the Port_Select field in base register 7. Table 6 shows the configuration of the port status page registers, and Table 7 gives the corresponding field descriptions. If the selected port is unimplemented, then all registers in the port status page are read as 0.

Table 6. Page 0 (Port Status) Register Configuration

ADDRESS	BIT POSITION							
	0	1	2	3	4	5	6	7
1000	Astat		Bstat		Ch	Con	RxOK	Dis
1001	Negotiated_speed			PIE	Fault	Standby_fault	Disscrm	B_Only (0)
1010	DC_connected	Max_port_speed			LPP	Cable_speed		
1011	Connection_unreliable	Reserved			Beta_mode	Reserved		
1100	Port_error							
1101	Reserved					Loop_disable	In_standby	Hard_disable
1110	Reserved							
1111	Reserved							

Table 7. Page 0 (Port Status) Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
Astat	2	Rd	TPA line state. This field indicates the instantaneous TPA line state of the selected port, encoded as follows: **Code** **Arb Value** 11 Z 01 1 10 0 00 invalid
Bstat	2	Rd	TPB line state. This field indicates the TPB line state of the selected port. This field has the same encoding as the Astat field.
Ch	1	Rd	Child/parent status. A 1 indicates that the selected port is a child port. A 0 indicates that the selected port is the parent port. A disconnected, disabled, or suspended port is reported as a child port. The Ch bit is invalid after a bus reset until tree-ID has completed.
Con	1	Rd	Debounced port connection status. This bit indicates that the selected port is connected. The connection must be stable for the debounce time of approximately 341 ms for the Con bit to be set to 1. The Con bit is reset to 0 by hardware reset and is unaffected by bus reset. NOTE: The Con bit indicates that the port is physically connected to a peer PHY, but this does not mean that the port is necessarily active. For 1394b-coupled connections, the Con bit is set when a port detects connection tones from the peer PHY and operating-speed negotiation is completed.
RxOK	1	Rd	Receive OK. In 1394a-2000 mode this bit indicates the reception of a debounced TPBias signal. In Beta mode, this bit indicates the reception of a continuous electrically valid signal. Note: RxOK is set to false during the time that only connection *tones* are detected in Beta mode.
Dis	1	Rd/Wr	Port disabled control. If this bit is 1, then the selected port is disabled. The Dis bit is reset to 0 by hardware reset (all ports are enabled for normal operation following hardware reset). The Dis bit is not affected by bus reset. When this bit is set, the port cannot become active; however, the port still tones, but does not establish an active connection.
Negotiated_speed	3	Rd	Indicates the maximum speed negotiated between this PHY port and its immediately connected port. The encoding is as for Max_port_speed. It is set during connection when in Beta mode or to a value established during self-ID when in 1394a-2000 mode.
PIE	1	Rd/Wr	Port-event-interrupt enable. When this bit is 1, a port event on the selected port sets the port-event-interrupt (PEI) bit and notifies the link. This bit is reset to 0 by a hardware reset and is unaffected by bus reset.
Fault	1	Rd/Wr	Fault. This bit indicates that a resume fault or suspend fault has occurred on the selected port, and that the port is in the suspended state. A resume-fault occurs when a resuming port fails to detect incoming cable bias from its attached peer. A suspend fault occurs when a suspending port continues to detect incoming cable bias from its attached peer. Writing 1 to this bit clears the Fault bit to 0. This bit is reset to 0 by hardware reset and is unaffected by bus reset.
Standby_fault	1	Rd/Wr	This bit is set to 1 if an error is detected during a standby operation and cleared on exit from the standby state. A write of 1 to this bit or receipt of the appropriate remote command packet clears it to 0. When this bit is cleared, standby errors are cleared.
Disscrm	1	Rd/Wr	Disable scrambler. If this bit is set to 1, then the data sent during packet transmission is not scrambled.
B_Only	1	Rd	Beta-mode operation only. For the TSB81BA3E, this bit is set to 0 for all ports.
DC_connected	1	Rd	If this bit is set to 1, the port has detected a dc connection to the peer port by means of a 1394a-style connect-detect circuit.

Table 7. Page 0 (Port Status) Register Field Descriptions (continued)

FIELD	SIZE	TYPE	DESCRIPTION
Max_port_speed	3	Rd/Wr	Max_port_speed The maximum speed at which a port is allowed to operate in Beta mode. The encoding is: 000 = S100 001 = S200 010 = S400 011 = S800 100 = S1600 101 = S3200 110 = reserved 111 = reserved An attempt to write to the register with a value greater than the hardware capability of the port results in the maximum value that the port is capable of being stored in the register. The port uses this register only when a new connection is established in the Beta mode or when a port is programmed as a Beta-only port. When a port is programmed as a bilingual port, it is fixed at S400 for the Beta speed and is not updated by a write to this register. The power reset value is the maximum speed capable of the port. Software can modify this value to force a port to train at a lower-than-maximum speed (when in a Beta-only mode), but no lower than the minimum speed.
LPP(Local_plug_present)	1	Rd	This flag is set permanently to 1.
Cable_speed	3	Rd	This variable is set to the maximum speed that the port is capable of. The encoding is the same as for Max_port_speed.
Connection_unreliable	1	Rd/Wr	If this bit is set to 1, then a Beta-mode speed negotiation has failed or synchronization has failed. A write of 1 to this field resets the value to 0.
Beta_mode	1	Rd	Operating in Beta mode. If this bit is 1, the port is operating in Beta mode; it is equal to 0 otherwise (that is, when operating in 1394a-2000 mode, or when disconnected). If Con is 1, RxOK is 1, and Beta_mode is 0, then the port is active and operating in the 1394a-2000 mode.
Port_error	8	Rd/Wr	Incremented when the port receives an invalid codeword, unless the value is already 255. Cleared when read (including being read by means of a remote access packet). Intended for use by a single bus-wide diagnostic program.
Loop_disable	1	Rd	This bit is set to 1 if the port has been placed in the loop-disable state as part of the loop-free build process (the PHYs at either end of the connection are active, but if the connection itself were activated, then a loop would exist). Cleared on bus reset and on disconnection.
In_standby	1	Rd	This bit is set to 1 if the port is in standby power-management state.
Hard_disable	1	Rd/Wr	No effect unless the port is disabled. If this bit is set to 1, the port does not maintain connectivity status on an ac connection when disabled. The values of the Con and RxOK bits are forced to 0. This flag can be used to force renegotiation of the speed of a connection. It can also be used to place the device into a lower-power state because when hard-disabled, a port no longer tones to maintain 1394b ac-connectivity status.

The vendor identification page identifies the vendor/manufacturer and compliance level. The page is selected by writing 1 to the Page_Select field in base register 7. Table 8 shows the configuration of the vendor identification page, and Table 9 shows the corresponding field descriptions.

Table 8. Page 1 (Vendor ID) Register Configuration

ADDRESS	BIT POSITION							
	0	1	2	3	4	5	6	7
1000	Compliance							
1001	Reserved							
1010	Vendor_ID0							
1011	Vendor_ID1							
1100	Vendor_ID2							
1101	Product_ID0							
1110	Product_ID1							
1111	Product_ID2							

Table 9. Page 1 (Vendor ID) Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
Compliance	8	Rd	Compliance level. For the TSB81BA3E, this field is 02h, indicating compliance with the 1394b-2002 specification.
Vendor_ID	24	Rd	Manufacturer's organizationally unique identifier (OUI). For the TSB81BA3E, this field is 08_00_28h (Texas Instruments) (the MSB is at register address 1010b).
Product_ID	24	Rd	Product identifier. For the TSB81BA3E, this field can be either 83_13_07h (the MSB is at register address 1101b).

The vendor-dependent page provides access to the special control features of the TSB81BA3E, as well as configuration and status information used in manufacturing test and debug. This page is selected by writing 7 to the Page_Select field in base register 7. Table 10 shows the configuration of the vendor-dependent page and Table 11 shows the corresponding field descriptions.

Table 10. Page 7 (Vendor-Dependent) Register Configuration

ADDRESS	BIT POSITION							
	0	1	2	3	4	5	6	7
1000	Reserved						Reserved	
1001	Reserved for test							
1010	Reserved for test							
1011	Reserved for test							
1100	Reserved for test							
1101	Reserved for test							
1110	SWR	Reserved for test						
1111	Reserved for test							

Table 11. Page 7 (Vendor-Dependent) Register Field Descriptions

FIELD	SIZE	TYPE	DESCRIPTION
SWR	1	Rd/Wr	Software hard reset. Writing a 1 to this bit forces a hard reset of the PHY (same effect as momentarily asserting the RESET terminal low). This bit is always read as a 0.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TSB81BA3E provides the digital and analog transceiver functions needed to implement a three-port node in a cable-based IEEE 1394 network. Each cable port incorporates two differential line Interface (HCI) Requirements transceivers. The transceivers include circuitry to monitor the line conditions as needed for determining connection status, for initialization and arbitration, and for packet reception and transmission.

9.2 Typical Application

A common application of the TSB81BA3E is a three-port 1394 transceiver, it can be configured port-basis for data strobe only, beta mode or bilingual modes.

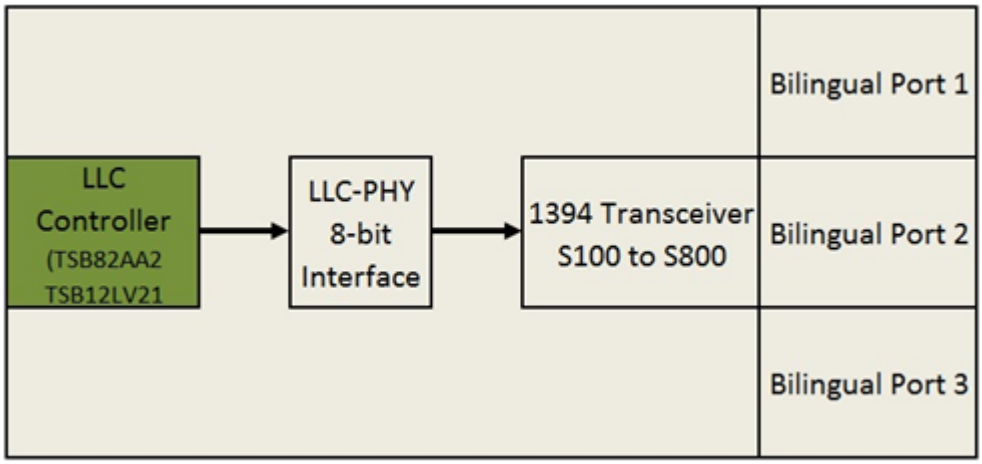


Figure 9. 3-Port 1394 Transceiver in 1394b Mode

Typical Application (continued)

9.2.1 Design Requirements

For this design example, use the parameters shown in Table 12.

Table 12. Design Parameters

PARAMETER	EXAMPLE VALUE
PHY POWER	3.3 V
LLC Controller	TSB82AA2
Crystal	24.576 MHz
Downstream Ports	3- 1394 Bilingual
Power Class	PC[0:2] = 100
Bus Power	12 V

9.2.2 Detailed Design Procedure

9.2.2.1 Port Termination for a 1394 Bilingual Port

The TPA and TPB lines require termination as illustrated in the following figure, the 1394 node connecting to this external port shall have the same terminations on its ports.

When configuring the TSB81BA3E port to be data-strobe only the TPBIAS terminal can be left unconnected.

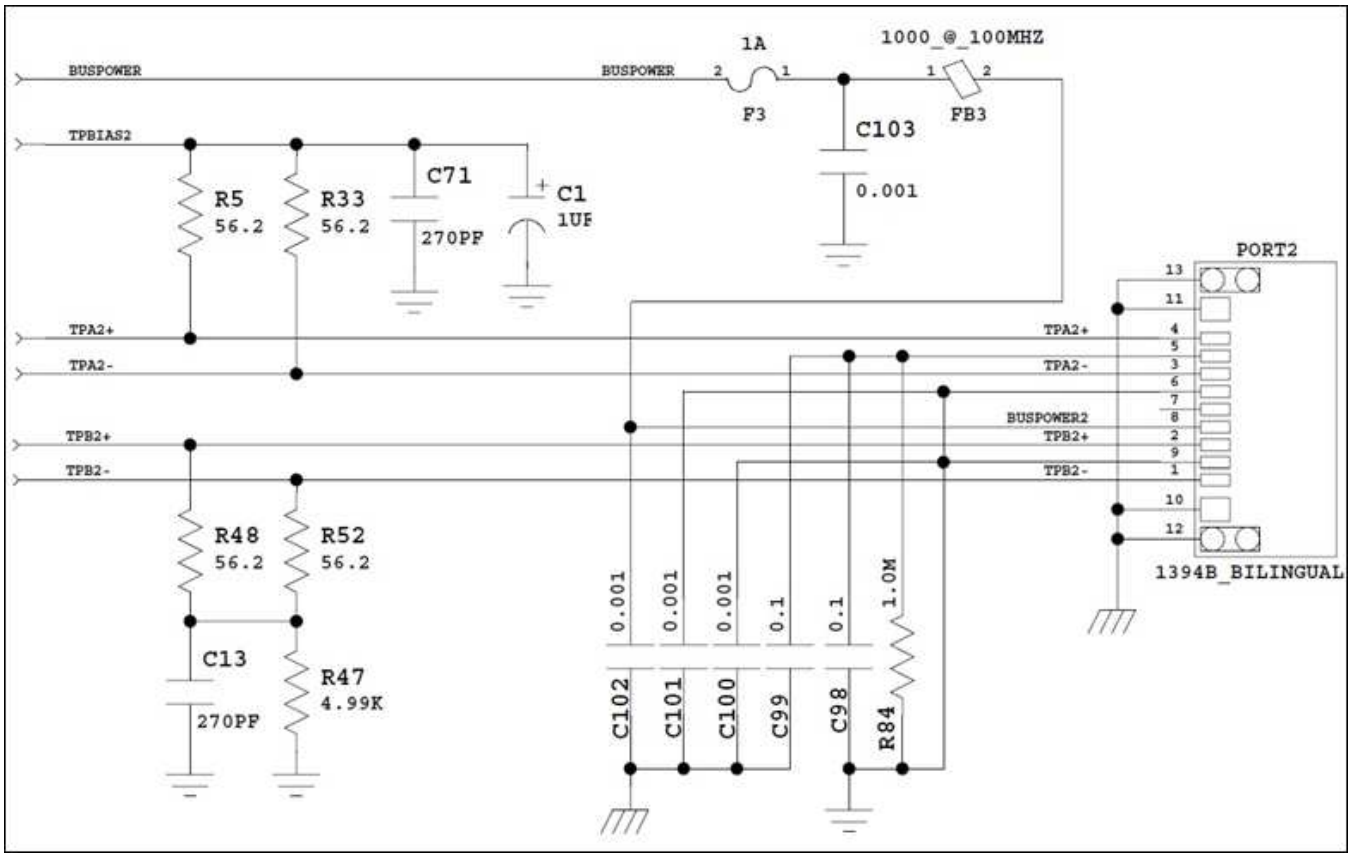


Figure 10. Port Termination

9.2.2.2 PHY-LINK Interface

The PHY-link interface of the TSB81BA3E can follow either the 1394a protocol or the 1394b protocol. When using any 1394-1995 or 1394a links such as the TSB12LV01B or the TSB12LV32, the PHY-link interface has to be in the 1394a protocol. In this case, the BMODE pin has to be tied low to GND.

When using any 1394b link such as the TSB82AA2, the PHY-link interface has to be in the 1394b protocol. In this case, the BMODE pin is tied high. The BMODE pin only sets the mode of operation of the PHY-link interface; it does not set the mode of operation of the cable interface. No isolation is implemented in this schematic.

The PHY and link operate off of the same ground plane. To reduce EMI emissions and reduce reflections on the PCLK line, a series-damping resistor is recommended. The schematic shows a 0-Ω resistor, which is essentially a placeholder on the board. To reduce EMI, a 22-Ω resistor on the PCLK line is recommended. This resistor should be placed as close to the PHY as possible. Its value can be adjusted to reduce emissions. By slowing down the edge rates on PCLK, this 22-Ω resistor significantly reduces reflections that may occur when the distance between the PHY and link is large (greater than 4 inches in this case).

The Link Request signal (LREQ) is input to the PHY from the link. The link uses this to initiate a service request to the PHY. When the BMODE pin is deasserted, the IEEE 1394b-2002 BOSS arbitration is disabled and the LREQ request stream follows the 1394a specification.

If a power down option control for PD is not implemented, the PD pin on the PHY (pin 77) should be tied to ground through a 1-kΩ resistor to keep the PHY enabled.

10 Power Supply Recommendations

Another means to minimize EMI emissions is to add decoupling capacitors with a ferrite bead at PLLVDD pin and DVDD pins of the chip. This array should be as close as possible to the chip in order to minimize the inductance of the line and minimize noise contributions to the system, a suggested example is shown in Figure 11(a) and Figure 11(b). In the case of DVDD pins, it is recommended to tie them up to a single low impedance point in the board and then adding the decoupling capacitors in addition to the ferrite bead. This array of caps and ferrite bead improve EMI and Jitter performance. Both EMI and Jitter should be taken into account before altering the configuration.

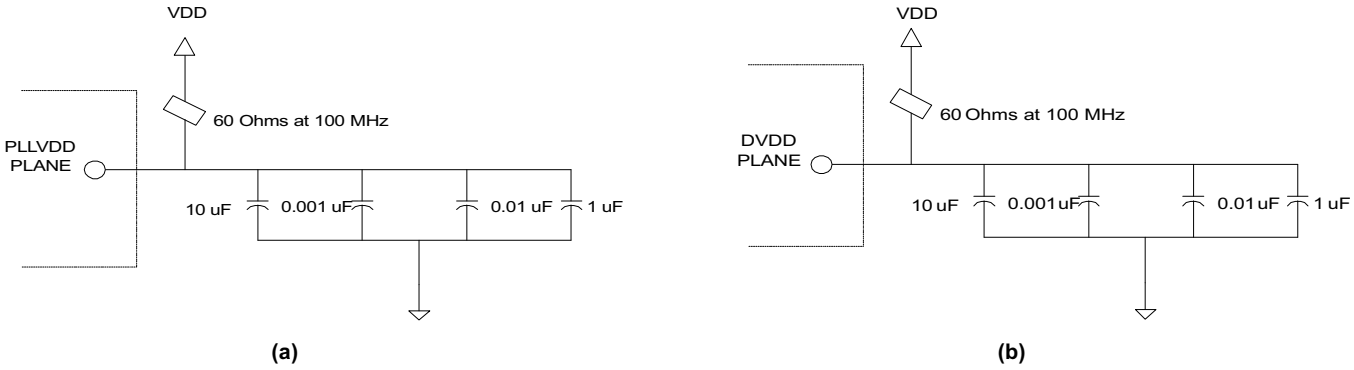


Figure 11. Suggested Array at PLLVDD and DVDD in Order to Minimize EMI

11 Layout

11.1 Layout Guidelines

Put pads in for all components in prototype boards. When testing prototype boards for EMI and ESD, some of the following components may not be required:

- The 1394 connector gasket between chassis GND, 1394 connector shield, and metal bracket on PCB board (for example on a PCI add-in card).
- The ferrite on the cable V- ground pin (socket pin 2).
- The ferrite on the cable V+ power pin (socket pin 1).

11.1.1 Board Stackup

Because of the high frequencies associated with 1394, a 1394 board with at least four layers is recommended; two signal layers separated by a ground and power layer (See Figure 12).

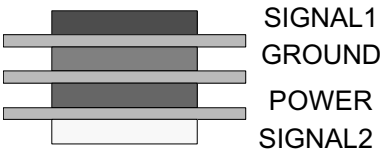


Figure 12. Four-Layer Board Stackup

The majority of signal traces should be run on a single layer, preferably SIGNAL1. Immediately next to this layer should be the GND plane which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used (see Section 3.3). Minimizing the number of signal vias could reduce EMI due to a reduction in inductance at high frequencies.

11.1.2 Digital and Analog Partitioning

If separate power planes are used, they must be tied together at one point through a low impedance bridge or preferably through a ferrite bead (See Figure 13). Care must be taken to capacitively de-couple each power rail close to the device.

The analog ground (AGND), digital ground (DGND), and Phase Locked Loop (PLL) ground (PLLGND) must be tied together to the low impedance circuit board ground plane.

Layout Guidelines (continued)

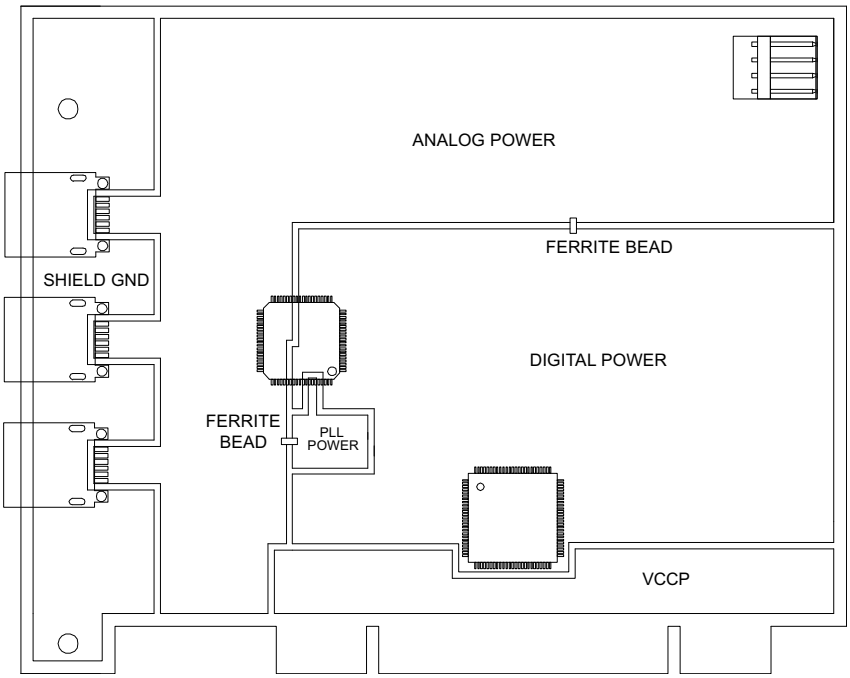


Figure 13. A Image Plane Partition, Route Signal Carefully

11.1.3 Image Planes

An image plane is a layer of copper (voltage plane or ground plane), physically adjacent to a signal routing plane. Use of image planes provides a low impedance, shortest possible return path for RF currents. For a 1394 board the best image plane is the ground plane, since on most designs a common ground can be used for both analog and digital circuits. Care should be taken not to route traces such that they cross from one plane to the other, as this can cause a broken RF return path resulting in an EMI radiating loop (See Figure 7). This is important for higher frequency or repetitive signals. Therefore it is best to run all clock signals on the signal plane above a solid ground plane (on a multi-layer board). Avoid crossing the image power or ground plane boundaries with high speed clock signal traces immediately above or below the separated planes. This also holds true for the twisted pair signals (TPA, TPB). Special care should be applied to the LPS and LKON signals as these do not always route easily on a single layer.

Any unused area of the top and bottom signal layers of the PCB can be filled with copper that is connected to the ground plane through vias.

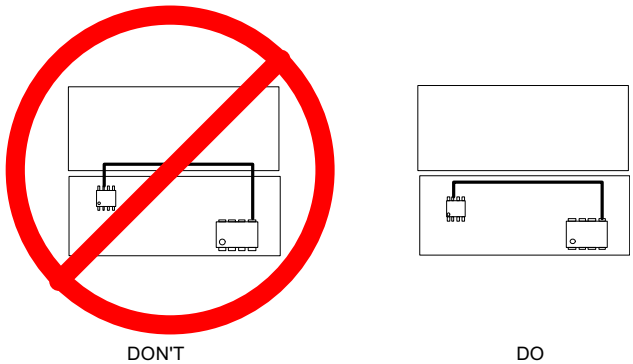


Figure 14. Do Not Cross Image Plane Boundaries

Layout Guidelines (continued)

Care should also be taken not to overlap planes that do not reference each other. For example do not overlap a digital power plane with an analog power plane as this will produce a capacitance between the overlapping area which could pass RF emissions from one plane to the other. See Figure 15.

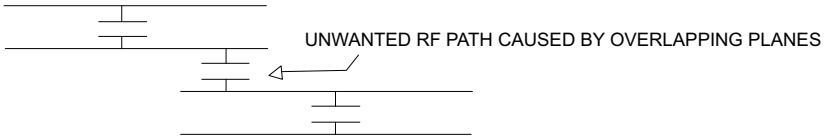


Figure 15. Do Not Overlap Planes

Avoid image plane violations. Traces that route over a slot in an image plane results in a possible RF return loop. See Figure 16.

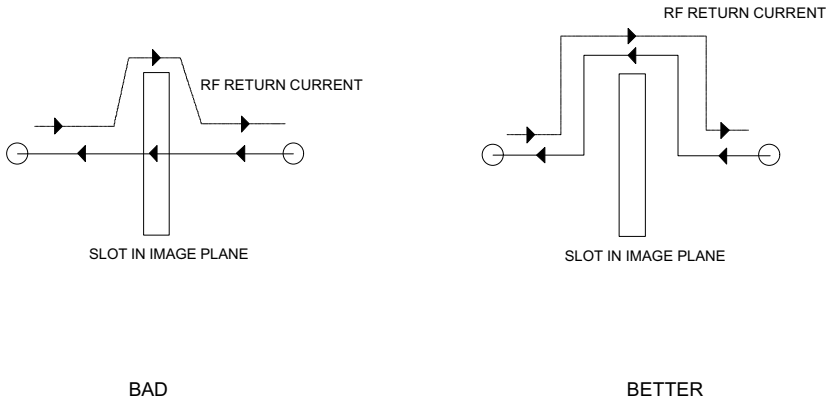


Figure 16. Do Not Violate Image Planes

11.1.4 Parts Placement

Components should be placed on the board such that the traces coming from a component will always be above its corresponding image plane. The PHY should also be placed close to the link to reduce the trace length of the PHY/link interface. For less radiated EMI, place the PHY device as far away from the 1394 connector (termination network should be close to the PHY) as is practical. Balance this against keeping the twisted pair trace lengths short (for signal integrity), keeping the PHY-Link interface traces short (for signal integrity and EMI) and keeping the PHY away from any switching power supply.

11.1.5 Decoupling Capacitors

Properly used decoupling caps keep RF energy from being injected into the power planes from high frequency components. Decoupling capacitors also provides a localized source of pulsed DC power for device or components. This reduces peak current surges from propagating across the board. Use 0.1 µF and 0.001 µF decoupling caps on the PHY and link (For PLLVDD see *Power Supply Recommendations*. Minimize the trace length between the decoupling capacitor and the corresponding power pins on the device. Also minimize the trace length from the capacitor pad to the power or ground plane. See Figure 17.

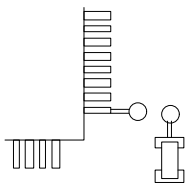


Figure 17. Decoupling Capacitors

Layout Guidelines (continued)

11.1.6 3W Rule for SCLK

When routing the SCLK trace from the PHY to link, try to use the 3W spacing rule. The distance from the center of the SCLK trace to the center of any adjacent signal trace should be at least three times the width of the SCLK trace. SCLK is a 49.152 MHz clock with a fast rise time. Using the 3W rule will cut down on crosstalk between traces. In general, leave space between each of the traces running from the PHY to link. Avoid using right angles when routing traces to minimize the routing distance and impedance discontinuities.

For further protection from crosstalk, run guard traces beside the SCLK signal from PHY to Link (GND pin to GND pin if possible). This is to lessen clock signal coupling onto the other PHYLink interface traces near it and thus radiating the clock signal from more antennas. See Figure 18.

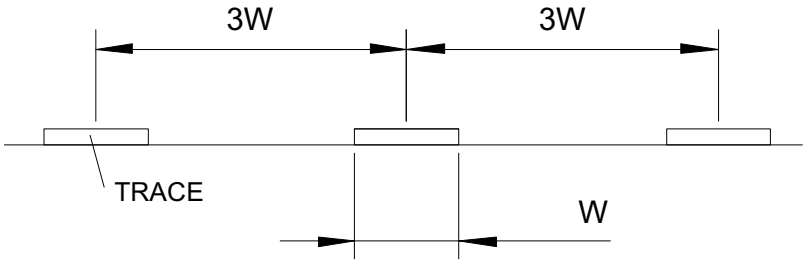


Figure 18. 3W Rule

12 Device and Documentation Support

12.1 Device Support

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

13.1 Designing With PowerPAD™ Devices (PFP Package Only)

The TSB81BA3E is housed in a high performance, thermally enhanced, 80-terminal PFP PowerPAD™ package. Use of the PowerPAD™ package does not require any special considerations except to note that the PowerPAD™, which is an exposed die pad on the bottom of the device, is a metallic thermal and electrical conductor. Therefore, if not implementing PowerPAD™ PCB features, the use of solder masks (or other assembly techniques) may be required to prevent any inadvertent shorting by the exposed PowerPAD™ of connection etches or vias under the package. The recommended option, however, is to not run any etches or signal vias under the device, but to have only a grounded thermal land as explained below. Although the actual size of the exposed die pad may vary, the maximum size required for the keepout area for the 80-terminal PFP PowerPAD™ package is 10 mm × 10 mm. The actual PowerPAD™ size for the TSB81BA3E is 6 mm × 6 mm.

It is recommended that there be a thermal land, which is an area of solder-tinned-copper, underneath the PowerPAD™ package. The thermal land varies in size, depending on the PowerPAD™ package being used, the PCB construction, and the amount of heat that needs to be removed. In addition, the thermal land may or may not contain numerous thermal vias depending on PCB construction.

Other requirements for thermal lands and thermal vias are detailed in the Texas Instruments *PowerPAD™ Thermally Enhanced Package* application report (SLMA002) available via the Texas Instruments web page at http://www.ti.com.

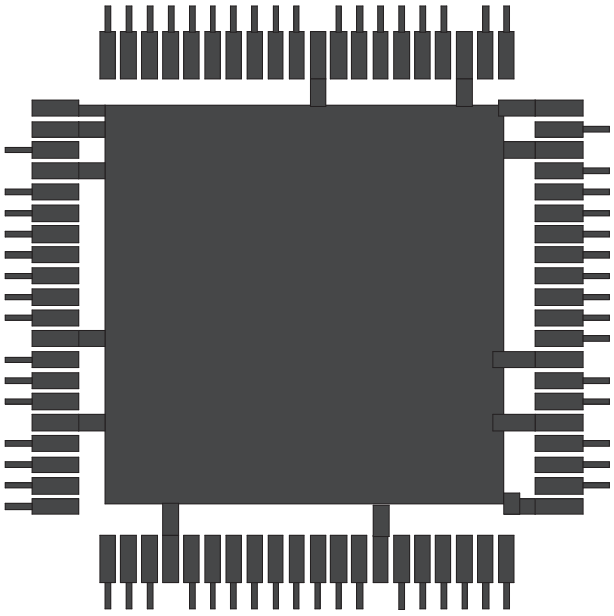


Figure 19. Example of a Thermal Land for the TSB81BA3E PHY

The thermal land must be grounded to the low-impedance ground plane of the device. This improves not only thermal performance but also the electrical grounding of the device. It is also recommended that the device ground terminal landing pads be connected directly to the grounded thermal land. The land size ought to be as large as possible without shorting the device signal terminals. The thermal land can be soldered to the exposed thermal pad using standard reflow soldering techniques.

While the thermal land may be electrically floated and configured to remove heat to an external heat sink, it is recommended that the thermal land be connected to the low impedance ground plane for the device. More information may be obtained from the TI application note *PHY Layout* (SLLA020).

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TSB81BA3EIPFP	Obsolete	Production	HTQFP (PFP) | 80	-	-	Call TI	Call TI	-40 to 85	TSB81BA3EI
TSB81BA3EIZAJ	Obsolete	Production	NFBGA (ZAJ) | 168	-	-	Call TI	Call TI	-40 to 85	TSB81BA3EI
TSB81BA3EPFP	Obsolete	Production	HTQFP (PFP) | 80	-	-	Call TI	Call TI	0 to 70	TSB81BA3E
TSB81BA3EZAJ	Obsolete	Production	NFBGA (ZAJ) | 168	-	-	Call TI	Call TI	0 to 70	TSB81BA3E

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

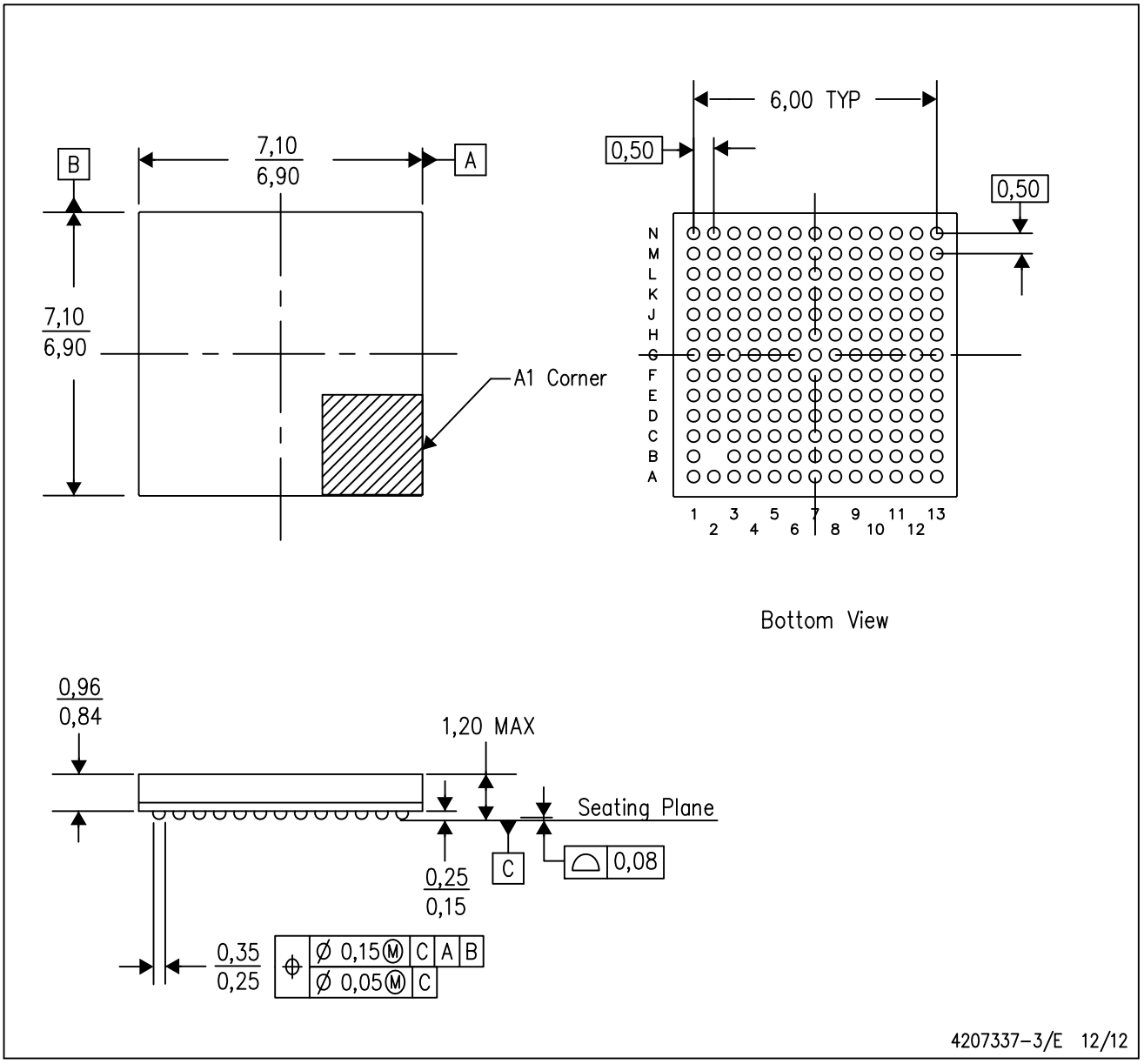
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

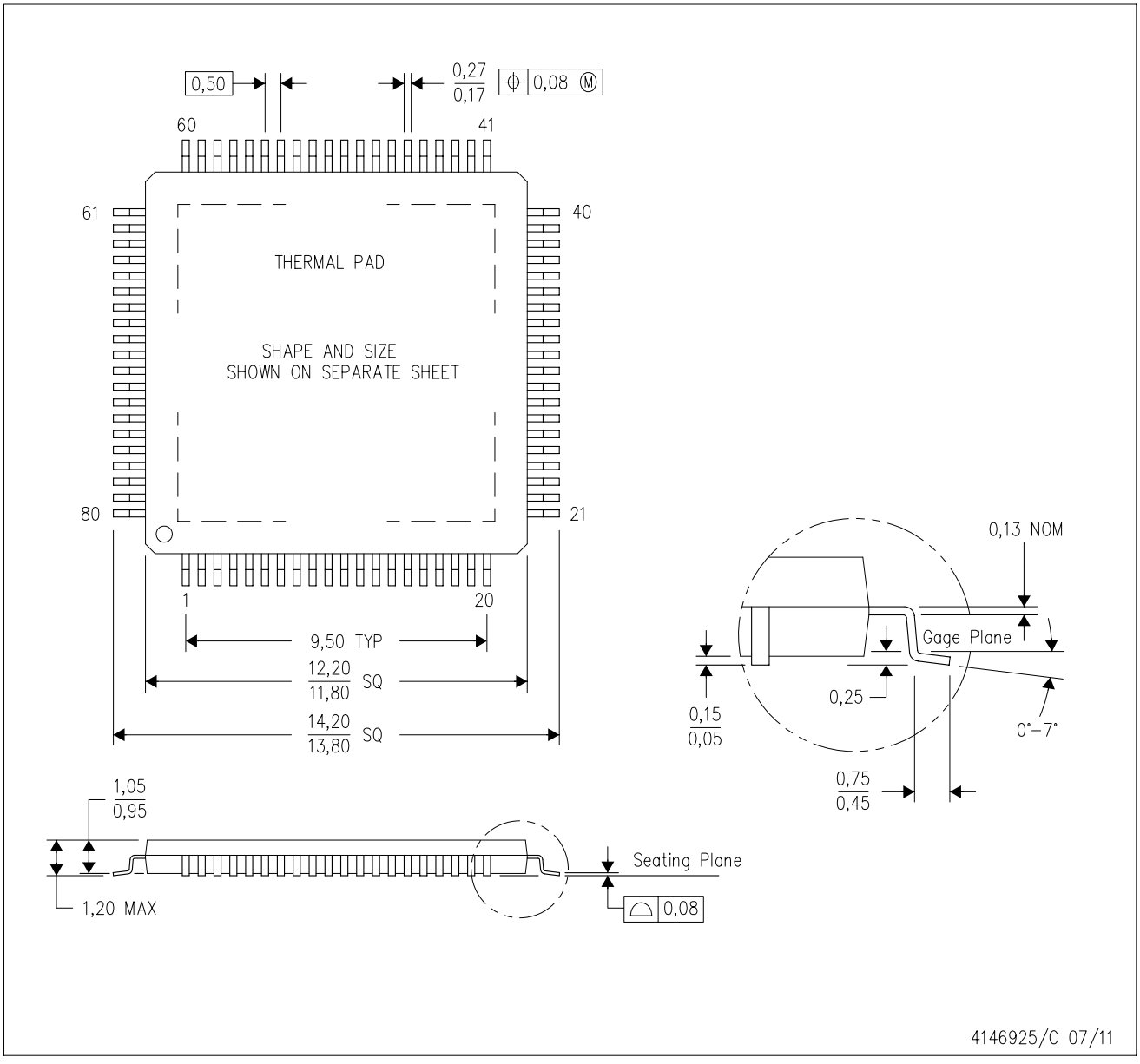
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

ZAJ (S–PBGA–N168) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This is a Pb–free solder ball design.

PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

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