

# TMS320C6671/72/74/78

## High-performance multicore fixed- and floating-point DSPs



### Product bulletin

For developers of applications such as mission critical, medical imaging, test and automation and high-performance computing, TI's TMS320C66x generation of DSPs offer the industry's first 10-GHz DSP with unsurpassed performance and a variety of on-chip resources that can be rapidly and effectively deployed to meet the most demanding requirements. Based on TI's KeyStone multicore architecture, the TMS320C6671, TMS320C6672, TMS320C6674 and TMS320C6678 DSPs come with one, two, four or eight cores, respectively.

Each high-speed core (1.5 GHz, 1.25 GHz or 1 GHz) is a true fixed- and floating-point DSP. In fact, the 40-nm C66x devices are the fastest integrated fixed- and floating-point DSPs and the fastest floating-point DSP available today. This high level of integration reduces software development cycles significantly, speeding new systems to market in a fraction of the time. And once deployed, these fixed- and floating-point capable C66x DSPs will be easy to upgrade from one, two-, four- or eight-core versions and effectively maintain in the field.

The C66x devices were designed to be backwards code compatible with TI's previous generation C6000™ fixed- and floating-point DSP cores, ensuring software portability and shortened software development cycles for applications migrating to faster hardware.

### **Slashing time to market**

The new C66x DSP generation features a number of breakthrough innovations that reduce an application's hardware and software development times while enabling the delivery of new products to market quickly.

For example, having access to fully integrated fixed and floating point processors reduces dramatically – from months to days – the time it would typically take to develop software on separate floating- and fixed-point devices. The typical code conversions, normalizing and scaling of algorithms are eliminated entirely from the development process. And performance is improved with greater precision and higher dynamic range. Moreover, the

comprehensive selection of peripherals already integrated on-chip gives developers the high performance and versatile resources they demand without requiring additional development effort. For example, the two lanes of PCI Express (PCIe) Gen II are each rated at either 2.5 or 5 Gbps.

Other I/O options include four lanes of 5-Gbps Full Duplex Serial RapidIO V2.1 (4x1, 2x2 or 1x4), two 10/100-Mbps Ethernet ports and an Ethernet switch, and a host of popular interfaces such as Telecom Serial Interface Ports (TSIP), UART, I2C, SPI, GPIO and 16-Bit External Memory Interface (EMIF-16). For high-speed chip-to-chip interconnection between two C66x devices, an interface

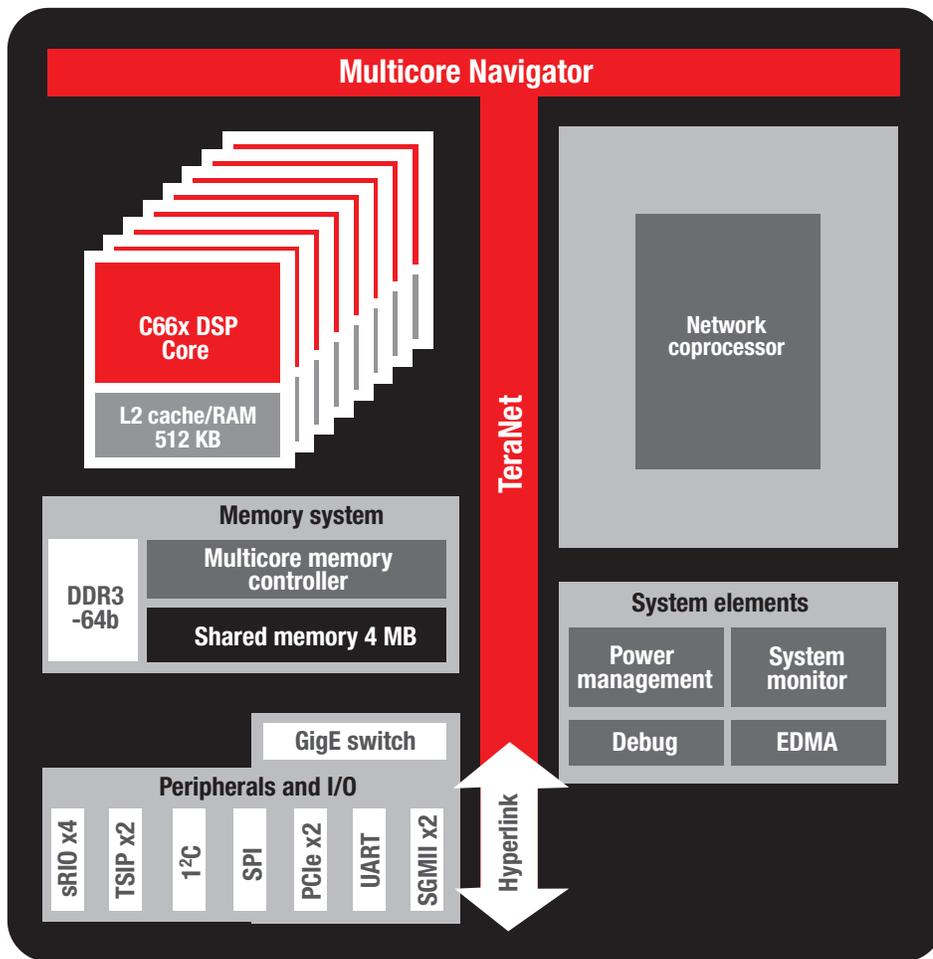
### **Key features**

- Performance – fastest fixed- and floating-point DSP
  - One, two, four or eight cores
  - 1.5 GHz per core (available with two-core device), 1.25 GHz per core (10 GHz total per device), or 1.0 GHz per core
  - 320 GMACs/160 GFLOPs for 1.25 GHz; 256 GMACs/128 GFLOPs for 1 GHz
- Architecture
  - KeyStone architecture
  - Multicore Navigator
  - TeraNet – On-chip switch fabric
- Coprocessor accelerators
  - Packet accelerator
  - Crypto engine
- High-speed input/output (I/O)
  - PCI Express Gen II single & double lanes
  - Serial RapidIO V2.1 x4
  - TSIP x2
  - DDR3-1600 (64b)
  - Hyperlink – chip-to-chip interconnect
- Low power
  - <10 W at 75°C at 1 GHz
  - Dynamic power monitoring
  - SmartReflex™ technology
- Industrial/extended temperature range
  - -40° to 100°C
- Peripherals
  - Ethernet ports SGMII x2
  - UART, I<sup>2</sup>C, SPI, GPIO

to TI's Hyperlink bus offers four lanes at 12.5 Gbps each Full Duplex, which can also be readily integrated into most FPGAs.

### **Target applications**

The unique combination of vast processing power; an innovative multicore architecture



▲ TMS320C6671, TMS320C6672, TMS320C6674 and TMS320C6678 block diagram

that assures lightning-fast data flows on- and off-chip; integrated fixed- and floating-point processing that shortens the typical time-to-market cycle; and many other factors make C66x devices ideal for a wide range of applications. Some of the most prominent of these are:

**Medical imaging** – As with most imaging applications, speed is of the essence for medical imaging. High-performance C66x devices, with an architecture designed to eliminate system bottlenecks and latencies, are ideal for the computationally intensive real-time signal processing typically required in image acquisition, enhancement and reconstruction. Moreover, the simplified programmability of C66x DSPs, with support for both fixed- and floating-point instructions, accelerates the implementation of new and innovative algorithms, while the low-power-per-performance ratio of these devices makes them ideal for

portable and green conscious products.

**Mission critical** – High-performance floating-point capability is essential in many public safety, defense and aerospace applications. In addition, power efficiency combined with reliability and continuity of supply are essential. By leveraging the telecom lifecycles and reliability requirements, the C66x DSPs affordably bring these features to mission critical markets. The industrial temperature range of -40 to 100°C ensures that the multicore processing capabilities of the C66x DSPs will be available when needed in crucial mission critical applications.

**High-performance computing** – High-performance computing has taken on even greater importance with the advent of the Internet and cloud computing. To ensure the responsiveness of networks, online processing nodes and storage systems must have extremely robust processing capabilities and

exceedingly fast data-throughput rates, just two of the qualities of C66x multicore DSPs. When combined with a general processor, these multicore devices can play a pivotal role in offloading compute intensive and multimedia tasks, making the overall system more energy and space efficient.

**Test and automation** – Robotics, visual inspection systems, and electronic test equipment like high-performance wireless and communication testers must be able to process an extremely large volume of data with a high degree of precision. The multicore architecture, as well as the powerful processing power of each individual core, makes the C66x DSPs an ideal fit for test and automation applications.

### KeyStone multicore architecture

TI's KeyStone multicore architecture implemented in C66x generation of DSPs maximizes the throughput of on-chip data flows to eliminate even the most remote possibility of bottlenecks, ensuring that the vast processing power of the devices' cores can be utilized to the maximum. Central to this architecture is TeraNet, a packet-based fabric of high-speed non-blocking channels that delivers as much as 2 terabits per second of on-chip throughput. With TeraNet and an extensive two-layer memory structure, data flows freely and effectively through C66x devices.

Although it provides direct chip-to-chip connectivity for local devices, Hyperlink is also integral to the internal processing architecture of C66x DSPs. Hyperlink is a fast and efficient interface with low protocol overhead and high throughput, running at an aggregate speed of 50 Gbps (four lanes at 12.5 Gbps each). Working in conjunction with Multicore Navigator, Hyperlink transparently dispatches tasks to other local devices where they are executed as if they were being processed on local resources.

In the KeyStone architecture, CorePac is defined as the main processing element in a multicore SoC. CorePac includes the infrastructure that supports the DSP cores, including shared memory and memory controllers. There are three levels of memory in the KeyStone architecture. Each C66x CorePac has its own level-1 program (L1P) and level-1 data (L1D) memory. Additionally, each CorePac

has a local level-2 unified memory (LL2). Each of the local memories can be independently configured as memory-mapped SRAM, cache or a combination of the two.

In addition, the KeyStone architecture includes a shared memory subsystem, comprising internal and external memory connected through the Multicore Shared Memory Controller (MSMC). The MSMC allows the CorePacs to dynamically share the internal and external memories for both program and data. The MSMC internal RAM offers flexibility to programmers by allowing portions to be configured as shared level-2 RAM (SL2) or shared level-3 RAM (SL3). SL2 RAM is cacheable only within the local L1P and L1D caches, while SL3 is additionally cacheable in the local L2 caches.

External memory is connected through the same memory controller as the internal shared memory, rather than to chip system interconnect as has been traditionally been done on embedded processor architectures, providing a fast path for software execution. External memory is always treated as SL3 memory and cacheable in L1 and L2.

The C66x DSPs also feature several innovative coprocessing accelerators that offload processing tasks from the C66x's DSP engines, thereby enabling sustained high application processing rates. The devices also contain a network coprocessor block that consists of a packet accelerator and a security accelerator that work in tandem. The packet accelerator speeds the data flow throughout the core by transferring data to peripheral interfaces such as the Ethernet ports or Serial RapidIO without the involvement of any core's DSP processor. The Security Accelerator provides security processing for a number of popular encryption modes and algorithms, including IPsec, SCTP, SRTP, 3GPP, SSL/TLS and several others.

### **Multicore Navigator**

A breakthrough feature of the C66x generation is TI's innovative Multicore Navigator, which brings single-core simplicity to multicore devices. Multicore Navigator is designed to support hardware-assisted functional acceleration that utilizes an innovative packet-based hardware subsystem in KeyStone devices. With an extensive series of

more than 8,000 queues and a packet-aware DMA controller, it optimizes the packet-based communications of the on-chip cores by practically eliminating all copy operations. The extreme efficiency made possible by Multicore Navigator results in a 100X performance gain in terms of the number of packets communicated per second over previous-generation cores.

The low latencies and zero interrupts ensured by Multicore Navigator, as well as its transparent operations, enable new and more effective programming models such as task dispatchers. Moreover, software development cycles are shortened significantly by several features inherent in Multicore Navigator, including dynamic software partitioning. With Multicore Navigator's "fire and forget" software tasking, developers save significant time and effort by defining repetitive tasks only once, and thereafter accessing and running these tasks automatically without additional coding efforts.

### **Low power across all applications**

TI has long been a leader in the industry in low power consumption; C66x DSPs are no exception. Taking full advantage of TI's groundbreaking low-power SmartReflex™ technology, C66x devices deliver additional power savings from previous-generation DSP devices.

Designated as a SmartReflex device, the C66x multicore DSPs can dynamically adjust supply voltages in response to environmental conditions. Unlike previous generations of DSPs, whose supply voltage would be hardwired into the device during production, C66x devices constantly monitor temperatures on the chip and correlate this with the device's supply voltage. If temperatures drop, the device can automatically adjust its supply voltage downward and achieve another dimension in power savings. TI's C66x multicore devices leverage the numerous power-saving solutions that TI has developed over the years, including several configurable power modes.

### **Tools to get to market fast**

The in-depth hardware and software support for the C66x DSPs is a continuation of the extensive support for which TI has earned a stellar reputation. In addition to evaluation modules (EVMs) for hardware and software evaluations, TI also offers a comprehensive

array of software tools, including the Linux operating system, BIOS, multicore platform software, open GCC tools, Code Composer Studio™ software, a software development kit with a C compiler, an assembly optimizer to simplify programming and scheduling, and a Windows debugger interface for visibility into source-code execution.

In addition, TI offerings include application-specific software libraries, such as those for high performance medical and imaging applications. For instance, developers of medical imaging applications can take advantage of the Embedded Processor Software Toolkit which includes common algorithms and software building blocks found in ultrasound and other types of medical diagnostic systems.

### **For more information**

For more information about the C66x DSPs, visit the TI website at [www.ti.com/c6671](http://www.ti.com/c6671), [www.ti.com/c6672](http://www.ti.com/c6672), [www.ti.com/c6674](http://www.ti.com/c6674) and [www.ti.com/c6678](http://www.ti.com/c6678)

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