OpenMP® Programming for KeyStone Multicore Processors

Texas Instruments offers support for the OpenMP API in its KeyStone multicore architecture. The KeyStone architecture supports heterogeneous programming as well as the integration of TI's fixed- and floating-point TMS320C66x digital signal processor (DSP) cores and ARM® Cortex™-A15 MPcore™ processors. In addition, support for key architecture elements such as Multicore Navigator and Multicore Shared Memory Controller, provides optimum multicore entitlement for applications. For the DSPs, TI has integrated OpenMP support into its optimized TMS320C66x compilers and DSP runtime software. For the Cortex-A15 processors, TI is leveraging industry standard GCC Compiler and Linux™ for OpenMP support.

The OpenMP API is a portable, scalable model that provides developers utilizing TI's multicore processors a simple yet flexible interface for developing parallel applications in high-performance computing disciplines such as imaging, scientific computing, and radar systems. TI's C66x DSPs are the first multicore DSP devices to support the OpenMP API. As embedded multicore hardware enables more functions to be implemented on the same device, efficient parallel programming methods are required to achieve desired performance without increasing software complexity.

OpenMP is a powerful programming model for TI's KeyStone architecture as it:

- Allows reuse of existing C/C++ software investment
- Leverages the ARM and DSP shared memory architecture for multicore
- Makes use of dedicated DSP hardware for fast synchronization
- Runs efficiently on industry-standard Linux and on TI's SYS/BIOS™ real-time operating system (RTOS)

This paper describes the OpenMP programming paradigm and some of the potential improvements proposed for the OpenMP API v4.0 specifications applicable to heterogeneous systems. It also presents TI's efforts to enable efficient OpenMP implementation on its KeyStone multicore architecture.

OpenMP Background

OpenMP is the industry standard for shared memory parallel programming. It provides portable high-level programming constructs that enable users to easily expose a program's task and loop-level parallelism in an incremental fashion. With OpenMP, users specify the parallelization strategy for a program at a high level by annotating the program code with compiler directives (pragmas) that specify how a region of code is executed by a team of threads. The compiler handles the detailed mapping of the computation to the computational engines such as DSPs or GPP cores such as Cortex-A15s.

As shown in Figure 1 below, OpenMP is a thread-based programming language. The master thread executes the sequential parts of a program. When the master thread encounters a parallel region, it forks a team of worker threads that execute in parallel with the master thread.

Migration is easy as OpenMP uses directives (#pragmas in C/C++) to express parallelism. The programmer can incrementally add OpenMP directives to an existing sequential application allowing them to quickly take advantage of multiple cores to execute threads in parallel.

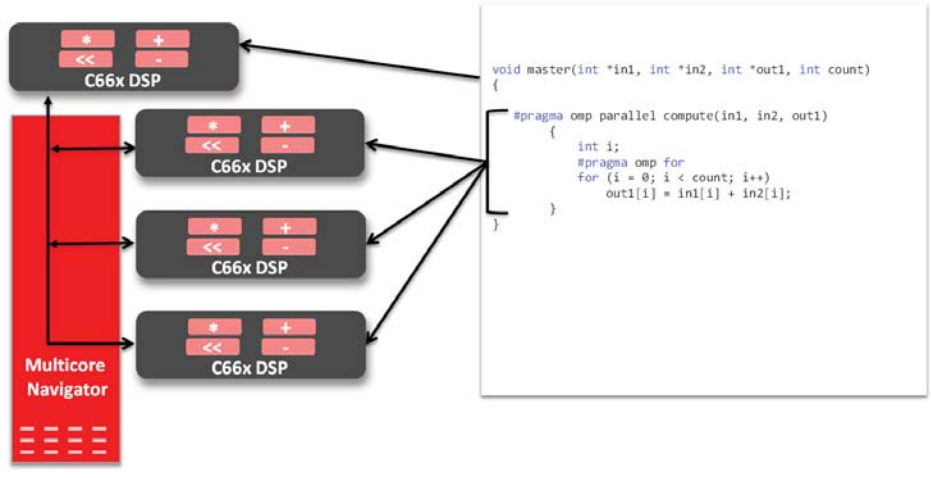


Figure 1: OpenMP in a homogeneous SoC.

With TI's support for OpenMP® in a multicore DSP environment, developers can use OpenMP on homogeneous SoC s such as TI's TMS320C6678. Similarly, OpenMP support is also available for use with other homogeneous TI multicore SoCs.

In the last few years we have seen an increasing number of applications explicitly written for multicore SoCs using OpenMP directives. Application developers have also made significant investments in adding OpenMP constructs to legacy applications.

While semiconductor companies have steadily increased the number of cores in an SoC, two challenges have started to emerge that require innovative approaches.

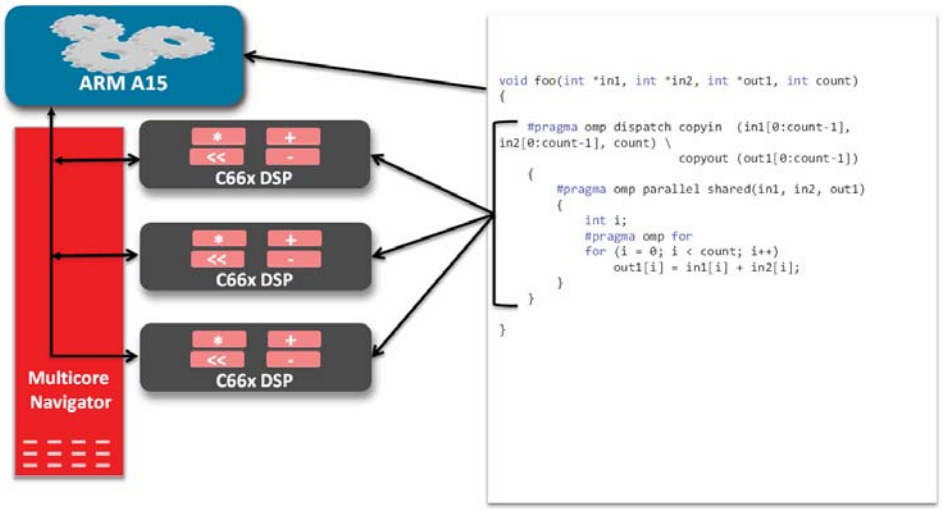
1. Traditional multicore interconnect architectures have not kept pace with the increasing number of cores integrated onto a single SoC. An innovative system architecture that facilitates efficient inter-core communication and synchronization is required to address this challenge.
2. Tailored processing cores should be used for specific workloads. For example, using a Cortex-A15 processor for signal-processing-intensive work is an inefficient use of core resources.

Texas Instruments has been working on addressing these challenges and has developed innovative approaches to solving them, utilizing its Multicore Navigator and a shared memory subsystem. Further elaboration on this novel approach is described in the following section.

To specifically address the second challenge described above, the OpenMP Architecture Review Board is planning to release the definition of an accelerator programming model in the OpenMP API v4.0 specification. Utilizing this capability, developers will be able to easily dispatch parallel processing from the host Cortex-A15 processor to other Cortex-A15 processors or C66x DSPs in TI's KeyStone architecture.

KeyStone Architecture and OpenMP

The anticipated OpenMP accelerator model will introduce new directives that will enable programmers to direct execution to accelerator cores such as DSPs. Using this directive, programmers will have the capability to describe the code segments that they want to run on the DSP.



▲ *Figure 2: Proposed OpenMP 4.0 accelerator model for heterogeneous SoC.*

Figure 2 shows a computation loop annotated with OpenMP-like pragmas (directives used in the figure below are for illustrative purpose only) that direct the compiler to distribute the iterations of the loop to a team of threads. With such directives, programmers will have the opportunity to use the right core for the right work. TI's C66x DSP provides the best dual-precision floating-point operation per watt, while the Cortex-A15 processor offers the best single-threaded performance for control-code functionality. Using ARM for the control type work and C66x DSP for compute or signal-processing-intensive work provides best of both worlds. Using OpenMP directive to enable such work distribution enables developers of embedded applications to achieve optimum performance while keeping their code portable across different heterogeneous architectures.

Support for OpenMP 4.0

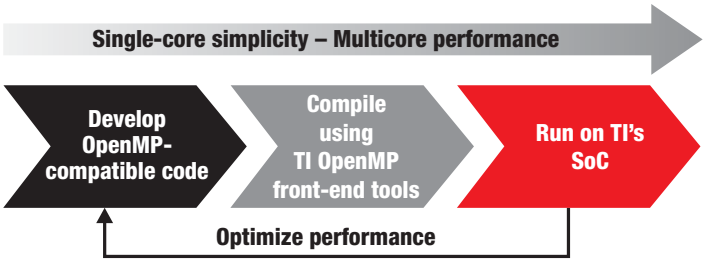
TI plans to support the anticipated OpenMP 4.0 accelerator model for KeyStone-II-based heterogeneous SoCs such the 66AK2Hx and 66AK2Ex SoCs.

TI is planning to develop a unified front-end technology so that developers get single-core simplicity with multicore performance as shown in Figure 3 to the right.

Developers will be able to use a unified front end to compile the code annotated with OpenMP directives. Developers will achieve significant work flow simplicity with this approach so they can focus on getting optimized performance from the SoC.

Behind TI's OpenMP front-end tools, significant work has been done that is transparent to developers. For the runtime software support on the ARM cores, OpenMP is built upon POSIX threads and SMP Linux™. For C66x DSPs, OpenMP executes on a lightweight distributed RTOS designed to require minimal memory and CPU cycles. The RTOS provides speed-optimized memory allocation schemes that avoid memory fragmentation.

TI's front end will automatically parse the code and generate code segments to be compiled for ARM® or C66x DSP cores. The compiler (either TI's C66x compiler or the ARM GCC compiler as appropriate) translates OpenMP directives into multi-threaded code with calls to the runtime library. The runtime library provides support for thread management, scheduling and synchronization. TI has implemented a runtime library that executes with SYS/BIOS™ and interprocessor



▲ *Figure 3: Best-in-class performance with portable, multicore optimized code.*

communication (IPC) protocols running on each DSP core. For the Cortex-A15 processors, the runtime library is available as a part of the standard distributions that go with Linux and GCC.

OpenMP Accelerated with TI's KeyStone Architecture

KeyStone multicore architecture

With up to up to 9.6 GHz of DSP and 5.6 GHz of ARM computational power, TI's flagship 66AK2Hx and 66AK2Ex platforms, based on the KeyStone II architecture, are ideal for high-performance computing applications that demand ultra-high performance at low power levels.

TI's KeyStone architecture features several innovative elements that enable sustained high application-processing rates for multicore systems. Among these are a Multicore Shared Memory Controller (MSMC) and Multicore Navigator, both of which provide hardware support for an efficient OpenMP implementation. The MSMC allows the cores to efficiently share memory as well as access external memory. The Navigator provides atomic hardware queues that can be used for OpenMP synchronization.

Shared memory

The KeyStone architecture includes a shared memory subsystem, comprising internal and external memory connected through the MSMC. The MSMC allows ARM or DSP cores to dynamically share the internal and external memories for both program and data. External memory is connected through the same memory controller as the internal shared memory, rather than to chip system interconnect as has been traditionally done on embedded processor architectures, providing a fast path for software execution. TI's OpenMP runtime library performs the appropriate cache control operations to maintain the consistency of the shared memory as required. Because TI's KeyStone multicore processors have both local private and shared memory, they map well into the OpenMP framework. Shared variables are stored in shared on-chip memory while private variables are stored in local on-chip L1 or L2 memory.

Fast synchronization with Multicore Navigator

A breakthrough feature of the C66x DSP generation and KeyStone architecture is TI's innovative Multicore Navigator, which brings single-core simplicity to multicore devices. TI's support for OpenMP extensively utilizes this feature to significantly accelerate OpenMP directives and resulting communication between cores.

Multicore Navigator provides hardware-assisted functional acceleration that utilizes an innovative packet-based hardware subsystem in KeyStone devices. With an extensive series of thousands of queues and a packet-aware DMA controller, it optimizes the packet-based communications of the on-chip cores by practically eliminating all copy operations. The extreme efficiency (supporting 40 millions queue push and pops per second) made possible by Multicore Navigator results in a 100× performance gain in terms of the number of packets communicated per second over previous-generation cores. The low latencies and zero overhead interrupts ensured by Multicore Navigator, as well as its transparent operations, enable an effective implementation of OpenMP. The TI OpenMP runtime library leverages Multicore Navigator to implement thread management operations, atomic operations and fast barrier operations.

Looking Ahead

TI is an active participant in the OpenMP Architecture Review Board and will implement support for the upcoming OpenMP API v4.0 specification including the accelerator model. TI will continue to evolve its SoC architecture, software and tools to ensure that developers using KeyStone SoCs get the best performance for their OpenMP-compliant applications.

For additional information on TI's KeyStone multicore processors, software and low-cost evaluation modules (EVMs), please visit **www.ti.com/multicore**.

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