Analog Engineer's Circuit Low (Microamp), High-Side, Current-Sensing Circuit With Current-Sensing Amplifier at High Voltage and Overtemperature

Design Description

This circuit demonstrates how to use a current sense amplifier to accurately and robustly measure small micro-amp currents and maximize dynamic range. The following error analysis can be applied to many current sense amplifiers. This design relies on using a precision, low input-bias current sense amplifier and analyzing the dynamic error due to input bias currents on large shunt resistors.

Design Notes

- 1. The *[Getting Started with Current Sense Amplifiers](https://www.ti.com/video/series/precision-labs/ti-precision-labs-current-sense-amplifiers.html?keyMatch=getting%20started%20with%20current%20sense%20amplifiers&tisearch=universal_search)* video series introduces implementation, error sources, and advanced topic for using current sense amplifiers.
- 2. Choose a precision 0.1% shunt resistor to limit gain error at higher currents.
- 3. Choose a low input-bias current (high input-impedance) amplifier such as the [INA190.](http://www.ti.com/product/INA190)
- 4. Confirm VCM is within the operating VCM range of INA190: –0.1V to 40V.
- 5. Error significantly reduces if DC offsets are calibrated out with one-point calibration or if device operates under the same conditions as the *[INA190 Low-Supply, High-Accuracy, Low- and High-Side Current-Shunt](https://www.ti.com/lit/pdf/SBOS863) [Monitor With Picoamp Bias Current and Enable](https://www.ti.com/lit/pdf/SBOS863)* data sheet specifies (V_{VS} = 1.8V, V_{CM} = 12V, V_{REF} = 0.9V, T_A = 25°C). A two-point calibration can be done to eliminate gain error.
- 6. It is recommended to add ≥ 1nF input differential capacitor to INA190 inputs when working with large shunt resistors and DC currents.
- 7. Follow best practices for layout according to the data sheet: decoupling capacitor close to VS pin, routing the input traces for IN+ and IN- as a differential pair, and so forth.

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Design Steps

1. Given the design requirements, verify the shunt resistor achieves a maximum total error of 3.51% at 1µA load current. Assume all offset and gain errors are negative. Note that error due to input bias current (I_{IB}) is a function of the V_{SHUNT} and input differential impedance (R_{DIFF}) where $R_{DIFF} = I_{IB+}/V_{DIFF}$. Since I_{IB} starts around $+500$ pA and decreases as V_{SHUNT} increases, this generates a negative input offset error. See the *IB+ and IB- vs Differential Input Voltage* plot in the data sheet.

T_{MIN} = 0^oC; T_{MAX} = 85^oC
\nI_{LOAD_MINIMUM} = 1µA
\nR_{SHUNT} = 1240Ω, 0.1%
\nV_{VS} = 3.3V; V_{CM} = 24V; V_{REF} = GND = 0V
\nV_{OSLMAR} = -15µV
\nV_{OS-DMRR_MAX} = |1.8V – V_{CK} | ·10<sup>-CMRR_{MMX}/20dB = 12V ·10^{-132dB/2}/20dB = -3.01µV
\nV_{OS-DNRR_MAX} = |1.8V – V_{VS} | ·PSRR_{MAX} = 3.2V ·5^µ/_{V_V} = -7.5µV
\nV_{OS-DVHR_MAX} = |0.9V – V_{REF} | ·RVRR_{MAX} = 0.9V ·10^µ/_{V_V} = -9µV
\nV_{OS-Drift_MAX} = |25°C – T_{MAX} | ·(
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\frac{dV_{OS}}{dT}
$$
)_{MAX} = 60°C ·80^η/_{V_C} = -4.8µV
\nV_{OS-MAX} = 4unc {V_{SHUNT}} = R_{SHUNT} | $\frac{dV_{S+UNT}}{R_{DIFF}} + I_{B_2 - T_yP}$ = 1240Ω: { $\frac{-1.24mV}{2.3MΩ} + 0.5nA$ } = -48.5nV
\nV_{OS-MAX} = V_{OSLMAX} + V_{OS-CMRR} + V_{OS-PSRR} + V_{OS-NVRR} + V_{OS-Drift_MAX} + V_{OS-BMAX}
\nV_{OS-MAX} = -39.4µV
\nR_{shunt_1} tolerance = -0.1% = 0.001
\nGE_{25C_MMX} = -7P^{pp}/_C · (85°C – 25°C) ·10<</sup>

- 2. Verify that the sensed current range fits within the output dynamic range of the device. This depends upon two specifications: Swing-to-V_{VS} (V_{SP}) and Zero-current Output Voltage (V_{ZL}). V_{ZL} is specified over -40°C to +125°C at V_{VS} = 1.8V, V_{REF} = 0V, V_{SENSE} = 0mV, V_{CM} = 12V, and R_L = 10kΩ. Since data sheet conditions do not match the conditions of this design, extrapolate what the maximum V_{ZL} would be.
	- a. Calculate the maximum possible positive offset for testing conditions of V_{ZL}. Call this V_{OS} TestConditions.
	- b. Convert this input offset into an output offset by multiplying by maximum possible gain.
	- c. Determine the Headroom voltage by taking difference between the V_{ZL_MAX} from data sheet and the previously determined maximum output offset.
	- d. Calculate V_{ZL_MAX} in this design by adding the Headroom voltage to the maximum possible output offset for this design.
	- e. Verify that the minimum V_{OUT} at 1µA is greater than V_{ZL_MAX}. Note V_{OUT_MIN} at 1µA assumes worst-case scenario of -1% tolerance for R_{SHUNT} and negative input offsets.

 $\rm V_{OS_TestConditions} = V_{OSI_MAX} + \lceil 0.9V - 0V \rceil \cdot RVRR_{MAX} + \lceil 125^{\circ}\text{C} + 40^{\circ}\text{C} \rceil \cdot (\frac{dV_{OS}}{dT})_{MAX}$ $V_{\rm OS_TestConditions} = +15 \mu V + 9 \mu V + 13.2 \mu V = 37.2 \mu V$ $Headroom = V_{ZL_MAX_DATASHEET} - V_{OS_TestConditions} \cdot Gain_{MAX}$ $Headroom = 3mV - 0.933mV = 2.07mV$ $= V_{\text{O}Cl}$ $_{\text{MAX}} + 10.9V - 0V$ \cdot RVRR $_{\text{MAX}} + 125^{\circ}C + 40^{\circ}C$ \cdot (

 $\rm V_{ZL_MAX} = Headroom + V_{OS_MAX} \cdot Gain_{MAX} = 2.07mV + (39.4 \mu V \cdot 25.061\frac{V}{V}) = 3.06mV$ $V_{\text{OUT_MIN_1}\mu\text{A}} = 29.9 \text{mV} > V_{\text{ZL_MAX}}$

f. Now establish that the maximum V_{OUT} at 104µA is less than V_{SP_MIN}. Note V_{OUT_MAX} at 104µA assumes worst-case scenario of +1% tolerance for R_{SHUNT} and positive input offsets.

 $V_{\text{OUT_MAX}} = [1240 \Omega \cdot (1.001) \cdot 104 \mu \text{A} - 29.6 \mu \text{V}] \cdot 25.061 \frac{V}{V} = 3.234 \text{V}$ $V_{\text{SP_MIN}} = V_{\text{VS}} - 40 \text{mV} = 3.26 \text{V}$ $\rm V_{OUT_MAX}$ = $\rm \left\lfloor R_{SHUNT} \cdot (1+R_{shunt_tolerance}) \cdot I_{LOAD_MAX} + V_{OS_MAX} \right\rfloor \cdot Gain_{MAX}$ $\rm V_{OUT_MAX} < V_{SP_MIN}$

3. Generate *Total Error vs Load Current* curves based upon the total error equations in Step 1. Do this for the typical and maximum data sheet specifications.

Design Simulations

DC Simulation Results

The following graph shows a linear output response for load currents from 1µA to 104µA

Total Error Calculations

The following graph shows the total absolute error over temperature using both the assured limit specifications and the typical specifications. Note that accuracy is limited by the offset voltage at the lowest current sensed and limited by gain error at higher currents. Active offset chopping limits the error due to temperature.

Design References

Texas Instruments, [SBOMAI6 circuit SPICE,](http://www.ti.com/lit/zip/sbomai6) simulation file

Texas Instruments, [Getting started with current sense amplifiers](https://training.ti.com/getting-started-current-sense-amplifiers), Precision labs video series

Texas Instruments, [Extending the Common-Mode Voltage Range of Current-Output Current Shunt Monitors](https://www.ti.com/lit/pdf/slla190), application brief

Texas Instruments, [Current sense amplifiers,](https://www.ti.com/amplifier-circuit/current-sense/products.html) products page

Design Featured Current Shunt Monitor

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