FIFO Patented Synchronous Retransmit: Programmable DSP-Interface Application for FIR Filtering

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Contents

List of Illustrations

Introduction

This application report presents one example of the many uses of the synchronous-retransmit feature of Texas Instruments (TI) digital signal processing (DSP) application-specific FIFOs. This report describes TI's patented synchronous-retransmit feature and shows how this feature can be used in conjunction with a DSP for finite-length impulse-response (FIR) filtering. The TMS320C31 floating-point DSP and the SN74ACT3638 bidirectional clocked FIFO are the examples for this discussion.

Description of Synchronous Retransmit

An SN74ACT3638 functional block diagram with the synchronous-retransmit logic block highlighted is shown in Figure 1. The synchronous-retransmit feature of the SN74ACT3638 allows data stored within the FIFO to be reread starting at a selected position. FIFO1, one of two 512×32 dual-port SRAM FIFOs on board the SN74ACT3638 device, buffers data from port A to port B. FIFO1 is placed in the retransmit mode to select a beginning word and to prevent ongoing FIFO write operations from destroying data to be retransmitted. Data vectors with a minimum length of three words can be retransmitted repeatedly starting at the selected word. The FIFO can be taken out of the retransmit mode at any time, allowing normal operation to resume.

Figure 2 shows the FIFO1 retransmit timing and minimum retransmit length. FIFO1 is placed in the retransmit mode by a low-to-high transition on CLKB when the retransmit mode (RTM) input is high and the port-B output-ready (ORB) flag is high. This rising clock edge marks the data present in the FIFO1 output register as the first retransmit word. FIFO1 remains in the retransmit mode until a low-to-high transition of CLKB occurs while RTM is low.

When two or more reads have been performed past the initial retransmit word, a retransmit is initiated by a low-to-high transition on CLKB when the read-from-mark (RFM) input is high. This rising CLKB edge shifts the first retransmit word to the FIFO1 output register and subsequent reads begin immediately. While FIFO1 is in the retransmit mode, retransmit loops can be performed repeatedly with each pulse of the RFM terminal.

When FIFO1 is in the retransmit mode, it operates with two read pointers. The current-read pointer operates normally, incrementing each time a new word is shifted to the FIFO1 output register. This pointer is used as a reference by the ORB and port-B almost-empty ($\overline{\text{AEB}}$) flags. The shadow-read pointer stores the SRAM location at the time FIFO1 is placed in the retransmit mode and does not change until FIFO1 is taken out of the retransmit mode. This pointer is used as a reference by the port-A input-ready (IRA) and almost-full ($\overline{\text{AFA}}$) flags. While the FIFO is in the retransmit mode, data writes to the FIFO may continue. $\overline{\text{AFA}}$ is set low by the write that stores ($512 - Y1$) words after the first retransmit word, where 512 is the FIFO depth and Y1 is the almost-full-flag offset value. The IRA flag is set low following 512 writes after the first retransmit word.

When FIFO1 is in retransmit mode and RFM is high, a rising CLKB edge loads the current pointer with the shadow-read-pointer value. The ORB flag immediately reflects the new level of fill. If the retransmit changes the status of FIFO1 such that it is no longer within the almost-empty range, up to two CLKB rising edges after the retransmit cycle are required before the AEB flag is asserted. The rising CLKB edge that takes FIFO1 out of the retransmit mode shifts the read pointer used by the IRA and $\overline{\text{AFA}}$ flags from the shadow-read pointer to the current-read pointer.
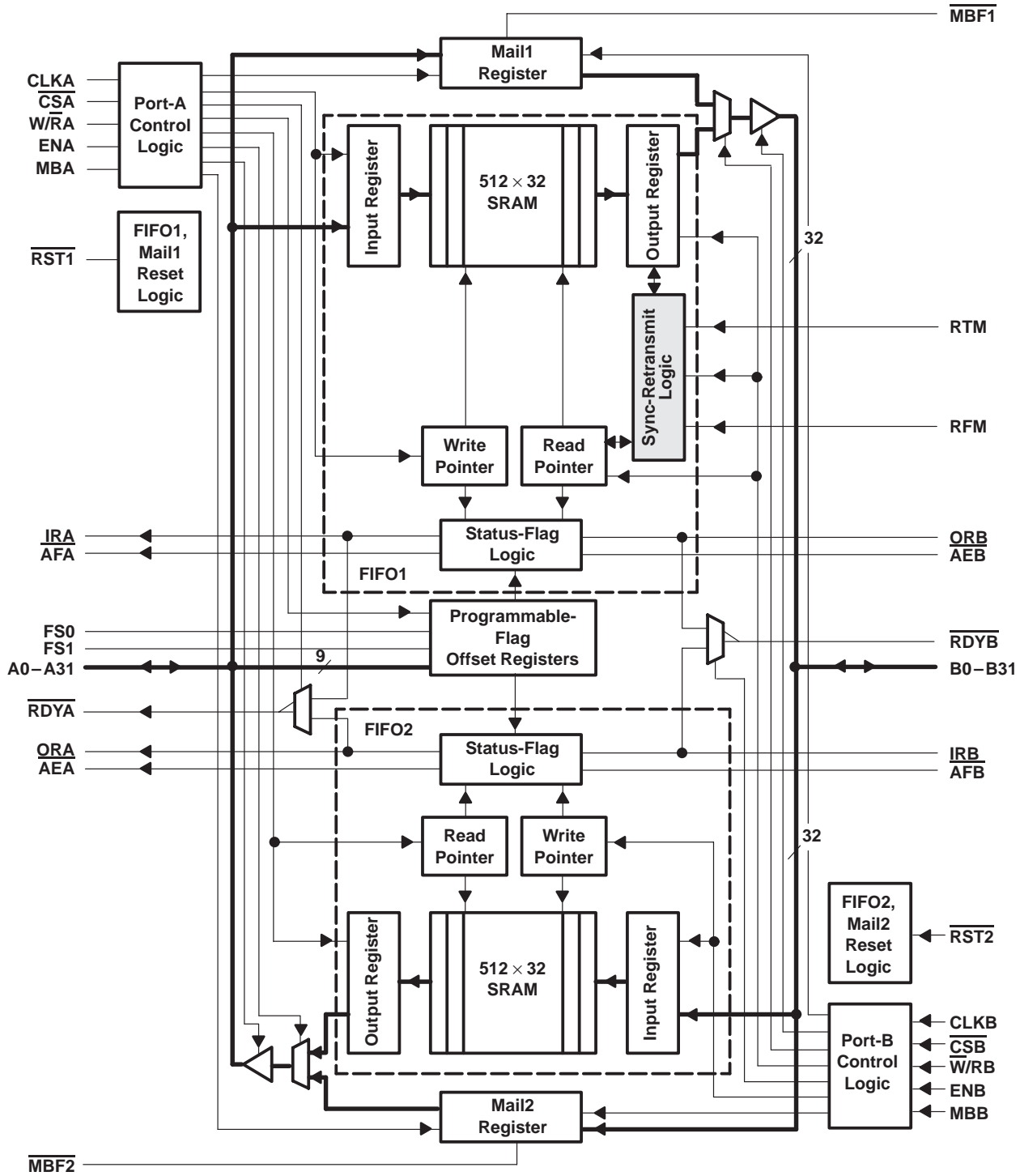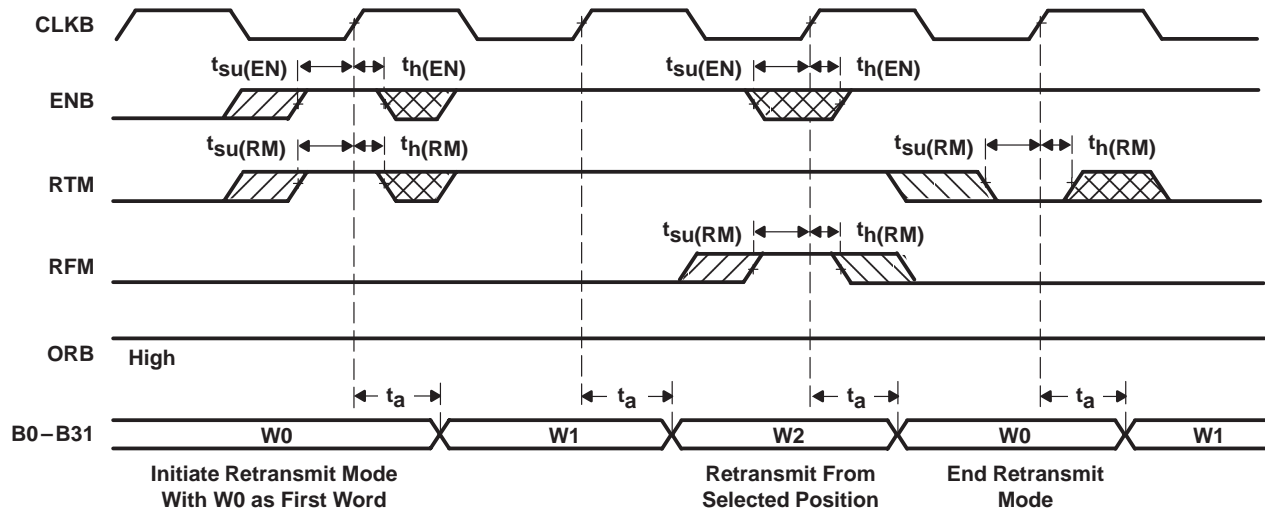
Figure 1. SN74ACT3638 Functional Block Diagram

$t_{su(EN)}$	Setup time, $\overline{CSA}$, W/$\overline{RA}$, ENA, and MBA before CLKA↑; $\overline{CSB}$, $\overline{W}$/RB, ENB, MBB, RTM, and RFM after CLKB↑
$t_{su(EN)}$	Hold time, $\overline{CSA}$, W/$\overline{RA}$, ENA, and MBA after CLKA↑; $\overline{CSB}$, $\overline{W}$/RB, ENB, MBB, RTM, and RFM after CLKB↑
t_a	Access time, CLKA↑ to A0 – A31 and CLKB↑ to B0 – B31

Figure 2. FIFO1 Retransmit Timing Diagram Showing Minimum Retransmit Length

Example of Retransmit for FIR Filtering

In addition to the typical interface functions, such as rate matching and clock partitioning, FIFOs with retransmit capabilities can provide a repeated sequence of data to a processing element such as a DSP. This sequence of information may take the form of coefficients for use in a DSP multiply/accumulate operations as shown in Figure 3.
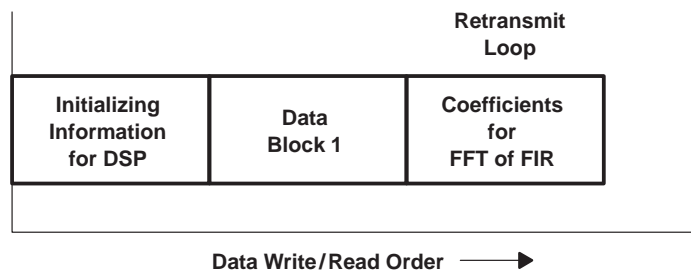

Figure 3. Using a FIFO for Coefficient Storage in Multiply/Accumulate Operations

Many DSP applications require filtering. The FIR filter is a type of digital filter that is implemented very efficiently by the TMS320C31. The FIR filter in the time domain takes the general form of:

$$y(n) = \sum_{i=0}^{N-1} h(i) \times x(n - i)$$

Where:

$y(n)$ is the output sample at time n,
$h(i)$ is the ith coefficient or impulse response, and
$x(n - i)$ is the $(n - i)$th input sample.

The capability for parallel multiply/add operations and circular addressing permits easy implementation of the FIR filter with the TMS320C31 DSP. The former allows a multiplication and addition operation to execute in one machine cycle; the latter generates a finite buffer of length N for the data $x(n)$.

When used for coefficient storage, the FIFO serves as a zero-wait-state SRAM. Applications in which coefficients or other data are stored in external SRAM or EPROMs can be greatly simplified, thereby reducing cost, space requirements, and overall device count. In other instances where DSP internal RAM is used to store the coefficients, a penalty is often paid in the form of overhead time for transferring the coefficients from the buffering FIFO to RAM. This overhead penalty and inefficient use of RAM can be eliminated by the use of the patented synchronous-retransmit feature of the TI FIFO.

Two TMS320C31 external input/output (I/O) flags (XF0 and XF1) can be configured as input or output terminals under software control. In the example of FIR filtering, I/O flags can be implemented to control the retransmit function of the FIFO, providing a programmable DSP interface. Figure 4 shows a block-diagram representation of the bidirectional interface to the programmable DSP.
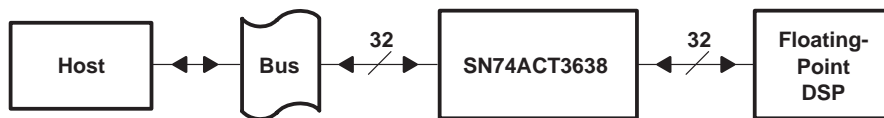

Figure 4. Bidirectional FIFO Interface

Figure 5 shows an interconnection example for the SN74ACT3638-30 FIFO and TMS320C31-40 DSP. The DSP XFO and XF1 terminals are configured for general-purpose output and are directly connected to the RTM and RFM terminals of the FIFO, respectively. The retransmit timing associated with this interface is shown in Figure 6. The I/O flag register (IOF), which is one of 28 registers in the TMS320C31 CPU register file, controls the external pins XF0 and XF1. Figure 7 shows a summary of IOF

register bit assignments. Additional information on the IOF register may be obtained by consulting the TMS320C3x User's Guide (literature number SPRU031C).
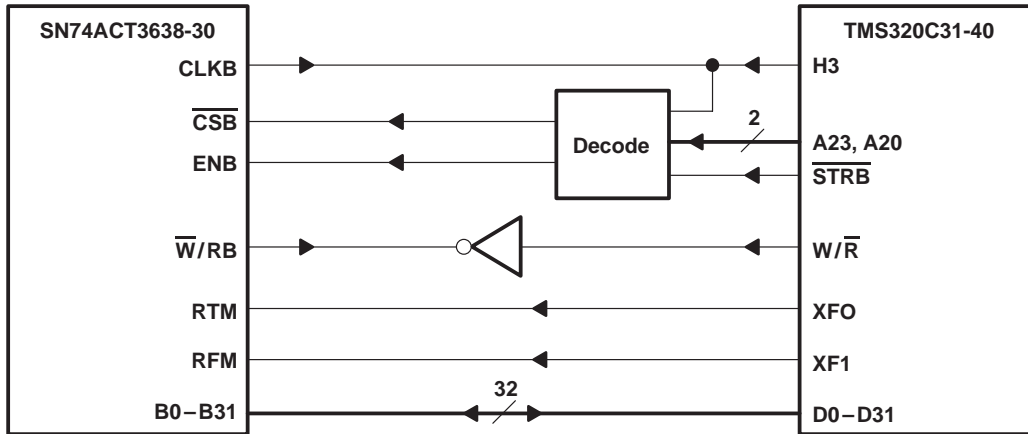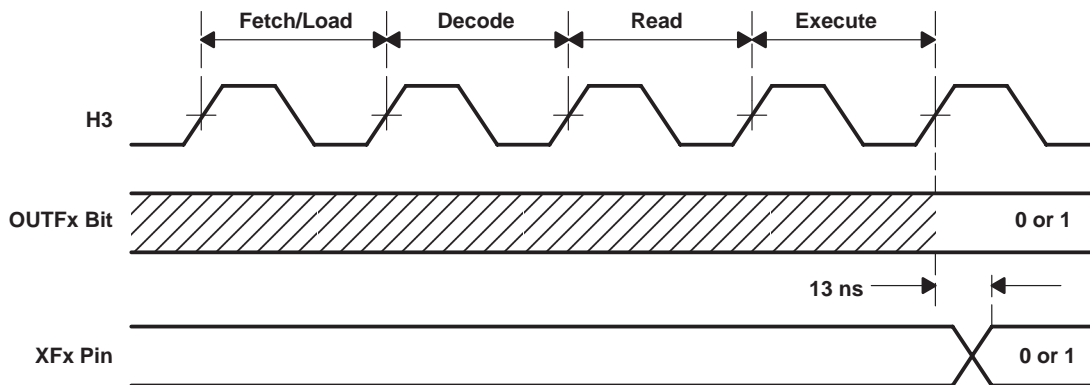

Figure 5. Interconnection Example

Figure 6. Retransmit Timing for Interconnection Example

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx	xx

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
xx	xx	xx	xx	xx	xx	xx	xx	INXF1	OUTXF1	$\overline{\text{I}}$/OXF1	xx	INXF0	OUTXF0	$\overline{\text{I}}$/OXF0	xx
								R	R/W	R/W		R	R/W	R/W	

NOTES: A. xx = reserved bit, read as 0
          B. R = read, W = write

BIT	NAME	RESET VALUE	FUNCTION
0	Reserved	0	Read as 0
1	$\overline{\text{I}}$/OXF0	0	If $\overline{\text{I}}$/OXF0 = 0, XF0 is configured as a general-purpose input terminal. If I/OXF0 = 1, XF0 is configured as a general-purpose output terminal.
2	OUTXF0	0	Data output on XF0
3	INXF0	0	Data input on XF0. A write has no effect.

BIT	NAME	RESET VALUE	FUNCTION
4	Reserved	0	Read as 0
5	Ī/OXF1	0	If Ī/OXF1 = 0, XF1 is configured as a general-purpose input terminal. If Ī/OXF1 = 1, XF1 is configured as a general-purpose output terminal.
6	OUTXF1	0	Data output on XF1
7	INXF1	0	Data input on XF1. A write has no effect.
31−8	Reserved	0−0	Read as 0

Figure 7. IOF Register Bit Summary

Modified Code for TMS320C3x FIR Filtering

The FIFO retransmit control for FIR filtering can be structured as in the following modified code fragment from the TMS320C3x User's Guide (see Figure 8). The values loaded into the IOF register are chosen to set and reset the RTM and RFM terminals of the FIFO as appropriate, providing retransmit control. Figure 9 shows the control timing associated with the FIFO retransmit for the FIR filter.

```
*     TITLE FIR FILTER
*       (!! denotes changes from code example in
*        the TMS320C3x User's Guide)
*     SUBROUTINE  F I R
*     EQUATION: y(n) = h(0) * x(n) + h(1) * x(n−1) +
*                    ... + h(N−1) * x(n−(N−1))
*     TYPICAL CALLING SEQUENCE
*       LOAD   AR0
*       LOAD   AR1
*       LOAD   RC
*       LOAD   BK
* !!    LOAD   IOF
*       CALL   FIR
*     ARGUMENT ASSIGNMENTS:
*      ARGUMENT| FUNCTION
*      --------+-----------------------------------------------
* !!   AR0     | ADDRESS OF FIFO where h vector is stored starting with
*              |   h(N−1)
*      AR1     | ADDRESS OF x(n−(N−1))
*      RC      | LENGTH OF FILTER − 2 (N−2)
*      BK      | LENGTH OF FILTER (N)
* !!   IOF     | XF0, XF1 configured as outputs.  XF0 is high, XF1 is low.
*              |    Initial register content is 026h. FIFO in retransmit mode.
* !! REGISTERS USED AS INPUT: AR1, RC, BK, IOF
* !! REGISTERS MODIFIED: R0, R2, AR0, AR1, RC, IOF
*     REGISTER CONTAINING RESULT: R0
*        .global FIR
*                                  ; Initialize R0
```

Figure 8. FIFO Retransmit Control for FIR Filtering

```
FIR     MPYF3   *AR0,*AR1++(1)%,R0          ; !! AR0 not incremented
*                                           ; h(N-1) * x(n-(N-1)) -> R0
        LDF     0.0,R2                      ; Initialize R2
*    FILTER (1 <= i < N)
        RPTS    RC                          ; Setup the repeat cycle
*                                           ; !! AR0 not incremented
        MPYF3   *AR0,*AR1++(1)%,R0          ; h(N-1-i)*x(n-(N-1-i))->R0
||      ADDF3   R0,R2,R2                    ; Multiply and add operation
*
        ADDF    R0,R2,R0                    ; Add last product
*  !!
        LDI     066h,IOF                    ; Retransmit FIFO data starting
*                                             with h(N-1) by asserting RFM
*                                             (XF1) high
*  !!
        LDI     026h,IOF                    ; End RFM (XF1) high pulse to
*                                             begin normal data reads
*    RETURN SEQUENCE
        RETS                                ; Return
*  end
        .end
```

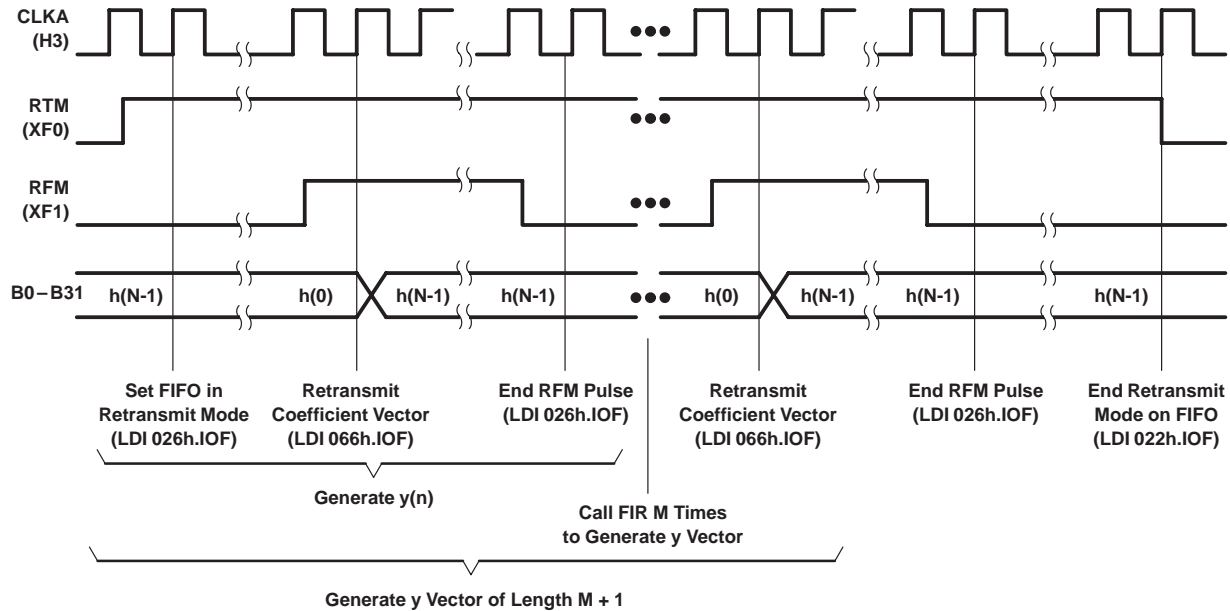**Figure 9. FIFO Retransmit Control for FIR Filtering (Continued)**

Figure 10. Control Timing for FIFO Retransmit for the FIR Filter

Conclusion

Unlike conventional retransmit, TI's patented synchronous-retransmit feature allows the user to select or mark the FIFO data to be retransmitted. Synchronous retransmit is easily controlled by two FIFO terminals: RTM and RFM. As previously discussed in this application report, synchronous retransmit provides a very efficient method for transferring a series of FIR filter coefficients to a DSP without storing the coefficients in a standard SRAM or EPROM. By interfacing the DSP external I/O terminals to the FIFO retransmit terminals, the DSP can effectively request the FIR filter coefficients on demand.

The following FIFOs belong to the DSP application-specific family featuring synchronous retransmit.

Table 1. DSP Application-Specific Family

DEVICE	ORGANIZATION	SPEED SORTS t_C (ns)	MAXIMUM FREQUENCY (MHz)	MAXIMUM ACCESS (ns)
SN74ACT3638	512 x 32 x 2	−15, −20, −30	67	11
SN74ACT3631	512 x 36	−15, −20, −30	67	11
SN74ACT3641	1K x 36	−15, −20, −30	67	11
SN74ACT3651	2K x 36	−15, −20, −30	67	11