

How to Synchronize the MSP430FR6047 Clock System Domains With the Ultrasonic Sensing Oscillator

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MSP430 Applications

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ABSTRACT

The Ultrasonic Sensing (USS) module of the MSP430FR6047 microcontroller (MCU) provides a buffered output of its high-frequency crystal signal (USSXT_BOUT). This signal can be used to drive the Clock System (CS) module through the high-frequency crystal input (HFXIN), as well as external devices. Driving HFXIN this way provides the advantage of synchronizing the timing of other peripherals with the operation of the USS and its submodules, such as the High-Speed Sigma Delta ADC (SDHS). Another benefit is the ability to use a single high-frequency crystal for both the USS and CS, reducing solution cost. The sample code described in this document can be downloaded from www.ti.com/lit/zip/SLAA744.

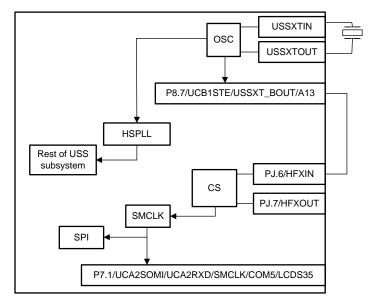


Figure 1. Block Diagram



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USSXT	Ultrasonic sensor high-frequency oscillator (crystal or ceramic)
USSXT_BOUT	Ultrasonic sensor high-speed oscillator buffered output
SMCLK	Subsystem master clock
HFXIN	Clock System high-frequency oscillator input
HFXT	Clock System high-frequency oscillator
HFXTCLK	Clock System high-frequency oscillator clocking signal
UNMI	User nonmaskable interrupt
OFIFG	Oscillator fault interrupt flag (part of UNMI)
HFXTOFFG	Clock System high-frequency oscillator fault flag
LFXTOFFG	Clock System low-frequency oscillator fault flag
MODOSC	Clock System internal low-power module oscillator (5-MHz typical frequency)
LPM3	Low-power mode 3
LPM0	Low-power mode 0

2 Hardware

The hardware uses the MSP-TS430PZ100E target board, which includes a socket and 8-MHz USSXT crystal (underside of PCB). The target board is set up by connecting P8.7 USSXT_BOUT to PJ.6 HFXIN (target board pins 95 and 9, respectively). The SMCLK output can be monitored on P7.1 (target board pin 41), and compared to the USSXT output by monitoring P8.7.

- **NOTE:** The crystal can be replaced with a 4- to 8-MHz resonator, but the firmware needs to be modified. See Table 1 and Section 3.1.
- **NOTE:** The USSXT_BOUT has been observed to be susceptible to glitches during EMI events. Therefore, it is not advised to use it to drive MCLK. To minimize this risk, the following considerations have been outlined in the *Applications, Implementation, and Layout* section of the MSP430FR6047 data sheet.
- Keep the traces of USSXTIN and USSXTOUT as short as possible. If one trace must be longer than the other, keep USSXTIN shorter, because USSXTIN is more sensitive to EMI.
- If USSXT_BOUT is used, keep coupling to USSXTIN and CH0_IN to a minimum.
- If USSXT_BOUT is feeding other clock or device inputs, apply a small capacitor (10 pF) as the line termination load at end of line. This avoids reflection artifacts on sensitive inputs (for example, HFXTIN).



Software

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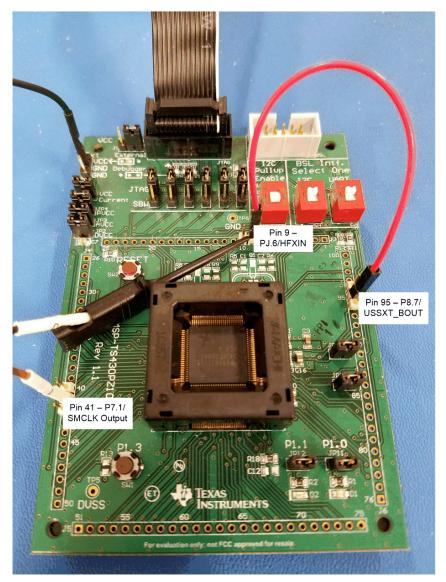


Figure 2. Target Board Setup

3 Software

The example firmware initializes the USSXT_BOUT, SMCLK output, and HFXIN pins, and configures P1.0 for an LED blink for visual confirmation that the code is running. The Clock System is configured so that HFXTCLK sources SMCLK with a divider of 1, so that SMCLK is 8 MHz.

The HFXT is configured in bypass mode for use with an external signal. This configuration requires setting the HFFREQ bits in CSCTL4 corresponding to output frequency of the USSXT_BOUT (see Table 1).

HFXT Frequency Range	HFFREQ[1:0]
0 to 4 MHz	00
>4 MHz to 8 MHz (selected for this use case)	01
>8 MHz to 16 MHz	10
>16 MHz to 24 MHz	11

Table 1. HFFREQ Settings

3.1 USSXT Oscillator Enable Steps

The USSXT oscillator is enabled by the following steps:.

- 1. Configure HSPLLUSSXTLCTL.OSCTYPE bit correctly based on the resonator type (0 for a crystal resonator, or 1 for a ceramic resonator).
- 2. Write 1 to the HSPLLUSSXTLCTL.USSXTEN bit.
- 3. Wait for the start-up time. Timer_A4 and its interrupt are setup for a 512-us delay LPM3 delay while the USSXT stabilizes. This delay equates to 4096 cycles, as required for a crystal resonator. If a ceramic resonator is used, a delay of only 512 cycles is required. The required timer cycles can be calculated by Equation 1.

Timer_F × SC / ResF

where

- SC = Startup cycles
- ResF = Resonator frequency
- Timer_F = Timer clock_frequency
- 4. Read the HSPLLUSSXTLCTL.OSCSTATE bit to check if the USSXT started.
- 5. The USSXT is running and USSXT_BOUT is enabled.

OPTIONAL: If using the rest of the USS module, after performing the preceding steps, power up the UUPS (Universal USS Power Supply) and checked for lock, as shown in the following code example.

```
// Start the UUPS/PLL
UUPSCTL |= USSPWRUP; // Power up the UUPS to start the PLL
while((UUPSCTL & UPSTATE_3) != UPSTATE_3); // Wait for UUPS to power up
while(!(HSPLLCTL & PLL_LOCK)); // Wait for PLL to lock
```

The HFXIN fault flag is cleared and tested; this step is critical! Without doing so, the CS will default any HFXT sourced clock to source from the MODOSC. This will be evident if an approximately 5-MHz signal is observed from the SMCLK output. The following code snippet shows an example of doing this.

```
// XT1 and XT2 Fault Flag Clear and Test
CSCTL0_H = CSKEY_H; // Unlock CS registers
do
  {
    CSCTL5 &= ~HFXTOFFG; // Clear XT2 fault flag
    CSCTL5 &= ~LFXTOFFG; // Clear XT1 fault flag
    SFRIFG1 &= ~OFIFG;
    } while (SFRIFG1 & OFIFG); // Test oscillator fault flag
    CSCTL0_H = 0; // Lock CS registers
```

The oscillator fault interrupt (OFIFG) of the UNMI interrupt vector is enabled. This interrupt occurs any time the HFXTOFFG bit (or LFXTOFFG bit) of the CSCTL5 register is set, allowing for detection of fault conditions. This interrupt is set up to light the LED in P1.0 when the HFXT fault occurs. To cause this fault, either disconnect the wire between Pin 9 and Pin 95, or short the USSXT (on the back of the board, marked Q3).

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Testing

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4 Testing

Figure 3 shows the configuration used for testing.

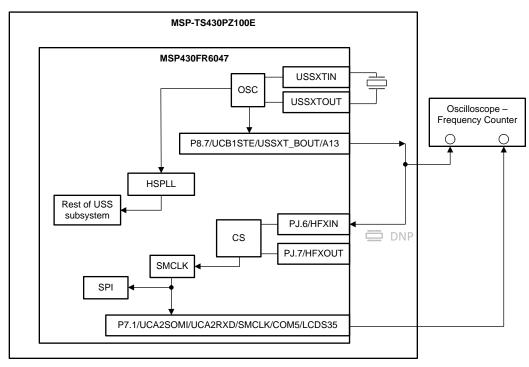


Figure 3. Test Setup

Figure 4, Figure 5, and Table 2 show the parameters measured using an Agilent 53220A Universal Counter to monitor the outputs of SMCLK and USSXT_BOUT. Phase difference was measured as the delay between the rising edges of the USSXT_BOUT signal and the SMCLK output, showing the degree of precision synchronization that is achievable. Phase variation was measured as the standard deviation of phase difference over time and converted to percentage of an 8-MHz period as Equation 2. StdDev(ϕ) / (360 × 8 MHz) (

(2)

NOTE: The phase difference did not vary significantly at steady temperature.

Frequency ratio was measured as the ratio of the absolute frequencies of USSXT_BOUT and SMCLK, which indicates the accuracy of the ability of the SMCLK to follow the USSXT.

NOTE: Phase angle was observed to change over temperature.





Figure 4. Phase at Room Temperature

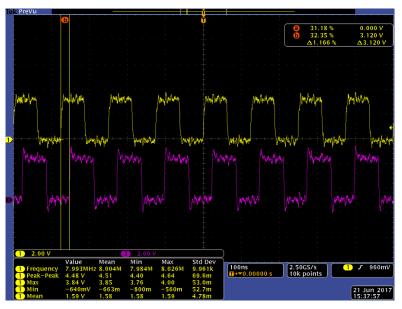


Figure 5. Oscilloscope Capture at Room Temperature

Table 2. Test Data

Measurement	Ambient Temperature	0°C to 80°C Sweep
Frequency ratio (USSXT_BOUT/SMCLK)	0.000453 ppm	0.085 ppm
Phase difference	52.98°	-
Phase variance (percentage of 8-MHz period)	0.27%	2.03%
Phase variance from power cycling USSXT	0.62%	

NOTE: The results in Table 2 are from simple tests and are not ensured or tested in production.



References

www.ti.com

5 References

- 1. MSP430FR58xx, MSP430FR59xx, MSP430FR68xx, and MSP430FR69xx Family User's Guide
- 2. MSP-TS430PZ100E Schematics

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