Application Report
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Comparing Bus Solutions

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ABSTRACT

The strong interest in this application report prompted this third edition. In addition to the changes and updates made throughout these sections, this edition also discusses Local Interconnect Network (LIN), USB-On-the-Go, DisplayPort, digital isolators, and more. This application report serves as a reference tool for finding the most appropriate data bus solution for today's advanced system architectures. It gives an overview of the different bus solutions available from Texas Instruments.

Designers can use many different solutions to solve the same problem. The task is to identify the optimum solution for their application. This application report makes it easier for designers to do this. It has sections on data transmission fundamentals, data line drivers and receivers, data links, and data signaling conditioners. Subsections discuss the electrical properties, applicability, and features of each product family.

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Trademarks

1 Overview

In today's information-hungry age, transmitting data several inches between computer memory and display screen is just as critical as sending it halfway around the globe. To meet these increasingly demanding data transmission needs, Texas Instruments has combined its expertise in high-speed digital and analog technologies to constantly extend the performance and capability of practically every data transmission standard.

This application report provides the reader with an overview of wired data-bus systems and provides insight into which standard or bus configuration best suits a designer's needs. Before discussing the prominent data transmission standards, their technical features, and the products that TI offers for each of these standard applications, the fundamental differences of the basic bus structures must be explained.

For the purposes of this report, products are divided into data line drivers and receivers, data links, and data signal conditioners or translators. Line drivers and receivers generate and receive the electrical signals over cables or board traces. Data link products arrange data for transmission and disassemble it for reception. Signal conditioners or translators modify data signals for particular application needs.

1.1 Single-Ended or Differential Transmission

The two basic forms of data transmission circuits are single-ended and differential. In the single-ended or unbalanced circuit of Figure 1, the voltage difference between the signal line and common local ground determines the bus state. In the Figure 2 differential or balanced circuit, the voltage difference between two complementary signal lines determines the bus state. Each has advantages and disadvantages.

Figure 1 presents the electrical schematic diagram of a single-ended transmission circuit and the noise sources V_N and V_G that directly add to the signal voltage, V_O. This makes the single-ended circuit susceptible to external noise influences. Because no complementary signal (as in differential) cancels the fields created by the single-ended signal, it radiates much more noise than differential circuits. Electromagnetic noise susceptibility and emissions relegate single-ended interfaces to low signaling rates and short transmission lines. However, the single-ended interface line driver, receiver, and interconnection costs are often less than those of differential circuits.

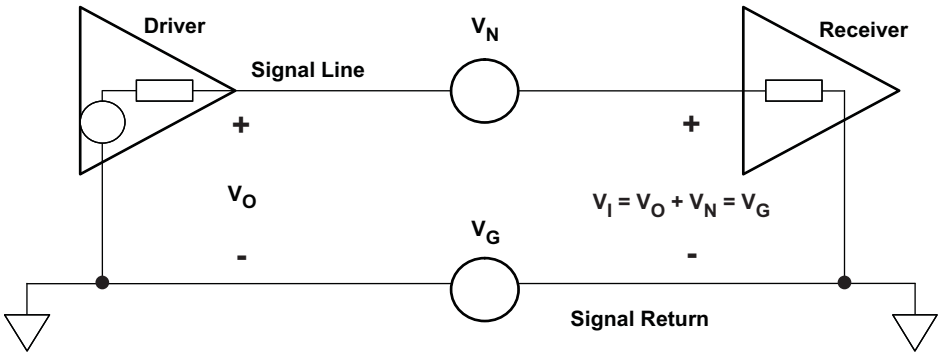


Figure 1. Single-Ended Transmission Circuit Model

Figure 2 shows the electrical schematic diagram of a differential transmission circuit in which noise sources V_N and V_G add to each signal line and are common to both signals. The differential receiver measures the difference between the two lines and rejects the common voltage of the signals. If used with closely coupled lines, the complementary signals cancel each other's electromagnetic fields, resulting in high immunity and low noise emissions. This immunity to external noise influence and the low radiated emissions make differential signaling a good choice when relatively high signaling rates and long distance are required in electrically noisy, or noise-sensitive applications. Differential signaling comes with the additional cost of the line driver, receiver, and interconnection over the cost of single-ended transmission.

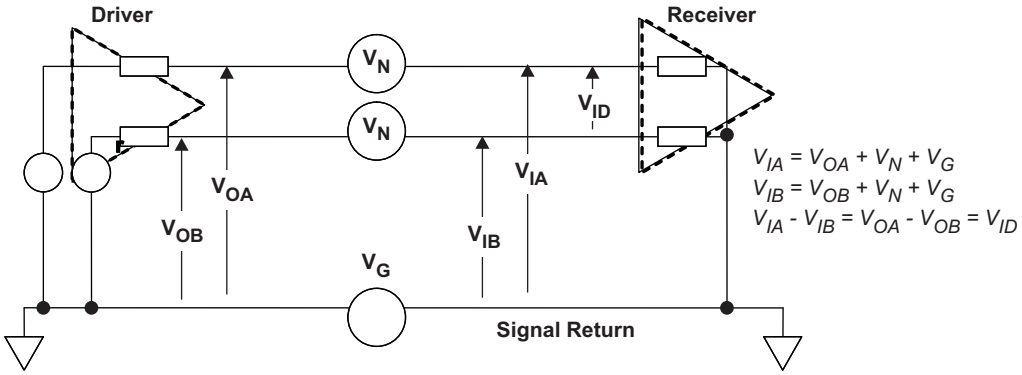


Figure 2. Differential Transmission Circuit Model

1.2 Modes of Operation

Modes of operation refer to the direction of data flow and affect the electrical requirements for line drivers and receivers. Figure 3 displays the simplex mode for the unidirectional (nonreversible) flow of data from a single line driver to a single line receiver.

Figure 3. Simplex Bus

The full-duplex mode consists of two simplex circuits transmitting simultaneously in opposite directions between ports.

The distributed simplex mode or differential multidrop mode is a single line driver transmitting unidirectional to more than one receiver. Figure 4 presents some examples.

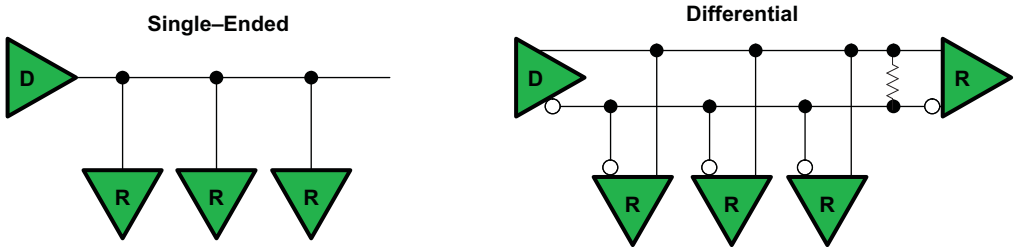


Figure 4. Multidrop Bus

The half-duplex mode is a nonsimultaneous, two-way data flow between two line driver and receiver pairs or transceivers. Figure 5 illustrates this.

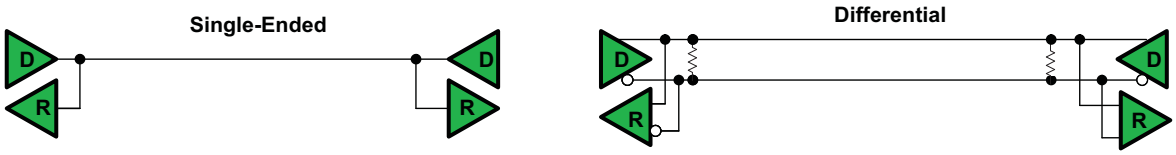


Figure 5. Half-Duplex Bus

The logical extension of the half-duplex mode is the multipoint bus. A multipoint bus is the nonsimultaneous, two-way data flow among three or more transceivers connected to the same physical transmission line, as illustrated in Figure 6. Multipoint line drivers and receivers have stringent electrical requirements and support all of the other modes of operation.

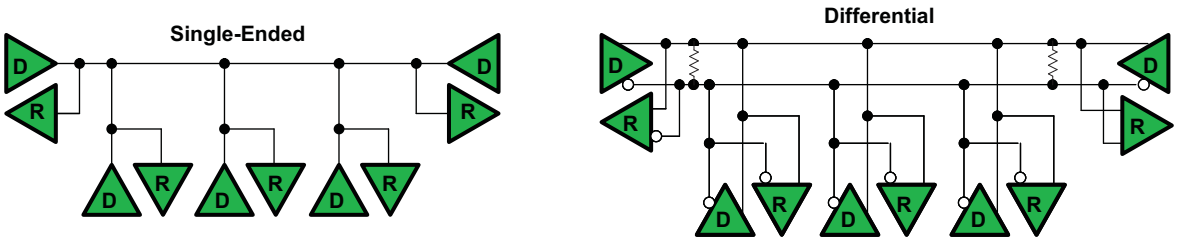


Figure 6. Multipoint Bus

1.3 Parallel or Serial Transmission

Figure 7 illustrates the difference between parallel and serial data transmission. Parallel data buses transmit multiple bits at the same time over a signal line for each data bit. Serial data buses transmit one bit after another through a single line by serializing, then de-serializing back to parallel data. Although serial buses must transmit at a higher rate to achieve the same signaling rates as a parallel bus, both methods have advantages and disadvantages.

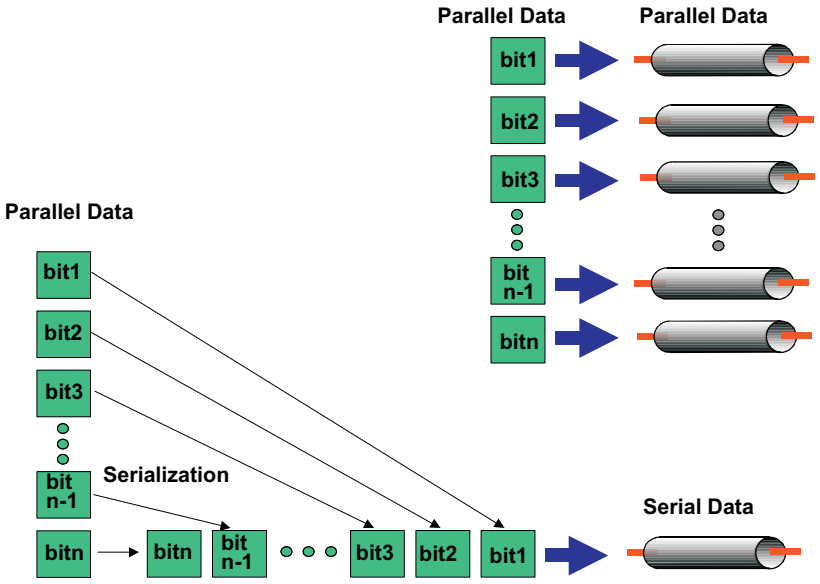


Figure 7. Principle of Parallel and Serial Transmission

Latency is typically referred to as the time from a data request to its receipt. Generally, latency is lower in parallel buses because the time to serialize and deserialize the data is not required. Operational software protocols are often implemented for a parallel bus interface by dedicating specific bits for the control of data transfer, thereby enabling higher signaling rates.

The interconnection cost advantage of the serial bus is from the single data path that results in less board area, fewer connector pins, and less transmission cable cost.

The signaling rate advantage goes to the parallel bus because the width of a bus has no limit. However, distance quickly become a critical factor as parallel fields interact with each other. High-quality, shielded, twisted-pair, parallel cable helps to slightly extend the parallel bus length, but not to the extreme lengths that can be attained on a single twisted-pair cable.

1.4 Data Transmission Speed

Many terms are used to describe the signaling rate or speed of data transfer, and the designer needs to understand the context when using signaling rate units. The minimum unit-interval or t_{UI} describes the minimum time duration of a single pulse of a bit sequence. Many standards define signal quality either in terms of signal rise and fall times or eye-pattern jitter as a percentage of the t_{UI}. The inverse of the t_{UI} is the signaling rate in units of bits per second such as kilobits per second (kbps) or megabits per second (Mbps). These parameters often define the basic bandwidth requirements of a data transmission circuit regardless of its form, mode, or other characteristic.

Some applications use the input clock frequency in Hertz to describe a data transfer rate. This is commonly used when comparing serializer and deserializer products with a known parallel bus width. The relation of Hertz to bits per second is that a single bit is typically considered to be a 180 degree unit – a 360 degree cycle is two bits. Therefore, 1 Hz is equal to 2 bits per second.

1.5 Standardized Interfaces

The primary reason for standardizing a data interface is the economy of scale. The high number of manufacturers of standardized interchangeable products such as RS-485 transceivers, typically lowers the end cost to a user. To this purpose, governments and industry trade groups have published many data transmission standards. The Institute of Electrical and Electronic Engineers (IEEE), the Telecommunications Industry Association (TIA), and the International Standards Organization (ISO) are just a few examples.

Some standards are comprehensive and specify all of the necessary characteristics for successful interoperation of a data interface. Others focus on a subset of the requirements, such as the electrical layer, and are referenced by other standards. In some cases, first-to-market interface products such as emitter-coupled logic (ECL) have become a de facto standard electrical layer.

2 Data-Line Drivers and Receivers

Line drivers and receivers are responsible for passing bits onto and receiving them from the connecting medium. They have no understanding of the meaning of the bits, but deal with the electrical characteristics of the signals and signaling methods. The signaling rate, mode of operation, and distance are the primary selection criteria.

Table 1 summarizes the Texas Instruments line drivers and receivers, which are discussed in the remainder of this section. The speed and distances listed are estimated maximums and simultaneous operation at both maximums may not be possible. As cable length increases, you must lower the signaling rate to keep the same bit-error rates. This, and the increased exposure to noise with distance, makes the analog characteristics of line drivers and receivers important and helps explain the number of different standards. It also complicates the selection process.

Table 1. Electrical Data Interfaces

INTERFACE RATE	SIGNALING	DISTANCE	FORM	MODE(S)	STANDARD	PRODUCT FAMILY[1]
Backplane Transceiver Logic (BTL)	< 50 Mbps	< 1 m	Single-ended	Multiplex	IEEE896.1	Backplane Logic
Controller Area Network (CAN)	< 1 Mbps	< 400 m	Differential	Multiplex	ISO 11898	CAN
Current-Mode Logic (CML)	< 5 Gbps	< 1 m	Differential	Half Duplex		LVDS/M-LVDS/ECL/CML
Emitter-Coupled Logic (ECL)	< 5 Gbps	< 10 m	Single-ended or Differential	Distributed simplex		LVDS/M-LVDS/ECL/CML
General-Purpose Interface Logic(GPL)						
Gunning Transceiver Logic (GTL)	<120 Mbps	< 1 m	Single-ended		JESD8-3	
Gunning Transceiver Logic Plus (GTLP)	< 200 Mbps	< 1 m	Single-ended		JESD8-3	
IEEE 1284 Compatible Devices						
Local Interconnection Network (LIN)						
Low-Voltage Differential Multipoint (LVDM)	< 1 Gbps	< 10 m	Differential	Half duplex	None	M-LVDS PHYs (<500Mbps)
Low-Voltage Differential Signaling (LVDS)	< 2 Gbps	< 10 m	Differential	Distributed simplex	TIA/EIA-644	M-LVDS PHYs (<800Mbps)
Multipoint-Low-Voltage Differential Signaling (M-LVDS)	<500 Mbps	< 30 m	Differential	Multiplex	TIA/EIA-899	M-LVDS PHYs (<500Mbps)
RS-232	< 250 kbps	< 20 m	Single-ended	Simplex	TIA/EIA-232	RS-232
RS-422 simplex	< 40 Mbps	< 1200 m	Differential	Distributed simplex	TIA/EIA-422	RS-422
RS-485	< 40 Mbps	< 1200 m	Differential	Multiplex	TIA/EIA-485	RS-485
Stub SeriesTerminated Logic (SSTL)	< 400 Mbps	< 1 m	Single-ended		EIA/JESD8-8, EIA/JESD8-9	
VMEbus	< 80 Mbps	< 1 m	Single-ended	Multiplex	ANSI/VITA1-1991	

(1) For additional information on each Product Family, go to www.ti.com and enter the relevant product family name in the *Search by Keyword* box.

2.1 Backplane Transceiver Logic (BTL)

In the past, the standard solutions for driving bus lines on backplane systems were TTL or CMOS logic circuits. However, some issues result from the high voltage swing of 3.3 V up to 5 V: Correct termination for all load conditions is not possible and large drive capabilities are necessary to enable incident wave switching.

A bus system with reduced voltage swing solves a lot of problems. The BTL bus realizes a bus in open-collector mode, as shown Figure 8. In this case, the falling edge is actively generated from the driver. Only a low impedance driver can switch the bus with the incident wave.

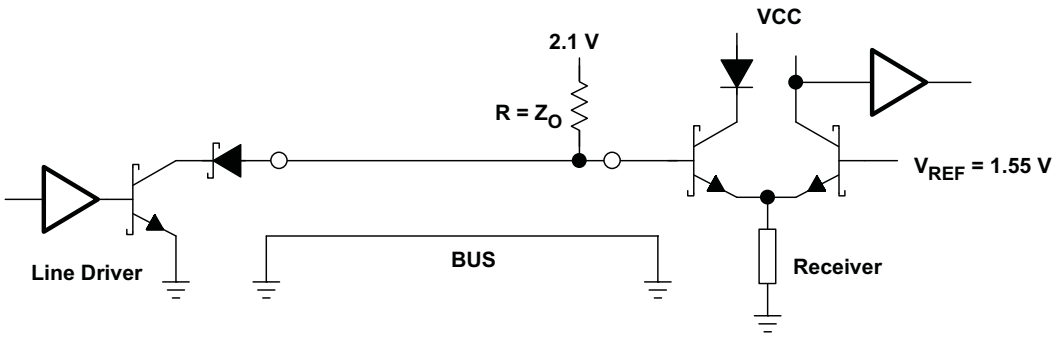


Figure 8. Principle Setup of an Open-Collector Bus System Using BTL Devices

2.1.1 Electrical

The physical layer of the Futurebus is called backplane transceiver logic (BTL) and works only with a voltage swing of 1.1 V, using an open-collector bus system. The saturation voltage of the pulldown transistor and the forward voltage of the serially connected diode generates the output low level voltage of 1 V. The high level of 2.1 V comes from the termination resistor connected to the termination voltage of 2.1 V. The value of the termination resistor is equal to the impedance of the bus-line and therefore the bus line is terminated correctly. For safe detection of the logic levels, the inputs are designed with differential amplifiers and a threshold at 1.55 V, exactly in the middle of the voltage swing.

To reduce ICC current spikes, the fall time is defined to be 2 ns or slower. The rise time is not generated by active electronics, but by the pullup resistor.

2.1.2 Applicability

Futurebus plus logical layer specification, according to the IEEE896.2 specification, describes the node management, live insertion, and profiles. However, the physical layer may also be used stand-alone without the logical layer.

The target area for BTL devices is the telecommunications sector, where live insertion capability is especially mandatory.

2.1.3 Features

- Reduced voltage swing: V_L = 1 V; V_H = 2.1 V generates low switching noise 10 Ω or 20 Ω || 20-Ω line impedance
- Correct line termination by a pullup resistor at the line end avoids line reflections
- Decoupling diode reduces output capacitance to < 5 pF, increases line impedance
- Maximum output edge rate 2 ns, trapezoidal waveform reduces system noise
- Supports live insertion/withdrawal

Table 2. Top Device List – Backplane Transceiver Logic

DEVICE	SPECIFICATION	DESCRIPTION	PACKAGE	STATUS
SN74FB2033A	TTL /BTL	8-Bit TTL /BTL registered transceivers	52-pin PQFP	Available
SN74FB1651	TTL /BTL	17-Bit TTL /BTL universal storage transceivers with buffered clock times	100-pin SQFP	Available
SN74FB2031	TTL /BTL	9-Bit TTL /BTL address/data transceivers	52-pin PQFP	Available
SN74FB1653	LVTTL /BTL	17-Bit LVTTL /BTL universal storage transceivers with buffered clock lines	100-pin SQFP	Available
SN74FB2041A	TTL /BTL	7-Bit TTL /BTL transceivers	52-pin PQFP	Available
SN74FB2040	TTL /BTL	8-Bit TTL /BTL transceivers	52-pin PQFP	Available

2.2 Current-Mode Logic (CML)

2.2.1 Electrical

Current-mode logic (CML) is used in point-to-point, high-speed, differential-data transfer applications. CML is typically used across a 50-Ω transmission medium, using a 50-Ω to VCC termination. Typical output voltage swings for CML are 600-mV peak or 1200-mV peak-to-peak, allowing for greater transmission distances, whereas the output common mode is typically VCC – 300 mV.

2.2.2 Applicability

CML is a high-speed, differential-signal logic implementation. CML is typically used to implement high-speed I/O structures found in gigabit SerDes, high-speed clocking devices, and other high-speed digital communication links. CML technology is often used for implementing multi-gigabit links running from 3 Gbps to 10 Gbps (or equivalent clock frequencies) for applications such as gigabit Ethernet, 10G Ethernet, and Fibre Channel.

2.2.3 Features

The CML interface drivers provide several design features, including high-speed capabilities, adjustable logic output swing, level adjustment, and adjustable slew rate. CML can be used in both AC-coupled and DC-coupled environments (assuming proper pullup and termination schemes are implemented). In the case of extremely high data rates applications (6 Gbps to 10 Gbps), superior propagation delay characteristics and static current consumption enable lower power solutions.

See Interface Selection Guide for a list of top CML devices: www.ti.com/interface.

2.3 Controller Area Network (CAN)

The Controller Area Network (CAN) is an International Standardization Organization (ISO)-defined, serial communications bus originally developed for the automotive industry to replace the complex wiring harness with a two-wire bus. The specification calls for signaling rates up to 1 Mbps, high immunity to electrical interference, and an ability to self-diagnose and repair data errors.

CAN is ideally suited in applications requiring a large number of small messages in a short time, with high reliability in rugged operating environments. Because CAN is message based and not address based, it is especially suited when data is needed by more than one location and system-wide data consistency is considered mandatory.

2.3.1 Electrical

The CAN standard, ISO 11898:1993 defines half-duplex, differential transmission on cable lengths up to 40 m, a maximum stub length of 0.3 m, and a maximum of 30 nodes at signaling rates up to 1 Mbps. However, with careful design, much longer cables, longer stub lengths, and many more nodes can be added to a bus – always with a trade-off in signaling rate. For more information on the CAN physical layer, see the application report *Controller Area Network Physical Layer Requirements* (SLLA270).

A single, shielded or unshielded, twisted-pair cable with a 120-Ω characteristic impedance (Zo) is specified as the interconnect. This interconnecting cable is terminated at both ends with a resistor equal to the Zo of the line. Nodes are then connected to the bus with unterminated drop cables or stubs.

Data transmission circuits employing CAN are used in applications requiring a rugged interconnection with a wide common-mode voltage range. Therefore, shielded cable is recommended in these electronically harsh environments, and when coupled with the Standard's –2-V to 7-V common-mode range of tolerable ground noise, helps to ensure data integrity.

The CAN communications protocol, ISO 11898:1993, describes how information is passed between devices on a network, and conforms to the Open Systems Interconnection (OSI) model that is defined in terms of layers. ISO 11898 defines the functions of the lower layers of the OSI model that are performed within a CAN controller. These CAN controller functions are designed for interaction with a higher layer protocol such as CANopen to complete node communication relationships for bus operation. An abundance of plug-n-play CAN programming routines are available on the Internet from different vendors.

2.3.2 Applicability

The robust features of CAN make it ideally suited for the many rugged applications to which the CAN protocol is being adapted. Among the applications finding solutions with CAN are automobiles, trucks, trains, buses, airplanes and aerospace, agriculture, construction, mining, and marine vehicles. CAN-based control systems are being used in factory and building automation and embedded control systems for machines, medical devices, domestic appliances, and many other applications.

2.3.3 Features

- Established standard and standardized plug-n-play products
- Fault tolerant – very high short-circuit protection
- Self-diagnosing error repair – every bit checked 5 times for error
- Very robust interface for harsh electrical environments
- Wide common-mode operating range

Table 3. Top CAN Device List

DEVICE	FEATURES	POWER	PACKAGE
SN65HVD230, SN65HVD231, and SN65HVD232 CAN Transceiver Family	High-temperature range and short-circuit protection. Low-power Standby and Sleep modes. Wide Common mode. Low power.	V_{CC}: 3.3-V I/O: (LV)TTL / CAN	8-pin SOIC
SN65HVD233, SN65HVD234, and SN65HVD235 CAN Transceiver Family	High-temperature range and short-circuit protection. Low-power Standby and Sleep modes. Wide Common mode. Low power. Auto-baud loopback diagnostic function.	V_{CC}: 3.3-V I/O: (LV)TTL / CAN	8-pin SOIC
SN65HVD251	High-temperature range and short-circuit protection. Low-power Standby. Wide Common mode. Low cost.	V_{CC}: 5-V I/O: 5-V CMOS / CAN	8-pin SOIC
SN65HVD1040	Low-power, 5-μA bus monitor. Wide Common mode. High-ESD protection. Split pin bus stabilizing function. High-temperature range and short-circuit protection.	V_{CC}: 5-V I/O: TTL / CAN	8-pin SOIC
SN65HVD1050	High-temperature range and short-circuit protection. Low-power Standby. Wide Common mode. Low cost.	V_{CC}: 5-V I/O: TTL / CAN	8-pin SOIC
TMS320LF240x DSP Family	Full CAN controller. Low power.	V_{CC}: 3.3 V I/O (LV) TTL / CAN, SPI, SCI	100-pin PZ, 144-pin PGE
TMS320F28xx DSP Family	Dual CAN controller versions. Low power.	V_{CC}: 3.3-V I/O (LV) TTL / CAN, SPI, SCI	Multiple PGE, PZ, and LQFP packages
TMS470xxx	16/32-bit RISC flash microcontroller Dual CAN controller versions. Low-power modes.	V_{CC}: 3.3-V ARM7, CAN, 2 SPI, 2 SCI, ADC	Multiple PGE, PZ, and LQFP packages

2.4 ControlNet

ControlNet is an open standard network that meets the demands of industrial applications requiring high speed (5 megabits per second) and high throughput with predictable and repeatable transfers of mission critical data.

2.4.1 Electrical

ControlNet can be implemented on several different types of media, including copper coaxial cable, fiber-optic cable, and fiber ring, with variations for media redundancy and intrinsically safe applications. ControlNet supports a maximum of 99 nodes, with no minimum distance limitation between nodes. The most common media implementation uses transformer-coupled signals over coaxial cable. The 5-Mbps data is Manchester-encoded so that the bus levels change at 10 Mbps.

Texas Instruments supplies the only integrated ControlNet PHY (transceiver) available– the SN65HVD61.

2.4.2 Protocol

ControlNet is part of the Common Industrial Protocol (CIP) maintained jointly by ControlNet International and Open DeviceNet Vendors Association (ODVA). It offers high network efficiency with multicast of inputs and peer-to-peer data, using a Producer/Consumer communication model that allows the user to configure devices, control actions, and collect information over a single network.

2.4.3 Applicability

ControlNet meets the demands of real-time, high-speed applications at the automation and control layer for integration of complex control systems such as coordinated drive systems, weld control, motion control, vision systems, complex batch control systems, process control systems with large data requirements, and systems with multiple controllers and human-machine interfaces.

See the application report *ControlNet Applications with the SN65HVD61 PHY* (SLLA265) for further information.

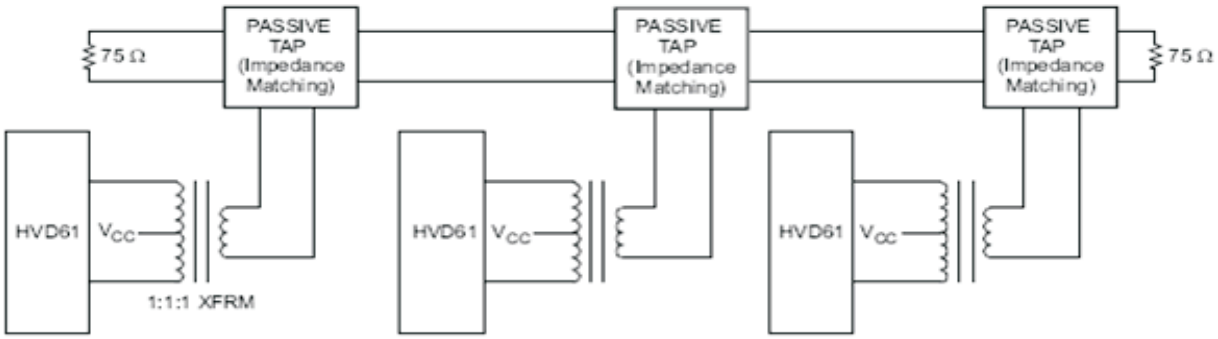


Figure 9. ControlNet Applications

2.5 Emitter-Coupled Logic (ECL) and Positive ECL (PECL)

2.5.1 Electrical

Emitter-coupled logic (ECL) is used in point-to-point, high-speed, differential-data transfer applications. A negative power scheme is used for ECL with VCC = 0 V and VEE = –5.2 V. ECL is typically used across a 50-Ω transmission medium using a 50-Ω to VEE termination. Typical output voltage swings for ECL are 800-mV peak or 1600-mV peak-to-peak allowing for greater transmission distances, whereas the output common mode is typically –1.3 V.

Positive/pseudo emitter-coupled logic (PECL) is used in point-to-point, high-speed, differential-data transfer applications. The opposite of ECL, PECL has a positive power supply scheme with VCC = 5 V and VEE = 0 V. PECL is typically used across a 50-Ω transmission medium using a 50-Ω to VCC-2-V termination. Typical output voltage swings for PECL are 800-mV peak or 1600-mV peak-to-peak allowing for greater transmission distances, whereas the output common mode is typically VCC – 1.3 V.

Low voltage positive/pseudo emitter-coupled logic (LVPECL) is used in point-to-point, high-speed, differential-data transfer applications. LVPECL takes PECL and allows for lower power supply ranges. The typical power supply range for LVPECL is VCC = 3.3 V and VEE = 0 V. LVPECL is typically used across a 50-Ω transmission medium using a 50-Ω to VCC-2-V termination. Typical output voltage swings for LVPECL are 800-mV peak or 1600-mV peak-to-peak allowing for greater transmission distances, whereas the output common mode is typically VCC – 1.3 V.

2.5.2 Applicability

Emitter-coupled logic (ECL) and positive/pseudo emitter-coupled logic (PECL) have been traditionally considered high-speed logic families that are applicable for use in high-speed communications data and clock links. Also, many high-speed clock distribution devices use xECL as its logic type due to its noise performance as well as its universal familiarity among the engineering community at large.

2.5.3 Features

Emitter-coupled logic (ECL) uses negative power supply rail, which historically had the advantage of improved noise immunity. Because the implementation of positive-supply technologies such as TTL and CMOS, the older technologies no longer provide a benefit, as a system using them requires several power supplies including the –5.2 V or –4.5 V needed for ECL.

As a result, ECL migrated to PECL, which allowed designers to move away from this negative supply rail and simplify board layout. The principle behind PECL was simply to keep the same output swing of 800 mV, but shift it to a positive voltage by using a 5-V rail and ground. LVPECL is the same concept as PECL, but uses a 3.3-V supply rather that the 5-V one. This results in a power consumption reduction relative to PECL. One of the key benefits that made xECL popular was its constant current requirement mostly independent of the switching circuit. This results in less noise and relatively constant (predictable) power usage, which are especially important for high data rate applications.

See *Interface Selection Guide* for a list of top PECL devices: www.ti.com/interface

2.6 General-Purpose Interface Logic

For a long time TTL-buses have been the standard solution for backplane systems. Different logic families are available to fulfill the requirement for backplane buses. The choice for the appropriate logic strongly depends on physical characteristics of the bus. The main factor is the number of receiving and transmitting modules connected into that bus. The more cards on the backplane, the lower the impedance of the bus due to additional capacitive loading. This arises from the input/output capacitance of the transceivers, the capacitance layer of printed-circuit stub lines and the connectors, resulting in the need for a higher drive capability of the logic device.

Mature 5-V TTL and 5-V CMOS as well as 3.3-V CMOS technologies provide a drive capability of 24 mA and can only handle line impedance down to about 50 Ω. With the introduction of BiCMOS technologies, the drive has been enlarged to –32/64 mA and with so-called incident wave switching drivers (SN74ABT25xxx). It is even possible to drive bus lines with an impedance as low as 25 Ω. The enhanced transceiver logic (ETL) features improved noise margins, while maintaining compatible TTL switching levels and therefore enabling higher speed on the backplane.

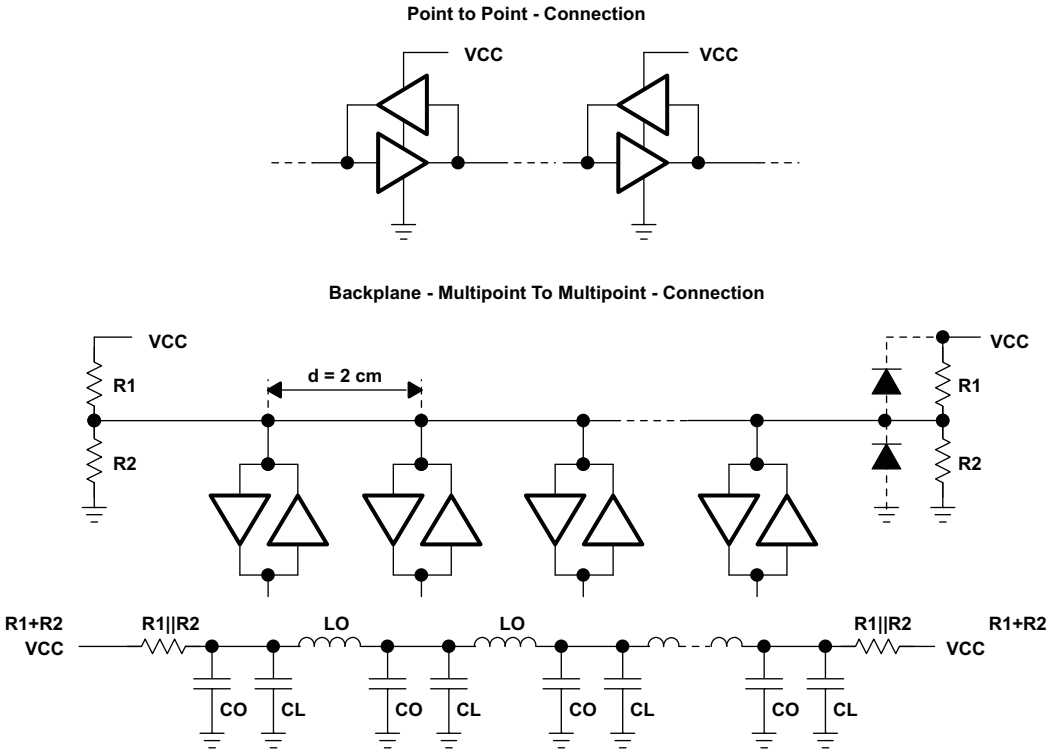


Figure 10. Point-to-Point Connection

Standard logic devices can be used for either point-to-point connections or to realize backplane buses, which consist of many drivers and receivers along the bus, as shown in Figure 10. Both solutions using standard logic devices are usually set up as parallel buses; up to 36 bits can be switched by one logic device. The operational frequency can be chosen within a range from a few MHz up to the clock frequency of about 50 MHz, such that the data throughput per device is in the range of 1 to 2 Gbps.

2.6.1 Electrical

The electrical specification of LVTTL levels meets the TTL specification. The combination of 5-V TTL with LVTTL is possible without any additional effort. Five-volt CMOS levels are not compatible with LVTTL levels. Five-volt tolerance is mandatory for unidirectional, and the use of 5-V level shifters is required for bidirectional data transfer, when combining a 3.3-V system with a 5-V-supplied system part. Table 4 shows the key parameters for 5-V and 3.3-V advanced system logic families. Another important feature is the live insertion capability of a logic family, which enables the user to insert and remove modules during operation. The important parameters are IOFF, power up/down 3-state, and precharge functionality as shown in Table 17. For more information about this topic, see the application report *Live Insertion* (SDYA012).

Table 4. Selected Characteristics for General-Purpose Logic Families

FAMILY	RECOMMENDED SUPPLY VOLTAGE	DRIVE (mA)	LEVELS	INTERFACING TO (LV) TTL	LIVE INSERTION, REMOVAL HOT INSERTION
AHC/LV	5 V	±8	5 V CMOS	Use level shifter	
AC	5 V	±24	5 V CMOS	Use level shifter	
ABT	5 V	–32/ +64	TTL	Yes	I_{OFF}, PU/D–3-state
ABT25	5 V	–80 (32)/+188 (64)			
ABTE	5 V	–60 (12)/ +90 (12)	ETL	Yes	I_{OFF}, PU/D–3-state and precharge
LVC	3.3 V	±24	LVTTL	Yes	I_{OFF}, (LVCZ: PU/D–3-state)
ALVC	3.3 V	±24	LVTTL	Yes	
LVT	3.3 V	–32/ +64	LVTTL	Yes	I_{OFF}, PU/D–3-state
ALVT	3.3 V	–32/ +64	LVTTL	Yes	I_{OFF}, PU/D–3-state
AVC	2.5 V	±12 + DOC™	2.5 CMOS	Yes	I_{OFF}, PU/D–3-state
AUC	1.8 V	±8	1.8 CMOS	Yes	I_{OFF}, PU/D–3-state

A maximum bus length is not specified for backplanes; however, in practice, the bus length of parallel backplanes does not exceed about 50 cm.

2.6.2 Applicability

The backplanes are not limited to any special domain. They are used in telecom, computer, and industry application, wherever several system parts are connected using a backplane or a memory bus. ABTE supports VME64.

2.6.3 Features

- 8-, 16-, and 32-bit devices enable parallel operation on the backplane/memory bus.
- Boundary scan devices (JTAG – IEEE 1149.1) available in LVT and ABT enable easy testability during design and production.
- Bus-hold feature eliminates external pullup resistor.
- Series damping resistors enable improved signal integrity in point-to-point buses.
- ABT, LVT, ALVT, and LVCZ incorporate power-up, 3-state outputs.
- ABTE supports precharge feature, enabling support hot swapping.
- LVC, ALVC are specified down to 1.8 V, further reducing power consumption.

Table 5. Top Feature List of Advanced System Logic by Logic Family

FUNCTION	AHC	AC	ABT	ABTE	(A)LVC	LVT	ALVT	AVC	AUC
Gates	n	n	n	N/A	n	N/A	N/A	N/A	n
Flip–flops	n	n	n	N/A	n	n	n	N/A	n
Drivers	n	n	n	n	n	n	n	n	n
Transceivers	n	n	n	n	n	n	n	n	n
UBT™ (1)	N/A	N/A	n	N/A	n	n	n	n	n
Bus hold (2)	N/A	N/A	n	n	n	n	n	n	n
26-Ω series resistors (3)	n	n	n	n	n	n	n	DOC™	n
SCOPE™ (4)	N/A	N/A	n	N/A	N/A	n	N/A	N/A	N/A

(1) The universal bus transceiver (UBTTM) combines D-type latches and D-type flip-flops for operation in transparent, latched or clocked mode.
(2) Bus hold on data inputs eliminates the need for external pullup resistors.
(3) 26-Ω series resistors are included in the output stages to match bus impedance and avoid external resistors.
(4) SCOPE™ products are compatible with the IEEE Standard 1149.1–1990 (JTAG) test access port and boundary scan architecture.

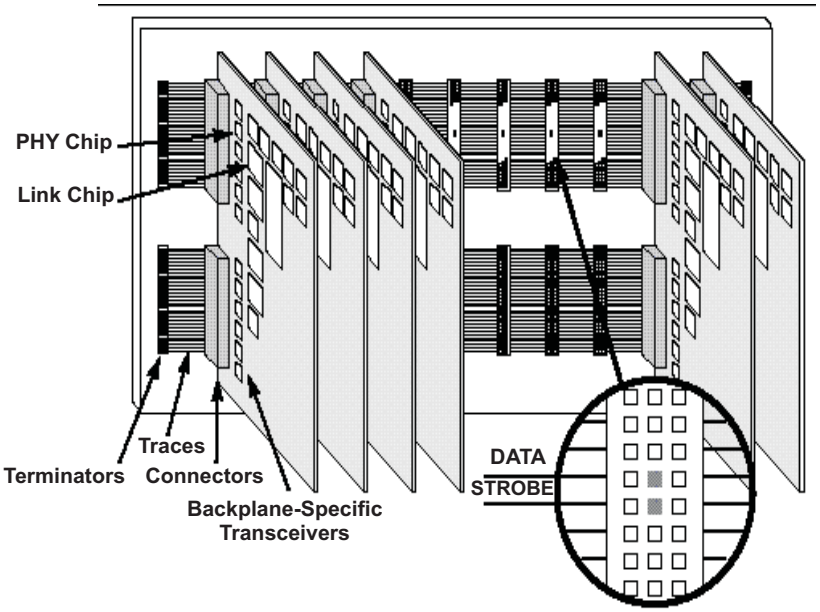


Figure 11. Typical Backplane Application Using Several Plug-In Cards

2.7 Gunning Transceiver Logic (GTL)

The basic concept of a GTL bus is similar to a BTL system and is shown in Figure 12.

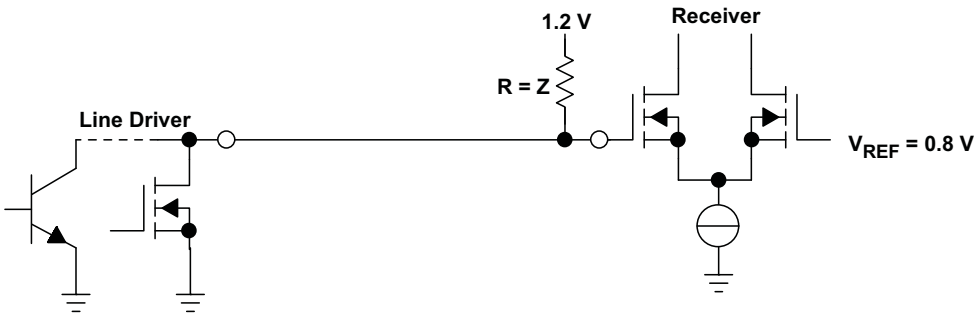


Figure 12. Principle Setup of an Open-Collector Bus System Using GTL Devices

Because of the missing diode in the open-collector/drain outputs (compared to the BTL– solution), the low level is 0.4 V. With a chosen high level of 1.2 V, the voltage swing is reduced to 0.8 V only. Again, the threshold is in the middle of the voltage swing at 0.8 V.

With a drive capability of GTL outputs up to about 40 mA, the GTL devices are able to drive a termination resistor of 0.8 V/40 mA = 20 Ω. If the bus line is terminated correctly, the lowest impedance that can be driven by a GTL driver in the middle of a bus is 40 Ω (effectively the driver sees: 40 Ω || 40 Ω = 20 Ω). As a result of the 0.8-V swing and the 40-mA IOL, the maximum power dissipation of one output is 16 mW. It is thus possible to integrate these low power drivers into ASICs.

2.7.1 Specialities of the GTL Device SN74GTL1655

With the SN74GTL1655, the benefits of the BTL family and GTL family are combined within one device. The drive capability of the SN74GTL1655 outputs now provides up to 100 mA, enabling the outputs to drive a termination resistor of 11 Ω.

With the GTL1655, even heavily loaded backplane buses can be served. For those buses, the line impedance can decrease down to 22 Ω.

All the features for live insertion and withdrawal have also been included in the GTL1655. The SN74GTL1655 further includes a selectable edge rate control (ERC) circuit for variable rise and fall rates so that the designers can fine-tune their circuits for maximum data throughput as system loading dynamically changes. The edge rate control minimizes bus-settling time.

2.7.2 Electrical

The gunning transceiver logic (GTL) devices support two different logic-level specifications: GTL (according EIA/JEDEC Standard EIA/JESD8-3) and the GTL + levels. The bus system is – similar to the BTL bus – realized as open-collector bus. No diode is included in the open-collector/drain output stage of the GTL-devices, such that the output low level can be reduced down to 0.4 V (GTL+: 0.55). With a chosen high level of 1.2 V for GTL (GTL+: 1.5 V), the voltage swing is reduced to 0.8 V (0.95 V) only. The threshold is in the middle of the voltage swing at 0.8 V (GTL+: 1 V).

GTL+ is becoming more and more a standard in the industry due to the enlarged noise margin of GTL+ levels. For example, GTL+ levels are being used on the Intel Pentium Pro (P6) processor to address this noise margin concern. By using GTL+ levels instead of GTL, the margin is increased about 16%.

2.7.3 Applicability

GTL was originally designed for a small bus on a board, for example, between a processor and its memory modules. Because the target application for GTL is not a backplane bus, but a bus on a board, no requirements for live insertion or withdrawal have been included in the specification.

With reduced output levels and state-of-the-art designs, the results are a reduction of power consumption, higher speeds, and improved signal integrity compared to the BTL bus, such that GTL+ backplane optimized-drivers are a premium solution for heavily loaded bus systems. Live insertion capabilities and an increased drive for low impedance backplanes are met with the GTL1655 device.

2.7.4 Features

- Differential amplifier ensures stable threshold voltage of the receiver.
- Low voltage swing generates low switching noise.
  - GTL: V_L = 0.4 V; V_H = 1.2 V
  - GTL+: V_L = 0.55 V; V_H = 1.5 V
- High drive capable option available, enabling incident wave switching as low as 10 Ω or 20 Ω || 20-Ω line impedance
  - GTL/GTL+: Low drive capability, I_{olmax} = 40/50 mA
  - GTL1655: High drive capability, I_{olmax} = 100 mA
- Correct line termination using a pullup resistor at the line end avoids line reflections.
- Edge-rate-control-output circuit of GTL1655 enables variable output slew rate depending on load condition for maximum data throughput.

Table 6. Top Device List GTL

DEVICE	SPECIFICATION	DESCRIPTION	PACKAGE	STATUS
SN74GTL16612	LVTTL /GTL	18-bit LVTTL /GTL+ universal bus transceivers, like 16601 function	56-pin SSOP 56-pin TSSOP	Available
SN74GTL1655	LVTTL /GTL	17-bit LVTTL /GTL+ universal bus transceivers with live insertion, like 16501 function	64-pin TSSOP	Available
SN74GTL16616	LVTTL /GTL	16-bit LVTTL /GTL+ universal bus transceivers with buffered clock outputs, like 16601 function	56-pin TSSOP 56-pin SSOP	Available
SN74GTL16622A	LVTTL /GTL	18-bit LVTTL /GTL+ bus transceivers, like 16601 function w/o LE and two CE	64-pin TSSOP	Available
SN74GTL16923	LVTTL /GTL	18-bit LVTTL /GTL+ bus transceivers, like 16601 function w/o LE and two OE	64-pin TSSOP	Available

2.8 Gunning Transceiver Logic Plus (GTLP)

GTLP devices are high-speed transceivers (LVTTL/card and GTLP/backplane) that operate like the GTL family with two major differences: they have been optimized for the distributed loads found in multislot backplanes, and they support live insertion with internal precharge circuitry. The GTLP reduced output swing (<1 V) and reduced input threshold levels allow higher backplane clock frequencies increasing the bandwidth for manufacturers developing next-generation telecommunication and data communication solutions. GTLP devices are backward-compatible with commonly used parallel backplane technologies such as ABT, FCT, LVT, ALVT, and FB+ and provide an alternative to more complex serial technologies.

GTLP offers two different drives, 50 mA and 100 mA at 0.55 V, to allow the designer flexibility in matching the device to backplane length, slot spacing, and termination resistor. The medium drive device can drive lines in point–to–point configurations down to 19 Ω. The lowest termination resistor that can be driven by the driver in the middle of a bus is 38 Ω (effectively the driver's load is 38 Ω || 38 Ω = 19 Ω). The high drive devices can drive loads of 9.5 Ω (0.95 V/100 mA). Therefore, the minimum termination resistor for bus configuration is 19 Ω. It is important to pick a termination resistor that matches the backplane impedance for best signal integrity but is within the capacity of the driver. Impedance is a function of natural trace impedance (Z_O), stub length, connector impedance, device impedance, and card spacing. Closer spacing reduces the effective impedance, which requires a smaller termination resistor as shown in Figure 13.

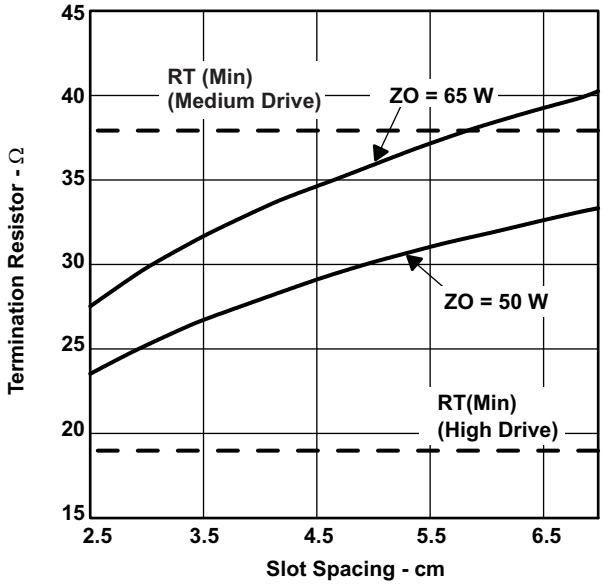


Figure 13. R_T Versus Slot Spacing With GTLP Medium and High Drive Devices

To enhance the data throughput of a GTLP backplane a source synchronous clock layout is advised. Because the clock signal is sent from the same source, the flight time over the bus is eliminated in the timing budget. This roughly doubles the data throughput of the backplane. TI offers a special device, the GTLPH1627 and GTLPH16927, which has one bit integrated for the source synchronous clock. It also features a flexible set-up time adjustment (FSTA), which offers the designer an easy way to implement a source synchronous bus.

2.8.1 Electrical

Optimized for the GTLP signal level specifications, also operates at GTL (according JEDEC Standard JESD8–3) or GTL+ signal levels. The bus system, identical to the GTL bus, is realized as an open-drain bus. The GTLP voltage swing is from 1.5 V to 0.55 V with ±50 mV around the V_{REF} threshold of 1 V.

2.8.2 Applicability

GTLP is used where the major concerns are higher data throughput, live insertion capability, or lower power consumption in parallel backplane architectures. GTLP offers up to four times the performance of TTL devices in backplane upgrade applications.

2.8.3 Features

- 3.3-V operation with 5-V tolerant LVTTL inputs/outputs, which allow the devices to act as 5-V TTL to GTLP as well as 3.3-V LVTTL to GTLP translators
- Significantly improved output edge control (OEC) circuitry on the rising and falling edge of the GTLP outputs reduces line reflections, electromagnetic interference (EMI) and improves overall signal integrity allowing clock frequencies in excess of 80 MHz, with source synchronous clock layout even in excess of 120 MHz
- Fully supports live insertion with I_{off}, PU3S and BIAS V_{CC} circuitry
- Edge rate control (ERC) circuitry on high drive devices allows fast or slow edge rates.
- CMOS construction for 1/3 the static power consumption of BiCMOS logic devices
- A-port (LVTTL side) balanced drive of ±24 mA with optional bus-hold circuitry

Table 7. Top Device List GTLP

DEVICE	SPECIFICATION	DESCRIPTION	PACKAGE	STATUS
SN74GTLPH306	LVTTL /GTLP	8-bit LVTTL /GTLP medium drive bus transceivers	24-pin SOIC 24-pin TSSOP 24-pin TVSOP	Available
SN74GTLP817	LVTTL /GTLP	GTLP/LVTTL medium drive with ERC 1:6 fan-out driver	24-pin SOIC 24-pin TSSOP 24-pin TVSOP	Available
SN74GTLP2033	LVTTL /GTLP	8-bit Registered Transceiver with Split LVTTL Port and Feedback Path and ERC	48-pin TSSOP 48-pin TVSOP 56-ball VFBGA	Available
SN74GTLP2034	LVTTL /GTLP	8-bit Registered Transceiver with Split LVTTL Port and Feedback path and ERC	48-pin TSSOP 48-pin TVSOP 56-ball VFBGA	Available
SN74GTLP21395	LVTTL /GTLP	Two 1-bit Transceiver with Split LVTTL Port, Feedback Path and Selectable Polarity	20-pin SOIC 20-pin TSSOP 20-pin TVSOP 20-ball VFBGA	Available
SN74GTLP22033	LVTTL /GTLP	8-bit Registered Transceiver with Split LVTTL Port and Feedback path and ERC	48-pin TSSOP 48-pin TVSOP 56-ball VFBGA	Available
SN74GTLP22034	LVTTL /GTLP	8-bit Registered Transceiver with Split LVTTL Port and Feedback path and ERC	48-pin TSSOP 48-pin TVSOP 56-ball VFBGA	Available
SN74GTLPH16912	LVTTL /GTLP	18-bit LVTTL /GTLP medium drive universal bus transceivers	56-pin TSSOP 56-pin TVSOP	Product Preview available
SN74GTLPH16916	LVTTL /GTLP	17-bit LVTTL /GTLP medium drive universal bus transceivers with Buffered Clock Outputs	56-pin TSSOP 56-pin TVSOP	Available
SN74GTLPH16927	LVTTL /GTLP	18-bit LVTTL/GTLP medium drive transceiver with Source Synchronous Clock Outputs, FSTA	56-pin TSSOP 56-pin TVSOP	Product Preview
SN74GTLPH16945	LVTTL /GTLP	16-bit LVTTL /GTLP medium drive bus transceivers	48-pin TSSOP 48-pin TVSOP	Available
SN74GTLPH32912	LVTTL /GTLP	36-bit LVTTL /GTLP medium drive universal bus transceivers	114-ball LFBGA	Available
SN74GTLPH32916	LVTTL/GTLP	34-bit LVTTL /GTLP medium drive universal bus transceivers with Buffered Clock Outputs	114-ball LFBGA	Available
SN74GTLPH32945	LVTTL /GTLP	32-bit LVTTL /GTLP medium drive universal bus transceivers	96-ball LFBGA	Available
SN74GTLP1394	LVTTL /GTLP	2-bit LVTTL /GTLP high drive bus transceivers with ERC	16-pin SOIC 16-pin TSSOP 16-pin TVSOP	Available
SN74GTLP1395	LVTTL /GTLP	Two 1-bit LVTTL/ high drive bus transceivers with ERC	20-pin SOIC 20-pin TSSOP 20-pin TVSOP 20-ball VFBGA	Available

Table 7. Top Device List GTLP (continued)

DEVICE	SPECIFICATION	DESCRIPTION	PACKAGE	STATUS
SN74GTLPH1612	LVTTL /GTLP	18-bit LVTTL /GTLP high drive universal bus transceivers with ERC	64-pin TSSOP	Available
SN74GTLPH1616	LVTTL/GTLP	17-bit LVTTL /GTLP high drive universal bus transceivers with Buffered Clock Outputs	64-pin TSSOP	Available
SN74GTLPH1627	LVTTL/GTLP	18-bit LVTTL/GTLP high drive transceiver with Source Synchronous Clock Outputs, FSTA	56-pin TSSOP 56-pin TVSOP	Product Preview
SN74GTLPH1645	LVTTL /GTLP	16-bit LVTTL /GTLP high drive bus transceivers with ERC	56-pin TSSOP 56-pin TVSOP 56-ball VFBGA	Available
SN74GTLPH1655	LVTTL /GTLP	16-bit LVTTL /GTLP high drive universal bus transceivers with ERC	64-pin TSSOP	Available
SN74GTLPH3245	LVTTL /GTLP	32-bit LVTTL /GTLP high drive bus transceivers with ERC	114-pin LFBGA	Available
SN74GTLPH16612	LVTTL /GTLP	18-bit LVTTL /GTLP medium drive universal bus transceivers	56-pin SSOP 56-pin TSSOP	Available

2.9 IEEE1284-Compatible Devices

The IEEE1284 standard provides an open path for communication between computers and intelligent printers and peripherals. The release of the standard signaling method for a bidirectional parallel peripheral interface for personal computers defines a common standard for bidirectional parallel communications between personal computers and peripherals. Preexisting methods used a wide variety of hardware and software products, each with unique and – in most cases – incompatible signaling schemes. An example is the Centronics printer port. An official standard for this printer port never existed. Therefore, problems in circuit designs occurred due to unknown hardware design elements, such as termination resistors or driver output impedance. For safe data transmission, only a short cable between host and peripheral (1 to 2 m) was acceptable. The release of the IEEE1284 standard answers the demand for an industry-wide, high-speed, high-integrity parallel port standard for a bidirectional peripheral interface. Texas Instruments offers three bus drivers. They support reliable data transfer through cables lengths up to 10 meters (30 feet) at a speed of 16 Mbps.

2.9.1 Electrical

The IEEE1284 specification defines the physical setup of the 1284 interface including wiring diagram, minimum drive capabilities, and termination considerations.

2.9.1.1 Applicability

The ’1284-compatible devices are widely used from computer and peripheral manufacturers, because the ’1284 standard can communicate more than 50 times faster than conventional parallel port interfaces. The protocol is defined in the IEEE1284 standard.

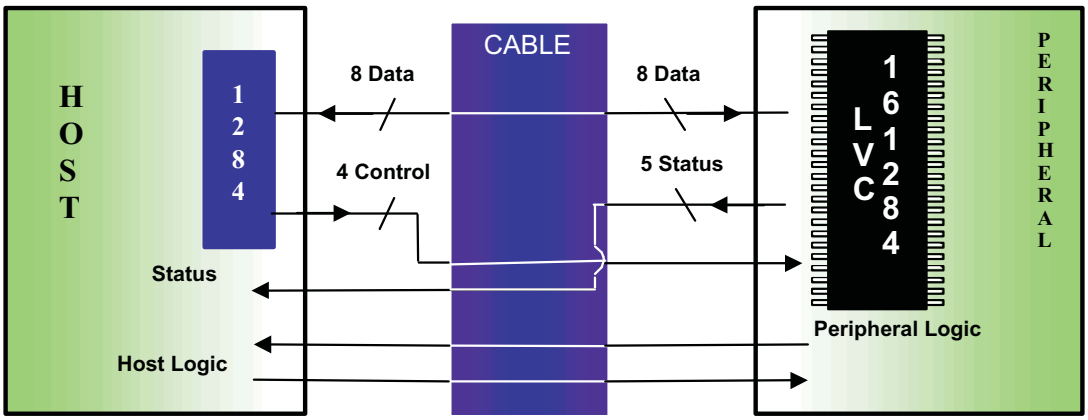


Figure 14. Typical Application Showing a 1284 Interface

2.9.2 Features

- Designed for the IEEE Std 1284–I (Level 1 Type) and IEEE Std 1284–II (Level 2 Type) electrical specifications
- Adds bidirectional capabilities to the existing Centronics parallel interface
- Supports five modes of data transfer (Centronics; Nibble; Byte; EPP; ECP)
- Advanced operating mode can reach speeds of 16 to 32 Mbps
- New electrical interface, cabling, and connector for improved performance and reliability while retaining backward compatibility
- 50 to 100 times faster than the original parallel port (Centronics)

Table 8. Top Device List – IEEE 1284–Compatible Devices

DEVICE	SPECIFICATION	DESCRIPTION	PACKAGE	STATUS
SN74ACT1284	TTL	7-bit bus interface with 3-state outputs	20-pin SOIC 20-pin SSOP 20-pin TSSOP 20-pin SO	Available
SN74LVC161284	LVTTL	19-bit bus interface	48-pin SSOP 48-pin TSSOP	Available
SN74LV161284	LVTTL	19-bit bus interface	48-pin SSOP 48-pin TSSOP	Available
SN74LVCZ161284A	LVTTL	19-bit bus interface with error free power-up	48-pin TSSOP	Available
SN74LVCE161284	LVTTL	19-bit bus interface with error free power-up and 15KV ESD protection	48-pin SSOP 48-pin TSSOP 48-pin TVSOP	Available

2.10 Local Interconnect Network (LIN)

The local interconnect network (LIN) was defined by a consortium of car makers, suppliers, and semiconductor companies. It is a concept for a low-cost automotive network that complements the existing portfolio of automotive multiplex networks by replacing complex power wiring harnesses with a bus and smart actuators and sensors. LIN is implemented as a sub-bus in a hierarchical vehicle network in order to provide quality enhancement and cost reduction in vehicles. The LIN standard includes the specification of the transmission protocol, the transmission medium (physical layer), the interface between development tools, and the interfaces for software programming. LIN promotes the interoperability of network nodes from the viewpoint of hardware and software and a predictable EMC behavior.

The specification calls for signaling rates up to 20 kbps using a single wire, high immunity to electrical interference, low electromagnetic emissions, and high ESD robustness. LIN is a single master with multiple slaves concept making it an ideal local sub-bus to the higher speed controller area network (CAN) typically used in the vehicle. The protocol may be implemented based on low-cost UART/SCI interface hardware, software equivalent, or as an embedded state machine. The LIN specification also provides a transport layer and diagnostic support.

LIN's simplicity and low-cost overhead makes it ideally suited in applications requiring a low number of small messages in a scheduled time with high reliability and low cost.

2.10.1 Electrical

The LIN standard defines half-duplex, single-ended transmission on cable lengths up to 40 meters with a maximum of 16 nodes at signaling rates up to 20 kbps. Additional nodes can be added but they lower bus impendence by approximately 3% per node. LIN is specified for reference to the vehicle battery voltage of 8 V to 18 V. However, with careful design, this can be extended to support commercial vehicles up to 27 V, but as always this involves a trade-off in signaling rate. A single cable with capacitance of 150 pF/m maximum is specified as the interconnect with a total bus capacitance of 10 nF. The bus is terminated at

the master node with a 1-kΩ pullup resistor and at each slave node with 30 kΩ. Nodes are connected to the bus through stubs. Data transmission circuits employing LIN are used in applications requiring a rugged interconnection, so robustness has been defined within the electrical layer and is designed into the physical layer transceivers. It withstands a wide input voltage range, has a wide short-circuit and transient voltage range, high ESD, and wide ground shifts to help ensure data integrity.

2.10.2 Protocol

The LIN communications protocol describes how information is passed between devices on a network and conforms to the open systems interconnection (OSI) model that is defined in terms of layers. LIN 2.1 defines the functions of the lower layers of the OSI model that are performed within a LIN controller. An abundance of LIN programming routines is available from various vendors.

2.10.3 Applicability

The robust features of LIN make it ideally suited for the many rugged applications to which the LIN protocol is being adapted. Although it was developed within the automotive market, it is beginning to find additional uses in trucks, buses, agriculture, and marine vehicles. LIN-based control systems can be developed for other applications where low data rate, single wire, and low cost are key concerns.

2.10.4 Features

- Established standard and standardized products
- Fault tolerant – high short-circuit protection
- Robust interface for harsh electrical environments

Table 9. LIN Device List

DEVICE	FEATURES	SUPPLY	PACKAGE
TPIC1021x-Q1 LIN Transceiver Family	High-temperature range and short-circuit protection. Low power sleep mode with wake up from LIN bus or HV input	VSUP: 7 V to 27 V I/O: 3 V to 5.25 V	8-pin SOIC
TMS470 MCU Family	Full LIN 2.0 controller. Low power modes	Single 3.3 V or 3.3 V I/O and 1.8-V core	80-, 100-, 144-pin LQFP
TMS570 MCU Family	Full LIN 2.0 controller. High performance.	3.3-V I/O and 1.5-V core	128-, 144-, 176-pin LQFP 208-, 256-, 324-ball BGA

2.11 Low-Voltage Differential-Multipoint (LVDM)

LVDM stands for LVDS-multipoint, enabling a half-duplex operation with LVDS voltage levels and speeds. It benefits from the same advantages as LVDS. Additionally, it allows bidirectional data transfer and the attachment of several drivers, receivers, and/or transceivers. LVDM is a LVDS-multipoint option exclusively available from TI. Meanwhile, a new standard has been released, following the industry demand for standardized multipoint-LVDS, including definitions such as bus contention-prevention, and so forth, which are of high importance when mixing devices of multiple suppliers. The next section addresses M-LVDS. As the devices following the new standard provide an higher output drive capability than LVDM, for some applications where power consumption and heat sinking is of concern, LVDM may still be an option versus M-LVDS. Existing products will remain available.

2.11.1 Electrical

LVDM is LVDS with doubled driver output current. For bidirectional transfers, a termination is needed at each end of the line. The requirement of termination matching the line impedance remains. Therefore, both ends are terminated with 100-Ω. The effective termination resistance results in the parallel configuration of these two resistors, equaling half the impedance or twice the load. To ensure the same input voltage levels like with LVDS (that is, at a 100-Ω load), the output current is doubled to generate the required amplitude on just 50 Ω.

2.11.2 Applicability

LVDM can be used as a replacement for TIA/EIA–485 interconnections, especially for high-speed, low-power, and/or low EMI interfaces. As the physical parameters on the line are identical with LVDS, regular LVDS receivers may be used. This way, common-mode input range is between 0 V and 2.4 V, which limits the line length and the applicability in a electrically noisy environment. It is suited for backplane applications and cabled interfaces.

2.11.3 Features

- Drives double-terminated multipoint
- Very high speed
- Very low power consumption
- Very low EMI
- Low cost

Table 10. TOP LVDM Device List

DEVICE	FEATURES	SUPPLY	PACKAGE
SN65LVDM176	Single-Channel Transceiver	VCC: 3.3 V I/O: LVTTL /LVDM	8-pin SOIC
SN65LVDM1676 / 1677	16-Channel Transceiver	VCC: 3.3 V I/O: LVTTL /LVDM	64-pin TSSOP
SN65LVDM050	Dual-Channel Driver – Receiver	VCC: 3.3 V I/O: LVTTL /LVDM	16-pin SOIC
SN65LVDM320	Octal Latched Transceiver	VCC: 3.3 V I/O: LVTTL /LVDM	64-pin TSSOP
SN65LVDM31	Quad Driver	VCC: 3.3 V I/O: LVTTL /LVDM	16-pin SOIC

2.12 Stub Series Terminated Logic (SSTL)

Stub series terminated low-voltage logic (SN74SSTVxxx) designers are constantly trying to get the most out of their designs in the most cost-effective means. As faster versions of a particular CPU become available, the designer often tries to improve the throughput of an existing design simply by increasing the CPU clock frequency.

These issues resulted in JEDEC defining two SSTL switching standards (SSTL_3, EIA/ JESD8–8, SSTL_2, EIA/ JESD8-8). Both standards specify a particular termination scheme with appropriate values for the resistors and capacitors.

The SSTL interface standard is intended for high-speed memory interface applications and specifies switching characteristics such that operating frequencies up to 200 MHz are attainable. The primary application for SSTL devices is to interface with SDRAMs.

A two-resistor network is used to establish a voltage level such that differential voltage swings can be used and two different resistor value configurations can be acceptable.

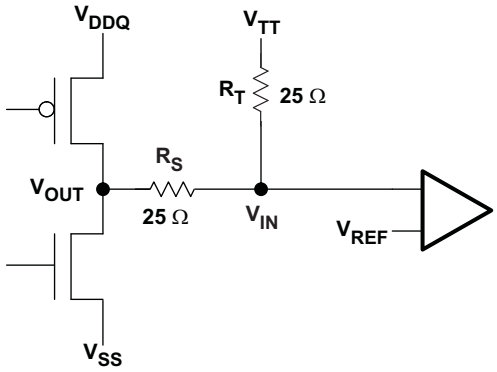


Figure 15. Typical Output Buffer Environment, Class II of SSTL Standard

Class I specifies an acceptable value of 50 Ω for the termination resistor R_T, and Class II specifies an acceptable value of 25 Ω. Figure 15 shows the typical dc environment for the output buffer (Class II); in this case, an additional series resistor R_S is specified at 25 Ω. To meet the 400-mV minimum requirement for VIN, a minimum of 8 mA must be driven into R_T, if R_T equals 50 Ω (Class I); or 16 mA if R_T equals 25 Ω (Class II). The standard states that for each value of R_T, a capacitive load equal to 10 pF or 30 pF can be used. The SSTL16837A supports both SSTL and LVTTL switching levels. Although the data sheet provides specifications where SSTL levels are used for the input and output levels, the device can operate under any combination of SSTL/LVTTL levels for the inputs and the outputs. When SSTL levels are applied to the device, it functions approximately 2 ns faster than using LVTTL levels.

2.12.1 Electrical

The stub series terminated logic (SSTL) interface standard is intended for high-speed memory interface applications and specifies switching characteristics such that operating frequencies up to 200 MHz are attainable. The input high and low voltage levels (V_{IH} and V_{IL}) are V_{REF} +200 mV and V_{REF} –200 mV, resulting in a worst-case noise margin of 25%. This seems to be a relatively small noise margin, but because it is a terminated bus, the actual noise source has to be a high current to produce 400 mV across the relatively low-impedance termination.

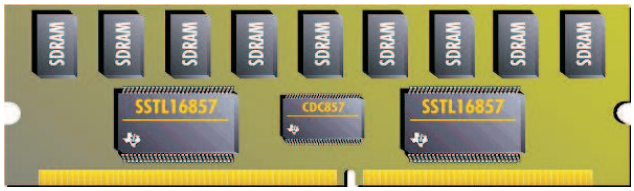
All totem-pole outputs of the SSTL-compatible devices have a dedicated V_{DDQ} supply that (as stated in the SSTL_3 and SSTL_2 JEDEC standards) can be lower than or equal to V_{DD}, but never greater than V_{DD}. This feature allows the internal circuitry supply voltage to be raised to 3.6 V for maximum speed performance, while lowering V_{DDQ} to prevent the device from dissipating large amounts of power in the output stage.

Regardless of the input and output switching levels, the characteristic high-level and low-level output drive current of 20 mA is maintained.

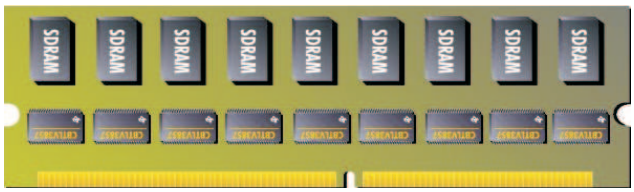
2.12.2 Applicability

Figure 16 shows a complete DDR SDRAM (SDRAM II) memory interfacing solution offered from Texas Instruments. Using a specially designed register, low-voltage bus switches, and a differential clock, DDR SDRAM modules can achieve double the memory data rate by allowing the SDRAMs to operate at twice their system frequency using the rising and the falling edge of the system clock.

The 14-bit registered buffer SSTL16857 is designed for 2.3-V to 3.6-V VCC operation and differential data input and output levels. It buffers DDR SDRAM address and control signals. The CDC857 differential clock completes the TI solution for 184-pin DDR SDRAM modules. Optionally, the SSTL_2 optimized CBTLV3857 provides bus isolation in the DDR SDRAM DIMM application and reduces the capacitive loading on the data lines.



Front View



Back View

Figure 16. DDR SDRAM Memory Interfacing Solution Using the SN74SSTL16857

2.12.3 Features

- Maximum frequency of 200 MHz enables fast DDR SDRAM memory buses.
- Supports both SSTL and LVTLL switching levels, which enables any combination of SSTL and LVTTL levels for inputs and outputs
- SSTL and LVTTL levels for inputs and outputs
- Outputs have dedicated V_{DDQ}, which can be lower or equal to V_{DD}. This enables the internal circuitry supply voltage to be raised to 3.6 V for maximum speed, while lowering V_{DDQ} to prevent the device from large power dissipation in the output stage.

Table 11. Top Device List for Stub Series Termination Logic

DEVICE	SPECIFICATION	DESCRIPTION	PACKAGE	STATUS
SN74SSTL16837A	SSTL_3	20-bit SSTL_3 interface universal bus driver with 3–state outputs	64-pin TSSOP	Available
SN74SSTL16847	SSTL_3	20-bit SSTL_3 interface buffer with 3–state outputs	64-pin TSSOP	Available
SN74SSTL16857	SSTL_2	14-bit SSTL_2 registered buffer	48-pin TSSOP	Available
SN74SSTV16857	SSTL_2	14-bit registered buffer with SSTL_2 inputs and outputs	48-pin TSSOP or TVSOP	Available
SN74SSTV16859	SSTL_2	13-bit registered buffer with SSTL_2 inputs and outputs	48-pin TSSOP	Available
SN74SSTV32852	SSTL_2	24-bit registered buffer with SSTL_2 inputs and outputs	114-ball LFBGA	Available
SN74SSTV32867	ULTTL	26-bit registered buffer with SSTL_2 inputs and LVCMOS outputs	96-ball LFBGA	Available
SN74SSTV32877	SSTL_2	26-bit registered buffer with SSTL_2 inputs and outputs	96-ball LFBGA	Available

Table 11. Top Device List for Stub Series Termination Logic (continued)

DEVICE	SPECIFICATION	DESCRIPTION	PACKAGE	STATUS
SN74SSTVF16857	SSTL_2	14-bit registered buffer with SSTL_2 inputs and outputs	48-pin TSSOP or TVSOP	Available

2.13 TIA-232 (RS-232)

Usually, it is based on or is identical to other standards (for example, the EIA/TIA-232-F). The following section gives a closer view of these specifications, their benefits, and applicability. Where appropriate, the protocol is briefly described.

TIA/EIA-232, previously known as RS-232, was developed in the 1960s to interconnect layers of the interface (ITU-T V.11). It specifies the pinout of the appropriate connectors (25-pin D-type or 9-pin DB9S) (ISO 2210) and the protocol (ISSUED-T V.24). The control lines data carrier detect (DCD), data set ready (DSR), request to send (RTS), clear to send (CTS), data terminal ready (DTR), and the ring indicator (RI) might be used, but do not necessarily have to be (for example, the PC-serial-mouse uses only RI, TD, RD, and GND). Although the standard supports only low-speed data rates and line length of approximately 20 m maximum, it is still widely used. This is due to its simplicity and low cost.

2.13.1 Electrical

TIA-232 has high signal amplitudes of ±5 V to 15 V at the driver output. The triggering of the receiver depends on the sign of the input voltage: that is, it senses whether the input is above 3 V or less than –3 V. The line length is limited by the allowable capacitive load of less than 2500 pF. This results in a line length of approximately 20 m. The maximum slope of the signal is limited to 30 V/μs. The intention here is to limit any reflections that can occur to the rise and fall times of the signal. Therefore, transmission line theory does not need to be applied, so no impedance matching and termination measures are necessary. Due to the voltage swings of –5...15 to 5...15 V, a dual-supply voltage was necessary in the past. Nowadays, many devices operate with single supplies, generating the large positive and negative driver output voltage swings with integrated charge pumps.

2.13.2 Applicability

Different from other purely electrical-layer standards, TIA-232 defines not only the physical layer of the interface (ITU–T V.11), but also the pinout of the appropriate connectors (25-pin D-type or 9-pin DB9S) (ISO 2210) and the protocol (ITU-T V.24). The interface standard specifies also handshake and control lines in addition to the two unidirectional receive data (RD) line and transmit data (TD) line.

TIA-232 is historically associated with computers interfacing with peripherals at low speed and short distance (for example, a mouse, a modem, a joystick, and so forth) or to interconnect two PCs (that is, null modem, Figure 17).

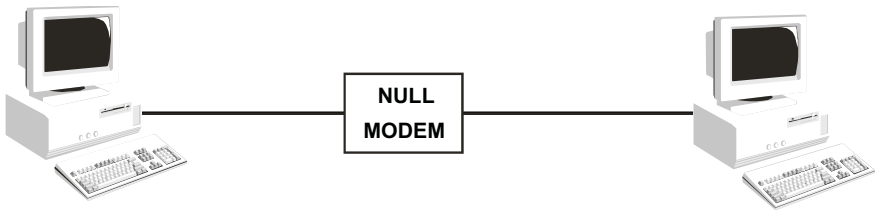


Figure 17. Null Modem Application Using RS232

2.13.3 Features

- Established standard
- Inexpensive
- Universally used

Table 12. Top TIA/EIA-232 Device List

DEVICE	BIT WIDTH	POWER	PACKAGE
MAX3221	1 driver/1 receiver	VCC: 3.3 V, 5 V I/O: LVTTL / RS232 250 kbps	16-pin SSOP, TSSOP
MAX3222	2 drivers/2 receivers	VCC: 3.3 V, 5 V I/O: LVTTL / RS232 250 kbps	20-pin SOIC, SSOP, TSSOP
MAX3223	2 drivers/2 receivers	VCC: 3.3 V, 5 V I/O: LVTTL / RS232 250 kbps	20-pin SOIC, SSOP, TSSOP
MAX3232	2 drivers/2 receivers	VCC: 3.3 V, 5 V I/O: LVTTL / RS232 250 kbps	16-pin SOIC, SSOP, TSSOP
MAX3238	5 drivers/3 receivers	VCC: 3.3 V, 5 V I/O: LVTTL / RS232 250 kbps	28-pin SSOP, TSSOP
MAX3243	3 drivers/5 receivers	VCC: 3.3 V, 5 V I/O: LVTTL / RS232 250 kbps	28-pin SSOP, TSSOP
SN75C3221	1 driver/1 receiver	VCC: 3.3 V, 5 V I/O: LVTTL / RS232 1 Mbps	16-pin SSOP, TSSOP
SN75C3222	2 drivers/2 receivers	VCC: 3.3 V, 5 V I/O: LVTTL / RS232 Mbps	20-pin SOIC, SSOP, TSSOP
SN75C3223	2 drivers/2 receivers	VCC: 3.3 V, 5 V I/O: LVTTL / RS232 1 Mbps	20-pin SOIC, SSOP, TSSOP
SN75C3232	2 drivers/2 receivers	VCC: 3.3 V, 5 V I/O: LVTTL / RS232 1 Mbps	16-pin SOIC, SSOP, TSSOP
SN75C3238	5 drivers/3 receivers	VCC: 3.3 V, 5 V I/O: LVTTL / RS232 Mbps	28-pin SOIC, SSOP, TSSOP
SN75C3243	3 drivers/5 receivers	VCC: 3.3 V, 5 V I/O: LVTTL / RS232 Mbps	28-pin SOIC, SSOP, TSSOP
SN75C23243	6 drivers/10 receivers	VCC: 3.3 V, 5 V I/O: LVTTL / RS232 25kbps	48-pin SSOP, TSSOP

2.14 TIA/EIA-422 (RS-422)

TIA/EIA-422 (RS-422) allows a multidrop interconnection of one driver, transmitting unidirectional up to 10 receivers. Although it is not capable of bidirectional transfer, it is still applicable and used for talker-audience scenarios.

2.14.1 Electrical

RS-422 (ITU-T V.11) is limited to unidirectional data traffic and is terminated only at the line-end opposite to the driver (see the preceding explanation of the distributed simplex mode, Section 1.2). Line length to 1200 m is possible and, over shorter distances, signaling rates of 10 Mbps are common. RS-422 allows up to ten receivers (input impedance of 4 kΩ attached to one driver. The maximum load is limited to 80 Ω whereas the output needs to supply amplitude of 2 V minimum. The receivers of RS-422 detect the bus state with as little as 200-mV differential and up to 7 V of common-mode signal.

2.14.2 Applicability

RS-422 is most commonly used in DTE-to-DCE interface in telecommunications but has general applicability to any simplex or distributed simplex bus where a direct connection is desired in the presence of ground noise.

2.14.3 Features

- Established standard
- Good for multidrop over long distances
- Good for use in noisy environments

Table 13. Top RS-422 Device

DEVICE	BIT WIDTH	POWER	PACKAGE
AM26LS31	4 drivers	VCC: 5 V, I/O: (LV)TTL /RS-422	16-pin PDIP and SOIC
AM26LS32A	4 receivers	VCC: 5 V, I/O: (LV)TTL /RS-422	16-pin PDIP and SOIC
SN75ALS192	4 drivers	VCC: 5 V, I/O: (LV)TTL /RS-422	16-pin PDIP and SOIC

2.15 TIA-485 (RS-485)

RS-422 was published before RS-485. Due to the lack of bidirectional capabilities allowing for multipoint connections, a new standard adding this feature was created: RS-485 . The standard (RS-485-A or ISO/IEC 8284) defines the electrical characteristics of the interconnection, including driver, line, and receiver. It allows data rates in the range of 35 Mbps and above and line lengths of up to 1200 m. Of course, both limits cannot be reached at the same time. Recommendations are given regarding wiring and termination. The standard does not specify the connector or any protocol requirements.

2.15.1 Electrical

RS-485 describes a half-duplex, differential transmission method designed for twisted-pair cables and other balanced media. The standard requires drivers to deliver a minimum differential output voltage of 1.5 V with up to 32 unit loads of about 12 kΩ each, plus termination resistors at each end of the bus. Connection of more than 32 nodes is possible if fractional unit-load devices are used. The common-mode voltage levels on the bus may vary between –7 V and 12 V, and receivers must be sensitive enough to determine the bus state based on a differential signal level of 200 mV.

2.15.2 Applicability

Due to its differential transmission form, RS-485 is robust against electrical noise corruption. Due to its wide common-mode voltage range, it is tolerant to ground potential shifts between nodes. For both of these reasons, this standard is perfectly suited for applications desiring low noise emissions and susceptibility. This is especially valuable in long lines. In most applications, the signaling rate is sufficient, for example, to control a process line. RS-485 is also used in backplane connections; its high node count and data integrity are necessary features for these applications.

No particular protocol is specified in the standard. However, many popular protocol standards refer to RS-485 as an electrical-layer solution. These include Profibus (EN 50170), Interbus-S, and MODBus.

2.15.3 Features

- Very robust interface (common mode range: –7 V to 12 V)
- Low radiated emissions
- High noise tolerance
- Half- or full-duplex (multiplex) mode of operation
- Up to 256 nodes with 1/8th Unit Load (UL) transceivers

Table 14. Top RS-485 Device List

DEVICE	FUNCTION	POWER	PACKAGE
SN65HVD1x	Single-Channel Transceivers	VCC: 3.3 V	8-pin SOIC
SN65HVD2x	Single-Channel, wide Common Mode Transceiver, SN65HVD23, SN65HVD24 with receiver equalization	VCC: 5 V	8-pin SOIC and MSOP
SN65HVD3082	Single-Channel, low power transceiver	VCC: 5 V	8-pin SOIC
SN65HVD17xx	Single-Channel transceivers with 70-V bus pin survivability	3.3 V and 5 V	8-pin SOIC and 14-pin SOIC

2.16 TIA-644 (LVDS)

Low-voltage differential signaling (LVDS) is an approach to achieve higher signaling rates on commonly used media. Because the limitation of the previously known differential standards is mainly related to the maximum achievable slew rate and EMI restrictions, LVDS targets low-voltage swings that are reached much faster, enabling higher speeds, lower EMI, and lower power consumption.

2.16.1 Electrical

As the name says, LVDS uses differential transmission mode and low signal amplitudes. The swing is in the range of only 350 mV, generated on a 100-Ω termination resistor. The driver may also be a current-mode driver forcing an output current between 2.47 mA and 4.54 mA into either one of the two outputs. This benefits in higher speed, lower power consumption and reduced EMI. More information on EMI comparisons can be found in application report *Reducing Electromagnetic Interference With Low Voltage Differential Signaling* (SLLA030) . The common-mode range of LVDS is specified as 0 V to 2.4 V, but devices are available already that allow for larger offsets (–4 V to 5 V). Figure 18 shows the dependency of the supply current versus the switching frequency for HVD (RS-422), LVDS, and PECL. As can be seen, the supply current is significantly lower and the increase over frequency is much lower with the use of LVDS drivers.

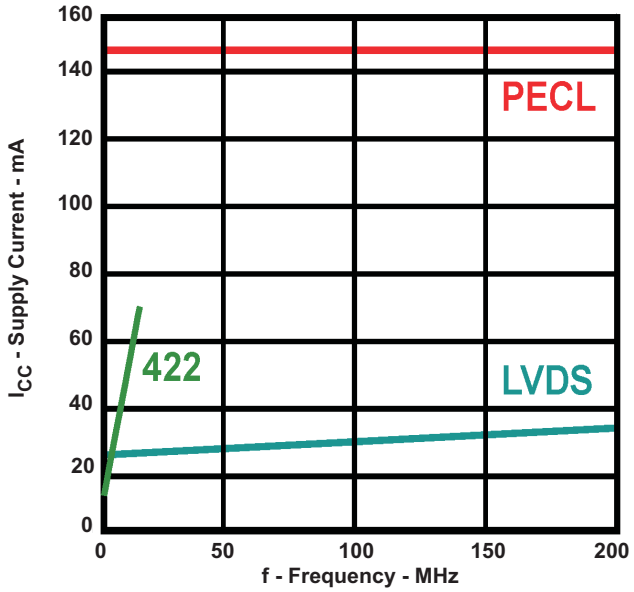


Figure 18. Supply Current Versus Switching Frequency

The initial specification, TIA-644, addresses only point-to-point interfaces, but it allows the attachment of multiple receivers if attention is paid to several conditions. These include stub line length, termination, and signaling rate. The A-revision of the standard includes the multidrop option.

Most recent devices support transfer rates in the Gbps-Range (gigabits per second).

2.16.2 Applicability

LVDS targets applications that transfer data point-to-point at very high speeds. It is also capable of driving multiple receivers if the user considers the load configuration. LVDS is particularly suitable for any application that requires low power and/or low EMI. The common-mode input voltage, which is currently limited by the standard to 0 V to 2.4 V, restricts the usage of LVDS with long line lengths (which cause unpredictable ground shifts), as well as the use in electrically noisy environments. With Texas Instruments *wide VICR* devices with a significantly increased input voltage range and integrated hysteresis, the applicability in those environments becomes suitable. In the high-speed range, TI offers repeaters and/or converters for LVDS-PECL/PECL-LVDS translation as well as PECL-CML, LVDS-CML and vice versa. Conversion between LVDS and other levels can be achieved with external circuitry. More detailed information can be found in the application reports *AC-Coupling Between Differential LVPECL, LVDS, HSTL and CML* (SCAA059) and *DC-Coupling Between Differential LVPECL, LVDS, HSTL, and CML* (SCAA062) and in several data sheets (for example, the *SN65LVDS10x 4-Port LVDS and 4-Port TTL-to-LVDS Repeaters* (SLLS396). LVDS is found in clock and data distribution, backplane and cable transmission, level conversion, and many more applications.

2.16.3 Features

- High speed

- Low power consumption
- Low EMI
- ESD protection of 12 kV or 15 kV (HBM) on most devices
- Same pinout as existing RS-422 and RS-485 parts or flow-through pinout

Table 15. TOP LVDS Device List

DEVICE	FUNCTION	POWER	PACKAGE
SN65LVDS33	4-channel Receiver w/ wide common mode and hysteresis	VCC: 3.3 V, I/O: LVTTL/LVDS	16-pin SOIC 16-pin TSSOP
SN65LVDS387/386	16-channel driver/receiver	VCC: 3.3 V, I/O: LVTTL/LVDS	64-pin TSSOP
SN65LVDS100/101 SN65CML100	Single-channel Gbps LVDS/LVPECL/CML repeater/translator	VCC: 3.3 V, I/O: LVDS/LVPECL/CML	8-pin SOIC 8-pin MSOP
SN65LVDS1 SN65LVDT2	Single driver/receiver with integrated termination	VCC: 3.3 V, I/O: LVTTL/LVDS	5-pin SOT-23
SN65LVDS/T122/125 SN65LVCP22/23	LVDS/LVPECL 2x2 (4x4) cross-point switch	VCC: 3.3 V, I/O: LVDS/LVPECL	16-pin SOIC 16-pin TSSOP

2.17 TIA-899 (M-LVDS)

After recognition of the benefits of LVDS, users soon demanded support for the multipoint (multiplex) mode of operation with LVDS-like signals. The technical committees of TIA responded with the development and publication of TIA-899 Multipoint-LVDS or M-LVDS. M-LVDS modifies the electrical specifications of LVDS to accommodate the lower impedance loads, stubs, fail-safe issues, and other problems unique to the multiplex bus structure.

2.17.1 Electrical

The differential output voltage of a standard M-LVDS driver is 480 mV to 650 mV across a 50-Ω test load and, with a 50-mV receiver threshold, provides a minimum of 430 mV of differential noise margin. This margin allows for loaded bus impedance as low as 30 Ω and reflection coefficients of –0.25. The receiver common-mode input voltage can range from –1 V to 3.4 V. TIA-899 specifies two types of receivers. Type-1 receivers have an input threshold near 0 volt whereas the Type-2 receiver threshold is nominally 100 mV as shown in Figure 19. The option of the Type-2 receiver allows idle-line fail safe to be implemented at the cost of noise margin.

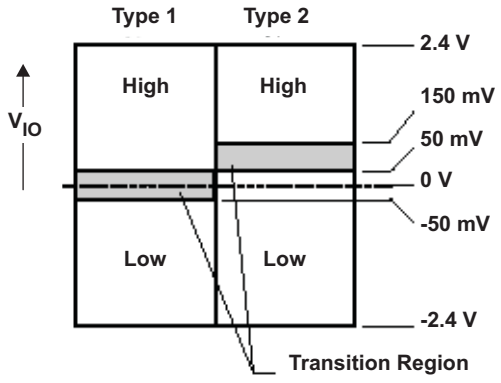


Figure 19. Type 1 / Type 2 Switching Levels

The driver and input characteristics of M-LVDS interfaces are specified such that 32 worst-case loads can be connected to a single bus segment. To allow for the stubs created by these connections, the driver output transition times are limited to be no faster than 1 ns. Additionally, the standard suggests that silicon providers offer different signaling-rate options, so that customers can choose according to their specific requirements (limit EMI, allow for longer stub lines, and so forth).

2.17.2 Applicability

M-LVDS allows multipoint connection of up to 32 nodes and signaling rates to 500 Mbps. These features make M-LVDS applicable to backplane or cabled data transmission where single-ended or RS-485 signaling rates, power consumption, or electromagnetic interference is unacceptable. The common-mode range of M-LVDS likely limits application to cables of 30 meters or less but depends on the environment.

2.17.3 Features

- High speed
- Low power consumption
- Low EMI
- Up to 32 bus connections
- Slew-rate-limited driver outputs
- Type-2 receivers available for idle-line fail safe
- Loaded bus impedances as low as 30 Ω
- Live-insertion compatible

Table 16. Top M-LVDS Device List

DEVICE	FUNCTION	PACKAGE
SN65MLVD200/201	100/200 Mbps, half duplex transceiver without fail safe	8-pin SOIC
SN65MLVD202/203	100/200 Mbps, full duplex transceiver without fail safe	14-pin SOIC
SN65MLVD204/206	100/200 Mbps, half duplex, fail-safe transceiver	8-pin SOIC
SN65MLVD205/207	100/200 Mbps, full duplex, fail-safe transceiver	14-pin SOIC
SN65MLVD080/082	200 Mbps, half duplex transceiver with/without fail safe	64-pin TSSOP

2.18 VMEbus

The VMEbus is an asynchronous bus, which operates in a master/slave architecture. In 1987, the VMEbus specification was originally introduced as IEEE1014, but was altered several times to adjust to newer technologies and to increase the data throughput. New standards became the VME64, VME64x, and finally the VME320 specification. TI was asked by the VITA committee, who governs the VMEbus standards, to develop in an joint effort a bus driver complying with the VME320 specification but still be backward compatible.

Table 17. Maximum Data Transfer Speeds

TOPOLOGY	BUS CYCLE PROTOCOL	MAXIMUM SPEED
VMEbus IEEE1014	BLT	40 Mbyte/s
VME64	MBLT	80 Mbyte/s
VME64x	2eVME	160 Mbyte/s
VME320	2eSST	320 – 500+ Mbyte/s

2.18.1 Electrical

The VMEbus uses push-pull totem pole outputs. For the VME320, it is using LVTTL levels with a ±48-mA output drive. For the implementation of the VME320 bus, a special star interconnection method is required to reach higher speeds.

2.18.2 Application

A VMEbus is often used in a wide variation of application, but the main areas are still industrial application, like factory automation, robotics, or in aerospace, like in fly by wire systems.

2.18.3 Features

- Live insertion capability
- Up to 21 slots in backplane
- Asynchronous data transfer
- Error detection
- Up to 64 address and data bits

Table 18. Top Device List VME

DEVICE	SPECIFICATION	DESCRIPTION	PACKAGE	STATUS
SN74VMEH22501A	LVTTL	8-bit universal bus transceiver and two 1-bit bus transceivers with 3-state outputs up to 1 Gbps	48-pin TSSOP 48-pin TVSOP 56-ball VFBGA	Available

3 Data Links

The data link is responsible for node-to-node validity and integrity of the transmission. Data link devices divide the transmitted bits into frames.

Table 19. Data Links

INTERFACE	DATA THROUGHPUT	DISTANCE	MODE	INPUT CLOCK	SERDES RATIO/ ENCODING	STANDARD	FAMILY
Panelbus (DVI)							
HDMI							
Displayport							
FlatLink™	<1.82 Gbps	<10 m	Simplex	20 MHz to 65 MHz	7:1/None		
General-Purpose Gigabit Transceivers							
Gigabit Ethernet and Fibre Channel							
IEEE 1394 Cable and Backplane Applications (FireWire)						IEEE1394	
Infrared Data Access (IrDA)							
LVDS SerDes and FlatLink™							
PCI/CompactPCI/PCIe							
SONET/SDH Transceivers							
Universal Asynchronous Receiver/Transmitters (UARTs)							
Universal Serial Bus (USB)							

3.1 Digital Video

3.1.1 Panelbus (DVI)

A digital video interface (DVI) connection formats and sends a digital, uncompressed video signal from a transmitter source (PC or Set Top Box, for example) to a receiver (LCD monitor or TV Display). The input to the transmitter is the universal graphics controller interface accepting 24-bit, 3.3-V CMOS single-ended or the Intel™ 81x chipset (DVO) 12-bit dual-edge, 1.1-V to 1.8-V adjustable input interface. The transmitter then encodes and serializes the data using transition minimized differential signaling (TMDS) .The receiver then outputs 24 or 48 bits of data and control signals supporting TFT panels as well as 16-bit or 24-bit DSTN panels.

High-bandwidth digital content protection (HDCP) technologies protect high-value digital motion pictures, television programs, and audio against unauthorized interception and copying between a digital set top box or digital video recorder and a digital TV or PC. HDCP is a specification developed by Intel Corporation to protect digital entertainment across the DVI/HDMI interface.

HDCP-enabled DVI devices first encrypt the data, then use the TMDS high-speed serial link between transmitter and receiver. A HDCP transmitter and HDCP receiver use a set of secret keys whose values are used and exchanged in the encryption algorithms for both transmit and receive. Software controls the encryption and exchange of values from the transmitter to the receiver and vice-versa.

3.1.1.1 Electrical

The DVI interface uses a TMDS link as the primary electrical interconnect between a transmitter and receiver. The TMDS link consists of four differential signal pairs: red channel, green channel, blue channel, and clock. Along with the red, green, and blue data, the following control signals are encoded on the link as well: HSYNC, VSYNC, DE, CTL0, CTL1, CTL2, and CTL3.

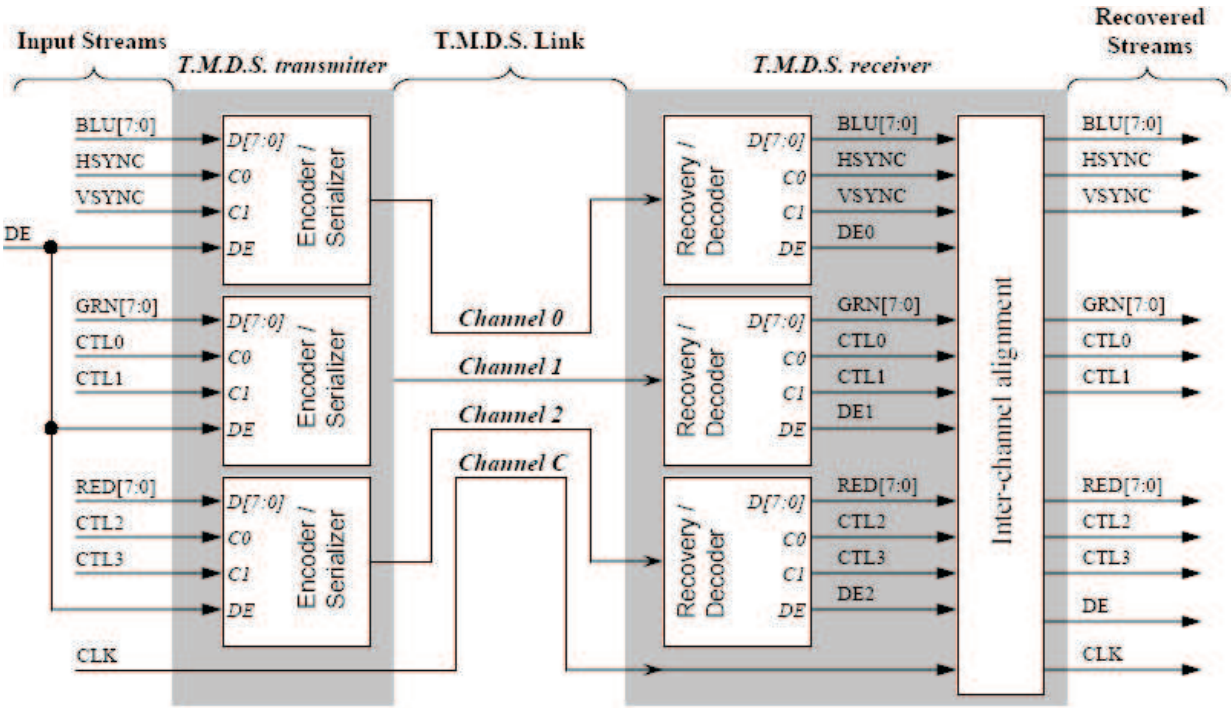


Figure 20. TMDS Link Channel Map

The transition minimization is achieved by implementing an advanced encoding algorithm that converts 8 bits of data into a 10-bit transition minimized, DC-balanced character. For every clock period, 10 bits of data on each channel are transmitted with a maximum clock rate of 165 MHz or data throughput of 1.65 Gbps per channel.

Each differential pair is current driven by the transmitter to develop the low-voltage differential signal at the receiver side of the DC-coupled transmission line. The link reference voltage sets the high level of the differential signal whereas the current source and termination resistance at the receiver sets the low level. The termination resistance and characteristic impedance of the cable must be matched (50 Ω, single-ended).

3.1.1.2 Protocol

DVI

DVI standards support the standard VESA video timings displays up to UXGA resolution and standard TV resolutions up to 1080 pixels. It is not required, however, to provide timings to the transmitter that meet all of the standard timing parameters. The data and timing of the signals input to the device are transmitted as is and output from the receiver with no changes. This allows custom timing, reduced blanking, or other various timing options to be used if needed for a given display.

HDCP

In additional to the DVI protocol, the HDCP authentication protocol is an exchange between the HDCP transmitter and an HDCP receiver that affirms to the transmitter that the HDCP receiver is authorized to receive HDCP content. Each HDCP device is provided with a unique set of secret device keys from the digital content protection LLC.

The HDCP authentication protocol has two steps. The first step establishes shared values between the two HDCP devices if both devices have a valid device key set from the digital content protection LLC. The second step occurs during the vertical blanking interval preceding each frame in which encryption is enabled and provides an initialization state for the HDCP cipher for encrypting the HDCP content within that frame.

3.1.1.3 Applicability

DVI and HDCP devices are widely used in both PC and consumer applications. DVI/HDCP transmitters are common on add-in graphics cards, set top boxes, or any digital video source. Receivers are common in TVs, desktop displays, and projectors. HDCP devices are most commonly used in set top boxes and TV or projector applications. Typically, DVI/HDCP devices operating at maximum throughput can be supported with cables up to 5 meters long. For this reason, most DVI/HDCP applications have the transmitter and receiver in relatively near proximity.

3.1.1.4 Features

- 1.65-Gbps maximum data throughput per each TMDS channel
- Uncompressed video removes any risk of compression artifacts or loss of color depth
- Transition-minimized, DC-balanced data for EMI reduction
- Single link supports 165 Mpixels/s, supports up to UXGA, or 1080-pixel resolutions
- Image quality better than analog (No D/A–A/D conversions) and has high skew/jitter tolerance
- Pin-to-pin-compatible devices for easy upgrade from non-HDCP to HDCP

Table 20. DVI Transmitter Device List

DEVICE	HDCP SUPPORT	SPEED (MHz)	POWER (V)	PACKAGE
TFP410	No	165	3.3	64-pin TQFP
TFP510	Yes	165	3.3	64-pin TQFP
TFP513	Yes	165	3.3	64-pin TQFP

Table 21. DVI Receiver Device List

DEVICE	HDCP SUPPORT	SPEED (MHz)	POWER (V)	PACKAGE
TFP101/A	No	86	3.3	100-pin TQFP
TFP201/A	No	112	3.3	100-pin TQFP
TFP401/A	No	165	3.3	100-pin TQFP
TFP403	No	165	3.3	100-pin TQFP
TFP501	Yes	165	3.3	100-pin TQFP
TFP503	Yes	165	3.3	100-pin TQFP

3.1.2 DisplayPort

DisplayPort is a Video Electronic Standard Association (VESA)-supported open standard currently at revision 1.1a. DisplayPort was developed to replace LVDS, VGA, and digital video interface (DVI) in the computing market space by several PC OEMs and graphic processor semiconductor companies. DisplayPort offers several advantages over these technologies with greater throughput, link quality management, and EMI benefits, see Table 22.

Table 22. EMI and Link Quality

FEATURE	VALUE
Scrambling/de-scrambling	16-bit LFSR
8B/10B	Yes
Embedded clock	Yes
Interllane skewing	2 UI per adjacent lane
Down spreading SSC	30 kHz–33 kHz
Link training	Yes
Monitoring	Yes
Link Quality Management	Yes

As LCD display panel resolution, color width depth, and refresh rates grow FlatLink requires more data channels and higher clock rates. VGA lacks scalability for the higher resolution monitors and is unable to provide content protection. DVI is a frozen standard at 1.0 and does not support the move to these higher resolution monitors. High definition multimedia interface (HDMI) is a standard that DisplayPort will coexist with as it is entrenched in the consumer market.

DisplayPort target applications are for the internal GPU-to-display panel link and for PC/notebook-to-monitor link. Display port is also anticipated to take over the internal TV link from the graphics chip to the panel. DisplayPort was defined in a manner that provides some backward-compatibility with DVI and HDMI, defined as dual mode DisplayPort (DP++). DP++ enabled transmitters and receivers can send and receive DisplayPort or HDMI/DVI formatted data using a DisplayPort electrical layer.

3.1.2.1 Electrical

DisplayPort has two differential signals, Main Link and Auxiliary, and a Hot Plug Detect (HPD) line. Both differential signals are ac-coupled, using a 75-nF to 200-nF capacitor. Table 23 provides the basic electrical layer parameters for the main link, auxiliary, and hot plug detect lines. Figure 21 and Table 24 demonstrate how the VTX-DIFFp-p and Pre-Emphasis parameters work together to optimize the link quality.

Table 23. DisplayPort Electrical Layer

PARAMETER	VALUE
HPD	
Voltage	2.25 V – 3.6 V
Detect threshold	2 V minimum
Unplug threshold	0.8 V maximum
IRQ pulse width Dr by sink	0.5 ms – 1 ms
IRQ pulse detect threshold	2 ms minimum
MAIN LINK	
Main link data rate per lane (Gbps)	1.62, 2.7
AC coupled	75 nF – 200 nF
TRANSMITTER	
$V_{TX-DIFFp-p}$	400 mV ±12 mV 600 mV ±8 mV 800 mV ±12 mV 1.2 V ±8 mV
Pre-Emphasis/De-Emphasis (dB)	0 dB 3 dB - 5 dB ±20% 6 dB ±20% 9.5 dB ±20%
$V_{TX-DC-CM}$ output DC common mode	0 V – 2 V
RECEIVER	
$V_{RX-DIFFp-p}$ (minimum for 2.7 Gbps)	120 mV
$V_{RX-DIFFp-p}$ (minimum for 1.62 Gbps)	40 mV

Table 23. DisplayPort Electrical Layer (continued)

PARAMETER	VALUE
$V_{RX-DC-CM}$ input DC common mode	0 V – 2 V
AUXILIARY LINK	
Data rate	1 Mbps
$V_{AUX-DIFFp-p}$ transmit (minimum – maximum)	0.39 V – 1.38 V
$V_{AUX-DIFFp-p}$ receive (minimum – maximum)	0.32 V – 1.36 V
$V_{AUX-DC-CM}$ DC common mode	0 V – 2 V

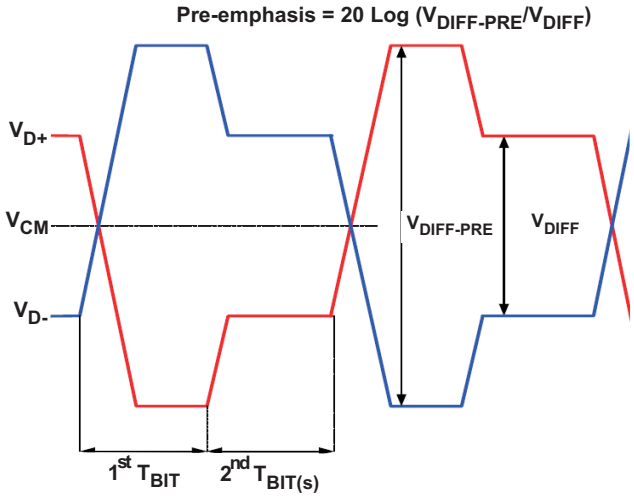


Figure 21. DisplayPort Output Wave Shaping

Table 24. DisplayPort Pre-Emphasis Levels (dB)

$V_{TX-DIFFp-p}$	VOD(pp)_PRE (V)			
	0 (1X)	3.5 (1.5X)	6 (2X)	9.5 (3X)
0.4	0.4	0.6	0.8	1.2
0.6	0.6	0.9	1.2	NA
0.8	0.8	1.2	NA	NA
1.2	1.2	NA	NA	NA

3.1.2.2 Protocol

DisplayPort has a defined protocol based on several standards and DisplayPort-specific requirements. Unlike HDMI and DVI, DisplayPort transmits audio/video as packetized data. The following is a list of Standards that are used by DisplayPort:

- Extended Display Identification Data (EDID)
- Display Data Channel and Command Interface (DDC/CI)
- Monitor Command and Control Set (MCCS)
- Supports equivalent functionality to various feature sets defined by CEA-861-C and CES-931-B
- Timing standard is based on VESA DMT and CVT as well as timing nodes listed in CEA-861-C
- Auxiliary channel is Manchester II coded.
- Audio supports 8 channels of Linear Pulse Code Modulation (LPCM)
- Support Colorimetry based on VESA and CEA for RGB and YCbCr based on at least 24 bpp YCbCr 4:4:4 and 16 bpp YCbCr 4:2:2 in both 601 (defined in ITU-R BT.601-5 section 3.5 or EIA/CEA-770.2-C section 3.3) and 709 (defined by ITUR BT.709-4 Part 1, Section 4 or EIA/CEA-770.3-C sections 5.4 to

5.7).

3.1.2.3 Applicability

DisplayPort targets applications where LVDS, DVI, and VGA are currently being used. LVDS is the internal link from a GPU to a timing control (TCON) for a notebook, monitor, or TV panel. As the GPU provides all scaling it is possible to develop a direct drive monitor using a DisplayPort link that simplifies the monitor design by removing the scaler required by the other display technologies. For external box-to-box type of applications, various types of circuits may be needed for switching, re-driving, and translating. Figure 22 shows various applications of these types.

DisplayPort will also be seen in the consumer space starting in 2009. The first application will be the internal link from the scaler/MCM chip set to the panel for HDTVs. With DP++ capability, it will not be long before the front-end connection will include DisplayPort followed by the set top box and mobile applications.

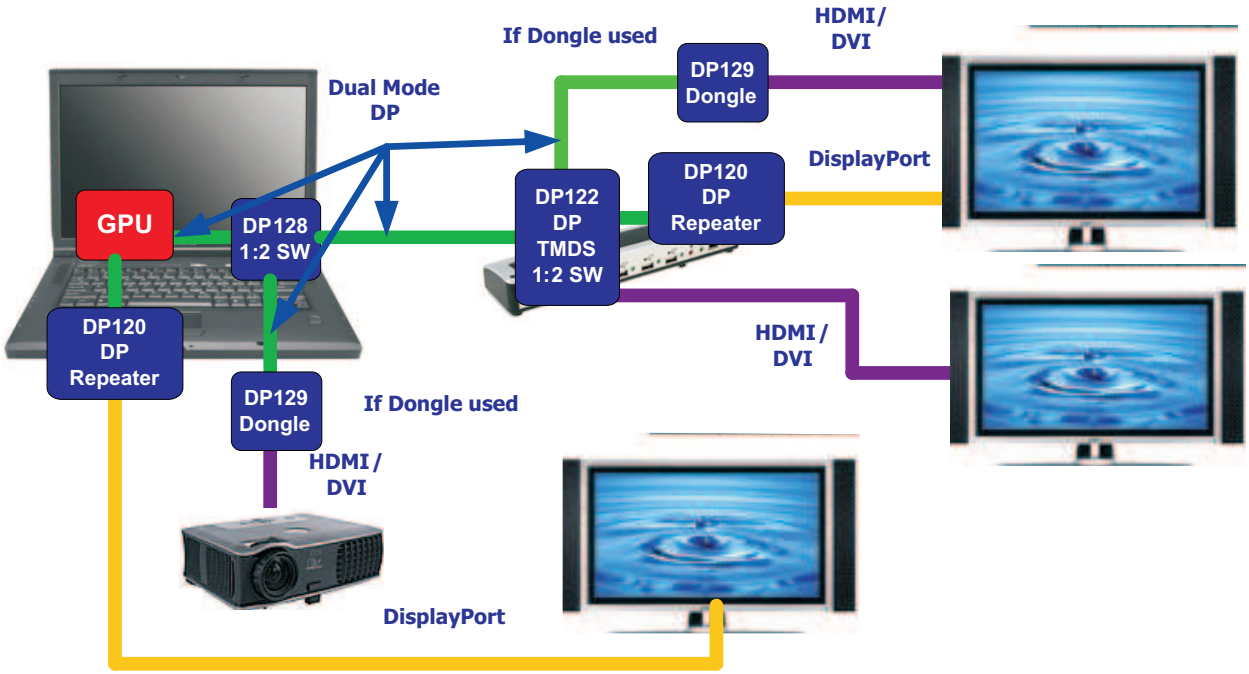


Figure 22. Typical DisplayPort Application

3.1.2.4 Features

- Integrated TMDS level translator
- Enhanced ESD:
- 10-kV to 12-kV HBM ESD on DisplayPort and TMDS pins
- 8 kV on all auxiliary and I^2C pins
- Receiver equalization
- Enhanced commercial temperature range: 0°C to 85°C
- DP port supports data rates up to 2.7 Gbps
- DP port supports dual-mode DisplayPort
- DP port output waveform mimics input waveform characteristics
- TMDS port supports data rates up to 2.5 Gbps
- Integrated I^2C logic block for DVI/HDMI connector recognition

Table 25. DisplayPort Products

DEVICE	FUNCTION	POWER	PACKAGE
SN75DP118	1:1 DP++ Buffer	V_{CC} : 5 V	36-pin QFN
SN75DP122	1:2 where channel A supports DP++ and channel B is a TMDS level translator for DVI/HDMI. Contains the HDMI/DVI connector recognition capability	V_{CC}: 3.3 V_{DD}: 5V	56-pin QFN
SN75DP128	1:2 where both channels support DP++	V_{DD}: 5V	56-pin QFN
SN75DP129	1:1 DP++ to TMDS level translator for DVI/HDMI. Contains the HDMI/DVI connector recognition capability	V_{CC}: 3.3V	36-pin QFN

3.1.3 LVDS SerDes, FlatLink™, and FlatLink™ 3G

The terms LVDS SerDes, FlatLink™, and FlatLink™ 3G each describe a device family based on LVDS serialization technology. The devices interconnect two parallel bus systems physically through serialization techniques using a high-speed serial data path. The following explanations apply equally to all three product families; differences are mentioned in the text accordingly.

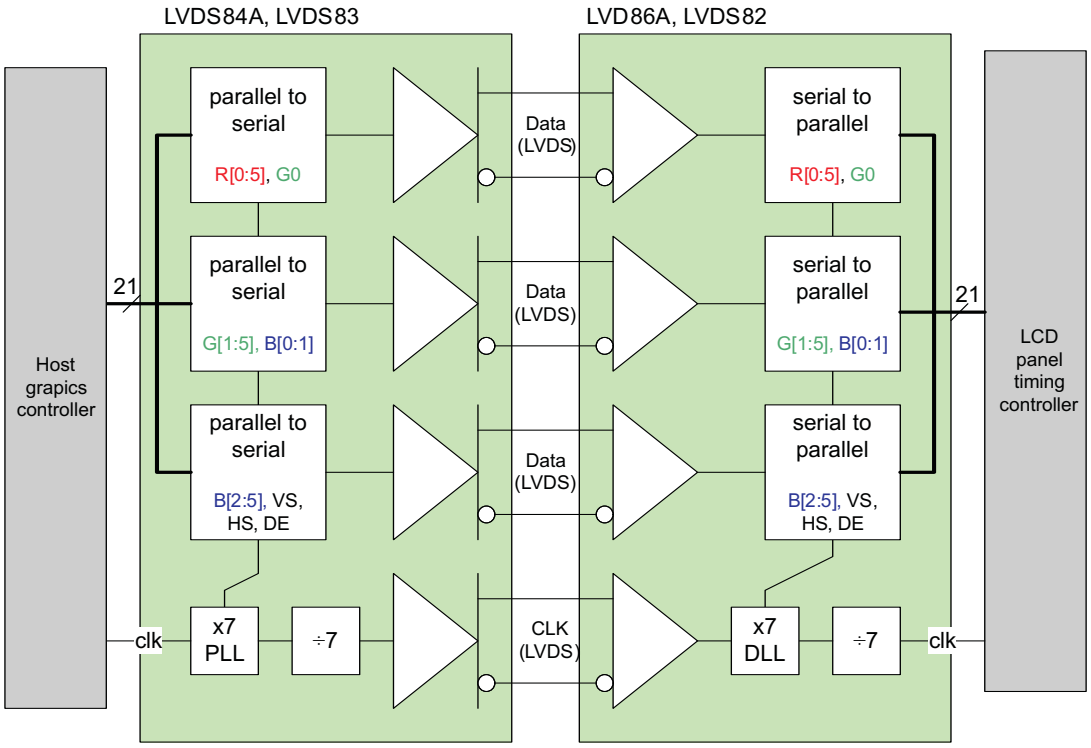


Figure 23. Typical FlatLink™ Application

Principle of a SerDes (Serializer/Deserializer) Device: A serializer device is a transmit device reducing the number of parallel input signals into fewer output signals; the signal count reduction from input to output results into a higher transfer speed on the output. A deserializer is a receiver device converting the serial inputs back to parallel. The output of the receiver is identical to the input signal to the transmitter concerning data rate and number of output signals. The serializer/deserializer pair is transparent to the link. The range for the bus clock rate is limited by the bandwidth of the on-chip PLL.

The transmitter has a certain number of LVTTL-compatible data input pins (parallel bus) and a clock input. The input pins can be divided into groups. All of the data signals in one group become serialized into a higher frequent data stream. The compression ratio can be, for example, 7:1, 10:1, 15:1, or 30:1, depending on the device. The process can be visualized as a multiplexer switching between all signals of a group running on a frequency equal to the clock multiplied by the number of signals to be transmitted. Each serial data stream is transmitted through a differential pair of lines based on LVDS (for example, FlatLink) or subLVDS (for example, FlatLink3G). The original clock signal is either transferred over an additional pair of lines or is embedded in the serial data stream and can be recovered on the receiver part (see Section 3.1.3.2).

On the receiving side, the high-frequency differential data stream is demultiplexed and clocked out to the parallel LVTTL output bus.

Table 26. Multiplexing Ratios for LVDS SerDes and FlatLink™ Devices

FUNCTION	PRODUCT FAMILY	INPUT (LVTTL)	OUTPUT (LVDS)
Transmitter	LVDS SerDes	10 data lines + clock line	1 line with embedded clock
	FlatLink	21 data lines + clock line	3 data lines + clock line
		28 data lines + clock line	4 data lines + clock line
	FlatLink3G	28 data lines + clock line	1, 2, or 3 data lines + clock line
Receiver	LVDS SerDes	1 line with embedded clock	10 lines + clock line
	FlatLink	3 data lines + clock line	21 lines + clock line
		4 data lines + clock line	28 lines + clock line
	FlatLink3G	1, 2, or 3 lines + clock line	28 lines + clock line

3.1.3.1 Electrical

The parallel I/O bus is based on LVTTL. LVDS signaling is used for the high-speed serial transmission lines of LVDS SerDes and FlatLink; LVDS meets or exceeds the ANSI EIA/TIA-644 Standard. The devices require a single 3.3-V power supply. The FlatLink3G serial lines use subLVDS signaling level, allowing for a 1.8-V core power supply and lower power.

3.1.3.2 Protocol

FlatLink™3G devices are optimized for true-color video data transmission, targeting small display panels from QVGA resolution up to XGA. FlatLink™ devices are optimized for video data transmission for medium-size display panels from VGA resolution up to HD.

No specific protocol requirements for using 10-bit LVDS SerDes devices exist. The transmitter generates a start and a stop bit for every 10 data bits. This start/stop bits ensure that the receiver detects the proper byte boundary and the two bits provide sufficient transition density for the clock recovery circuit.

3.1.3.3 Applicability

FlatLink™: is designed to transfer a continuous RGB video data stream from the GPU, scaler, or framer to the graphic LCD display in applications ranging from notebook to monitor and TV. The major advantages compared with realizing this transfer based on standard bus logic are in the reduced number of parallel data lines and lower electromagnetic emission.

FlatLink™3G: is designed to transfer a continuous RGB video data stream from the application processor to a LCD display in mobile applications such as flip phones or digital camcorders. The major advantages compared with standard FlatLink are a further reduction of the number of parallel data lines, reduced power consumption, and extremely low electromagnetic emission. This allows for more attractive swivel designs in mobile products. Low EMI reduces the interference between the phone antenna and display circuit. FlatLink™3G integrates the 100-Ω line end termination.

LVDS SerDes: The differential transmission mode provides high robustness against in-coupling noise. Therefore, LVDS SerDes devices are perfectly suited for point–to–point interconnections between two parallel buses in telecommunication backplanes or industrial applications, for example.

Bus Speed: The clock frequency of the parallel bus is limited to the PLL locking range of the transmitter and receiver PLL. TI products support the following frequency ranges:

- FlatLink™3G: 4 MHz to 65 MHz
- FlatLink™: 10 MHz to 100 MHz
- 10-bit LVDS SerDes: 10 MHz to 66 MHz

Bus Topology: SerDes can be used as point-to-point or multidrop connection.

Initialization After Reset/Power Down: As typical in all PLL-based applications, the receiver requires a certain time to lock to the clock signal. For LVDS SerDes and FlatLink, the result on the receiver output becomes valid after approximately 1 ms. FlatLink3G disables the transmitter and receiver output during startup for increased robustness.

3.1.3.4 Features

- Data throughput up to 700 Mbps over one differential pair
- Industrial temperature specification (–40°C to 85°C) for LVDS SerDes and FlatLink3G
- Low power consumption and low emission (portable devices)
- Using a daisy chain layout offers multidrop architecture ability
- Low power consumption when disabled (below 10 μW for FlatLink3G)

Table 27. LVDS SerDes Device List

DEVICE	SERDES RATIO	THROUGHPUT	VCC AND I/O	PACKAGE
LVDS SerDes				
SN65LV1021 SN65LV1023A/1224B	10:1	100–400 Mbps 100–660 Mbps	VDD: 3.3 V Parallel I/O: LVTTL Serial I/O: LVDS	28-pin SSOP
SN65LVDS95/96 SN65LVDS93/94	21:3 28:4	0.420–1.365 Gbps 0.560–1.820 Gbps		48-pin TSSOP 56-pin TSSOP
FlatLink™				
SN75LVDS84A/86A SN75LVDS83/82 LVDT1422 SN75LVDS83B	21:3 28:4 14:2 bi-directional 28:4	0.671–1.428 Gbps 0.868–1.904 Gbps 0.14–1.4Gbps 0.14–1.4Gbps	VDD: 3.3V Parallel I/O: LVTTL Serial I/O: LVDS	48-pin TSSOP 56-pin TSSOP 64-pin TSSOP 4,5 x 7 mm μBGA and 56-pin TSSOP
FlatLink™3G				
SN65LVDS301, 303, 306 SN65LVDS307 SN65LVDS302, 304, 306 SN65LVDS308 SN65LVDS310	27:1-3 (TX) 27:1-2 (TX) (1-3):27 (RX) 2:27 (RX) 1:27 (RX)	0.1–1.755 Gbps	VDD: 1.8V Parallel I/O: LVTTL Serial I/O: subLVDS	5×5 mm μBGA 4×4 mm μBGA

3.1.4 HDMI™

The High-Definition Multimedia Interface (HDMI) is provided for transmitting digital Video and audio signals from DVD players, set top boxes, and other audiovisual sources to television sets, projectors, and other displays. HDMI uses transition minimized differential signaling (TMDSTM) to transfer audiovisual data from HDMI source to HDMI sink.

Content protection technology is available. HDMI can also carry control and status information in both directions.

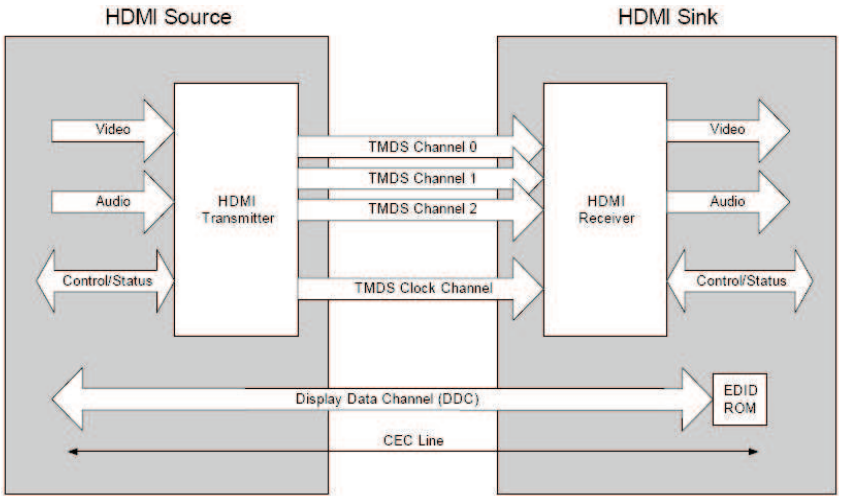


Figure 24. HDMI Block Diagram

Audio, video, and auxiliary data is transmitted across the three TMDS data channels. A TMDS clock is transmitted on the TMDS clock channel and is used by the receiver as a frequency reference for data recovery on the three TMDS data channels. The clock frequency is the pixel clock for 8-bit-per-color signals and a multiple for 10 (1.25x)-, 12 (1.5x)-, and 16 (2x)-bit-per-color content. At the source, TMDS encoding converts the 8 bits per TMDS data channel into the 10-bit, DC-balanced, transition minimized sequence which is then transmitted serially across the differential signal pair at a rate of 10 bits per TMDS clock period.

Video data can have a pixel size of 24, 30, 36, or 48 bits. Video formats with TMDS rates below 25 MHz (for example, 13.5 MHz for 480i/NTSC) can be transmitted using a pixel-repetition scheme. The video pixels can be encoded in either RGB, YCBCR 4:4:4, or YCBCR 4:2:2 formats. In order to transmit audio and auxiliary data across the TMDS channels, HDMI uses a packet structure. To attain the higher reliability required of audio and control data, this data is protected with a BCH error correction code and is encoded using a special error reduction coding to produce the 10-bit word that is transmitted. HDMI1.3A supports the following audio formats:

- A single IEC 60958 L-PCM audio stream at sample rates of 32 kHz, 44.1 kHz, or 48 kHz. This can accommodate any normal stereo stream.
- Audio at sample rates up to 192 kHz and with 3-to-8 audio channels
- IEC 61937 compressed (for example, surround sound) audio stream at bit rates up to 24.576 Mbps.
- 2 to 8 channels of one bit audio and a compressed form of one bit audio called DST.

The DDC channel is used by the source to read the Sink's Enhanced Extended Display Identification Data (E-EDID) in order to discover the sink's configuration and/or capabilities. DDC channel is also used to exchange audiovisual content protection HDCP keys.

3.1.4.1 Electrical

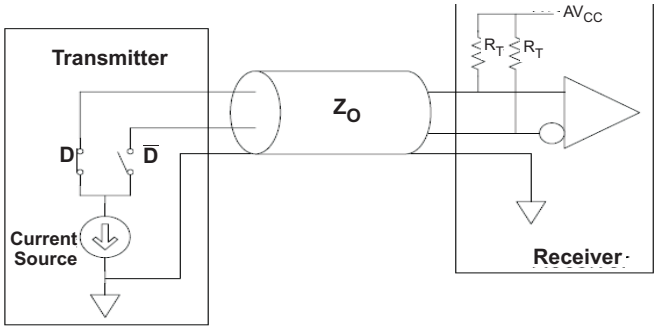


Figure 25. TMDS Electrical Schematic

- TMDS technology uses current drive to develop the low-voltage differential signal at the sink side of the DC-coupled transmission line.
- The link reference voltage sets the high-voltage level of the differential signal, whereas the low-voltage level is determined by the current source of the HDMI source and the termination resistance at the sink.
- The termination resistance and the characteristic impedance of the cable are matched at 100 Ω.
- TMDS data rate (Tbit) is 10X TMDS clock rate (Tpixel)
- HDMI sink minimum differential sensitivity: 150 mV
- HDMI sink maximum differential input: 1560 mV
- Fast rise and fall times on TMDS channel: 100 to 150 ps (typical)
- Eye closure at the receiver side up to 0.50 UI; eye closure at the transmitter side <0.30 UI
- Intrapair skew at the transmitter side: 0.15 × Tbit, Interpair skew at the transmitter side: 0.20 × Tpixel

3.1.4.2 Protocol

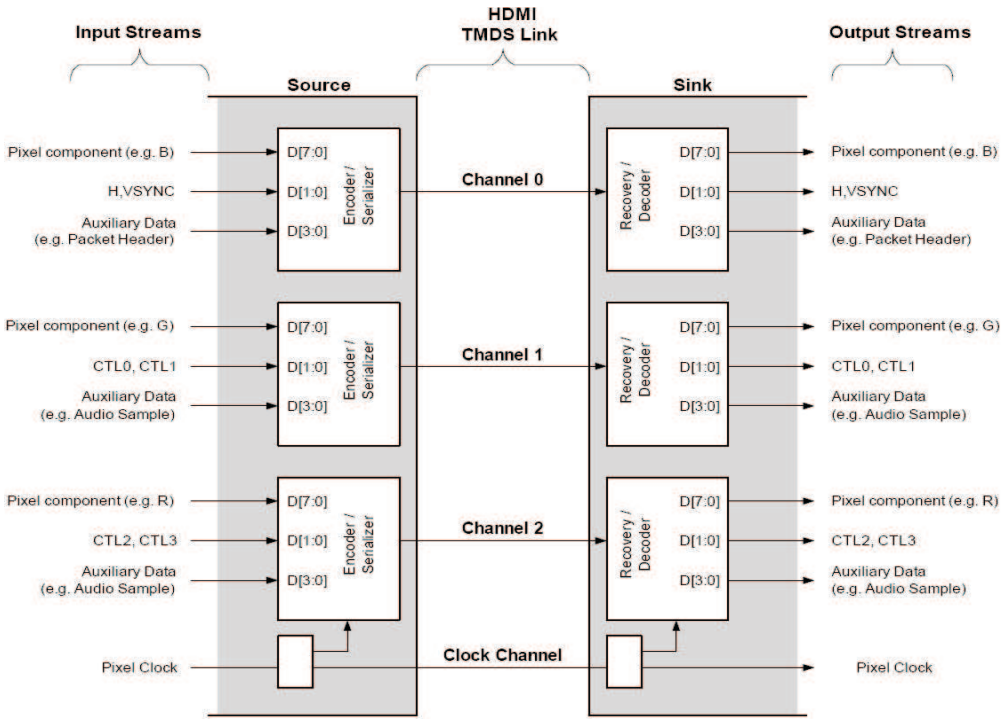


Figure 26. HDMI/TMDS Link Block Diagram

The HDMI link includes three TMDS data channels and one single TMDS clock channel.

The TMDS clock channel constantly runs at a rate proportional to the pixel rate of the transmitted video. During every cycle of the TMDS clock channel, each of the three TMDS data channels transmits a 10-bit character. This 10-bit word is encoded using one of several different coding techniques. The input stream to the source's encoding logic contain video pixel, packet, and control data. The packet data consists of audio and auxiliary data and associated error correction codes. These data items are processed in a variety of ways and are presented to the TMDS encoder as either 2 bits of control data, 4 bits of packet data, or 8 bits of video data per TMDS channel. The source encodes one of these data types or encodes a guard band character on any given clock cycle.

The HDMI link operates in one of three modes: Video Data Period, Data Island Period, and Control Period. During the Video Data Period, the active pixels of an active video line are transmitted. During the Data Island Period, audio and auxiliary data are transmitted using a series of packets. The Control Period is used when no video, audio, or auxiliary data needs to be transmitted. A Control Period is required between any two periods that are not Control Periods. Video Data Periods use transition minimized coding to encode 8 bits per channel, or 24 bits total per pixel. Data Island Periods are encoded using a similar transition minimized coding, TMDS Error Reduction Coding (TERC4), which transmits 4 bits per channel, or 12 bits total per TMDS clock period. During Control Periods, 2 bits per channel, or 6 bits total are encoded per TMDS clock using a transition maximized encoding.

3.1.4.3 Applicability

HDMI connects digital audio/video sources such as set top boxes, Blu-ray Disc players, personal computers, video game consoles, and AV receivers to compatible digital audio devices, video monitors, and digital televisions (DTV).

In addition to the HDMI transmitter and HDMI receiver, the market demands HDMI switches. The TMDS351 is a 3-port digital video interface (DVI) or high-definition multimedia interface (HDMI) switch that allows up to three DVI or HDMI ports to be switched to a single display terminal. TMDS351 also provides receiver equalization to accommodate to different input cable lengths.

3.1.4.4 Features

- Uncompressed audiovisual data from source to sink
- TMDS data rate up to 2.5 Gbps
- Content protection supported
- Single HDMI cable carries both audio and video data.
- Selectable fixed receiver equalization
- ESD: 8-kV HBM

The next generation of TI HDMI switches will include the following features:

- Adaptive receiver equalization to support up to a 230-m cable
- ESD: 10-kV HBM
- Clock activity detect to enable outputs only when a valid clock is present
- TMDS data rate up to 3.04 Gbps
- Integrated DDC repeater

Table 28. HDMI Switch Device List

DEVICE	MUX	HDMI SPECIFICATION	PACKAGE	DDC REPEATER
TMDS351	3 to 1	HDMI specification 1.3a (48-bit)	64TQFP	No
TMDS251	2 to 1	HDMI specification 1.3a (48-Bit)	64TQFP	No
TMDS341	3 to 1	HDMI specification 1.3a (36-bit)	80TQFP	No
TMDS141	1 to 1	HDMI specification 1.3a (36-bit)	40QFN	Yes
TMDS442	4 to 2	HDMI specification 1.3a (36-bit)	128TQFP	Yes

Table 29. Next Generation HDMI Switch Device List

DEVICE	MUX	HDMI SPEC	PACKAGE	DDC REPEATER	AVAILABLE
TMDS461A	4 to 1	HDMI spec 1.3a (48-bit)	100TQFP	Yes	July 2009
TMDS361A	2 to 1	HDMI spec 1.3a (48-Bit)	64TQFP	Yes	May 2009
TMDS261A	3 to 1	HDMI spec 1.3a (48-bit)	64TQFP	Yes	May 2009

3.2 General-Purpose Gigabit Transceivers

General-purpose gigabit transceivers devices has been made to bridge large number of data bits over one differential pair. The input to the transceiver is a parallel 16- or 18-bit wide bus system. These input bus signals are serialized and sent over a differential link to the second transceiver deserializing the serial pattern and clocking it out on parallel interface again. Input and output bus appears identical to the user.

General-purpose gigabit transceiver products address primary point-to-point, high-speed, data transfer applications.

3.2.1 Electrical

The parallel interface of TI's 16:1 general-purpose gigabit devices consists of 16 transmit data lines latched on the rising edge of a corresponding clock signal and two control signals enabling sending special characters. The receive path is designed in similar manner: 16 data bits and clock plus two status bits (Figure 27).

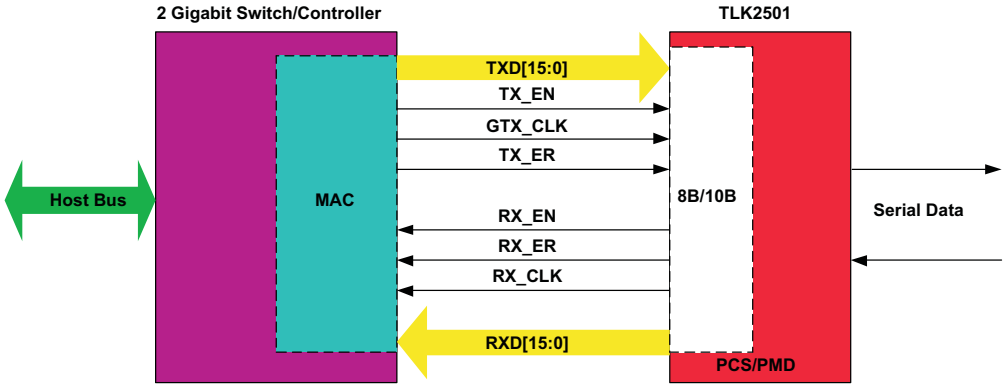


Figure 27. SerDes Parallel Interface

The 18:1 general-purpose gigabit transceiver accepts 18 bits of data with the clock signal on its parallel transmit interface. On the receiving path, 18 bits with recovered clock are present.

Parallel I/O: 3.3-V tolerant LVTTL input, 2.5-V LVTTL output.

Serial link: Historically, three driver topologies are generally used for data transmission at gigabit speeds: (LV)PECL (Low Voltage Positive Emitter Coupled Logic), CML (Current Mode Logic), and VML (Voltage Mode Logic).

A (LV)PECL driver sources VOH onto a load. Thus, it provides strong rising edge, but relies on a pulldown resistor for the falling edge.

A CML driver sinks a fixed current into a load – Ohm's law then tells signals swing. CML relies on a pullup resistor for rising edge.

VML drives certain V_{OL} and V_{OH} onto a load, instead. Loads impedance then determines current flow. VML sources both, rising and falling edge of the signal.

TI's CML and VML drivers provide a typical differential swing of 850 mV (LVPECL compatible). Receiver's input sensitivity is down to 200 mV.

The following steps are performed on the transmitter side of a 16-bit, general-purpose gigabit transceiver:

1. The incoming bus signal is buffered in reference to the input clock signal.
2. 8B10B encoding of the data word (this ensures sufficient transition rate of equal/above 3 or more transitions on 10-bit data for clock recovery purposes as well as DC balance of serial data stream allowing AC coupling)
3. Serialization of the data
4. Clock the serial data into the differential line using the CML/VML driver

The receiver side performs the reverse operations in reverse order to regenerate to original sent word.

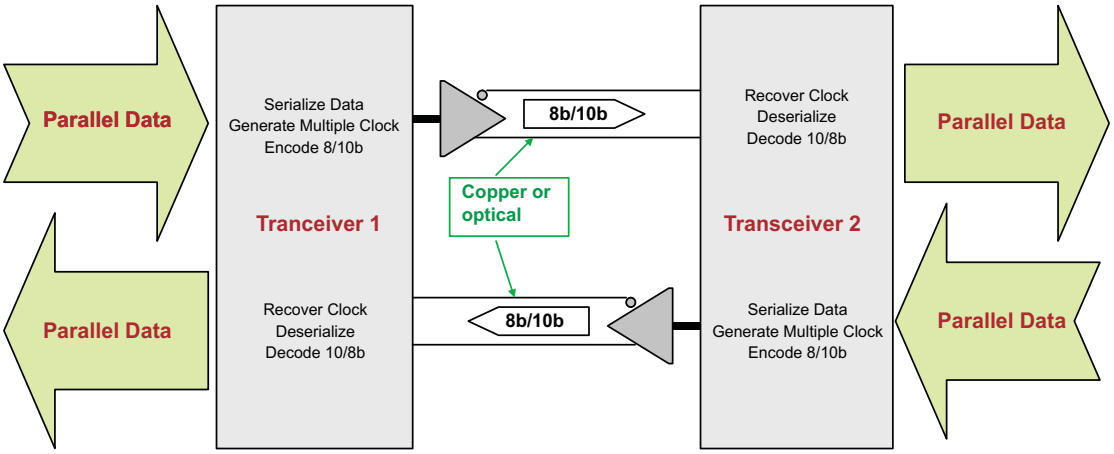


Figure 28. SerDes Interface Using Two Transceivers

The transmission media of the serial path can be PCB, copper cable, or fiber-optics using an optical module in-between. The impedance of the copper must be matched to 50 (75) Ω. The maximum distance to be bridged depends on the transmission speed and the transmission media; tests showed proper functionality at 2.5 Gbps over up to 10 m of xTP Cat5 cable.

3.2.2 Protocol

No special protocol is necessary for usage of TI's general-purpose gigabit transceivers.

Using special carrier words and an initialization algorithm, the on-chip state machine of a 16-bit transceiver allows correct data transfer after reset or data loss. It also guarantees boundary of the parallel output data word out of incoming serial bit stream. Status outputs on the receiver inform the user about the actual transmission state, as it can be normal data transfer, transmission error, idle, or carrier extension.

No specific protocol is required for using 18-bit, general-purpose SerDes devices. However, the transmitter adds a start and a stop bit between each 18 bits sent over serial link. These start/stop bits ensure correct byte boundary on the parallel receiver bus and sufficient transition density for the clock recovery circuit.

3.2.3 Applicability

The differential transmission mode provides high robustness against noise. Therefore, SerDes devices perfectly suit networking, telecommunication, or data-communication designs.

Bus speed: The clock rate of those bus systems can be chosen within a certain range. The limiting factor on minimum and maximum clock speed is the bandwidth of the fully integrated PLL (for example, 80 MHz to 125 MHz).

Bus Topology: General-purpose gigabit SerDes can be used for point-to-point connections.

Initialization after reset/power down: As typical in all PLL-based applications, the receiver requires a certain time to lock onto the incoming serial signal. During this time, the receiver output and control pins are held in a high–impedance state that can take one millisecond.

Adjustable voltage swing: The serial output driver offers adjustable voltage swing that can be used for optimizing a particular transmission line impedance and length, as well as for controlling the output swing for EMI and attenuation concerns.

3.2.4 Features

- Data throughput up to 2.5 Gbps over one differential pair
- Very low power consumption, low emission
- External pins signalize data errors/loss of signal on receiving side
- Integrated clock recovery
- Full duplex data transmission
- Serial link and device test using built-in random bit generator/verification function

Table 30. Serial Gigabit Device List

DEVICE	SERDES RATIO	SERIAL SPEED (DATA THROUGHPUT)	VCC AND I/O	PACKAGE
TLK1501	16:1	0.6–1.5 Gbps (0.48–1.2)	V_{DD}: 2.5 V Parallel input 3.3 V tolerant Serial I/O: CML	64-pin VQFP
TLK2501	16:1	1.6–2.5 Gbps (1.28–2.0)		
TLK2521	18:1	1.5–2.5 Gbps (1.35–2.25)		
TLK3101	16:1	2.5–3.125 Gbps (2.0–2.5)	V_{DD}: 2.5 V Parallel input 3.3 V tolerant Serial I/O: VML	

3.3 Gigabit Ethernet and Fibre Channel Transceivers

Gigabit Ethernet standards have primarily been developed to provide connectivity among quickly increasing computer networks, for example, within companies or organizations. Nowadays, it is also widely used for any kind of data communication over glass fiber, copper cables, and backplanes.

Fibre Channel is a channel/network standard containing protocol, connectivity, and distance guidelines for high-performance storage networks and server interconnects.

3.3.1 Electrical

IEEE802.3z Gigabit Ethernet standard specifies the physical and the data link layer (in reference to the Open Systems Interconnection reference model) for a serializer/deserializer device running at 1.25 Gbps on a serial link. The parallel interface is a Ten Bit Interface (TBI) with 10-bits of LVTTL data aligned to the rising edge of the clock in each direction. Nowadays, however, devices with Reduced Ten Bit Interface (RTBI) – a 5-bit Double Data Rate (DDR) interface are also available. The parallel data is already 8B/10B encoded. The serial link is based on LVPECL signaling.

The electrical part of ANSI X3T11 Fibre Channel specification defines using the TBI interface on a parallel bus and the LVPECL on a serial link as well.

The IEEE802.3ae 10 Gigabit Ethernet standard describes, among other things, the 10 Gigabit Media Independent Interface (XGMII) as a parallel bus as well as the 10 Gigabit Attachment Unit interface (XAUI) as a serial interface. XGMII interface consists of:

- 32 data bits of 1.5-V High-Speed Transceiver Logic (HSTL) Class 1 signals (former drafts of the specification prescribed using 1.8-V HSTL) in each direction
- 4 LVTTL control bits indicating that the Reconciliation Sub-layer is presenting either valid data or control characters
- Corresponding clock signal for sampling and driving both, data and control signals, in Double Data Rate mode (signals valid on rising and falling edge of clock)

XAUI interface includes four AC-coupled differential pairs. The nominal baud rate is 3.125 Gbps with maximum differential voltage of 1.6 V peak-to-peak.

3.3.2 Protocol

Gigabit Ethernet, 10 Gigabit Ethernet, and Fibre Channel standards prescribe using specific protocols for controlled data transmission. Detailed description of these standards is beyond the scope of this application report.

It is unnecessary, however, to provide full specification-compliant data to the transceiver device (PHY) to ensure its functionality. It is important to know, that Gigabit Ethernet and Fibre Channel transceivers expect 8B/10B encoded data on their parallel interfaces (10-gigabit devices can provide on-chip encoding/decoding function) and that they use a special pattern – K28.5 for word-alignment purposes on the receiver's parallel bus.

Many devices such as TLK1201A, TLK3134, and TLK2218 also support wireless infrastructure signaling standards as such and Common Radio Platform Interface (CPRI) and Open Base Station Architecture Initiative (OBSAI). These standards are built on Ethernet and 10G Ethernet in terms of electrical specifications.

3.3.3 Applicability

Gigabit Ethernet and Fibre Channel protocols are widely used in local area network (LAN) applications for transferring large amounts of data over copper cable or glass fiber. Ten Gigabit Ethernet systems are primary used in metropolitan and wide area networks.

Devices such as TLK1211, TLK1221, and TLK2541 also support Ethernet Passive Optical Networking (EPON) applications such as EPON OLT (Optical Line Terminal) equipment. Specifically, these devices support that fast relock (Burst mode relock) requirement that EPON OLT equipment needs to implement. Typically, these devices support relock times of approximately 256 ns (consult specific data sheet for numbers).

Bus speed: Fibre Channel transceivers work at a fixed speed of 106.25 MHz on parallel interface; Gigabit Ethernet devices accept 125-MHz parallel data; XGMII works at 156.25 MHz, respectively. However, TI's Gigabit Ethernet transceivers offer extended parallel clock range. The limiting factor on minimum and maximum clock speed is the bandwidth of the fully integrated PLL. Devices such as TLK3134 (TLK313x family) supports bus speeds up to 3.7 Gbps with flexible requirements on reference clocking as well as independent channel operation. The TLK313x family of devices also incorporates built-in reference clock jitter cleaner to enable customers to use lower quality (higher jitter) reference clocks, thereby reducing implementation cost.

Bus skew: The output data stream of a Gigabit Ethernet/Fibre Channel transceiver device is device specific and independent of the input bus skew. This might help to overcome bus skew problems.

Bus Topology: All Gigabit Ethernet, Fibre Channel, CPRI, and OBSAI transceivers are used for point-to-point connections.

3.3.4 Features

- Data throughput up to 3.7 Gbps over one differential pair
- Predefined patterns for controlled data transmission
- External pins signalize data errors/loss of signal on receiving side
- Integrated clock recovery
- Capability to drive data at 3.7 Gbps over up to 80 cm of FR-4 backplane
- Serial link and device test using built-in random bit generator/verification function

Table 31. Gigabit Ethernet/Fibre Channel Device List

FAMILY	DEVICE	SERDES RATIO	THROUGHPUT	VCC AND I/O	PACKAGE
Gigabit Ethernet transceivers	TLK1201A TLK2201B	sel. 10:1 (TBI) or 5:1 DDR Device expects 8B/10B-coded data	0.6–1.3 Gbps1.0–1.6 Gbps	VDD: 2.5 V Parallel input 3.3 V tolerant Serial I/O: VML	64-pin VQF P80-ball MicroStar Junior™ BGA
Gigabit Ethernet and Ethernet PON transceivers	TLK1211 TLK1221	10:1 (TBI)	0.–1.3 Gbps	VDD: 2.5 V Parallel input 3.3 V tolerant Serial I/O: VML	64-pin VQFP 40-pin QFN

Table 31. Gigabit Ethernet/Fibre Channel Device List (continued)

FAMILY	DEVICE	SERDES RATIO	THROUGHPUT	VCC AND I/O	PACKAGE
	TLK2541	10/20 bits	1–2.6Gbps	VDD: 2.5 V Parallel input 3.3 V tolerant Serial I/O: VML	80-pin TQFP
XGMII to XAUI/ 4 Channels Independent	TLK3134	10:1 (XGMII) or 8:1 or 5:1 DDR sel. 8B/10B on-chip	0.6–3.7Gbps/channel	1.2 V Core, 1.5 V/1.8 V HSTL I/O Supply, and 2.5 V LVCMOS I/O Supply	289-ball PBGA
XAUI transceivers	TLK3114SC	10:1 DDR or 8:1 DDR (XGMII)sel. 8B/10B on-chip	10–12.5 Gbps(uncoded: 8–10)	VDD: 2.5 V Parallel input 1.5 V (1.8 V) HSTL or SSTL_2 class 1 Serial I/O: VML	289-ball PBGA
	TLK2206	5:1 DDR (RTBI)sel. 8B/10B on-chip	6–7.8 Gbps(uncoded: 4.8–6.24)	VDD: 1.8 V Parallel input: 1.5 V/1.8 V HSTL (data) and 1.8 V/2.5 V LVCMOS (control) Serial I/O: VML	196-ball PBGA
Octal Gigabit Ethernet transceiver	TLK2218	10:1 DDR or 5:1 DDRsel. 8B/10B on-chip	8–10.4 Gbps(uncoded: 6.4–8.32)	VDD: 1.8 V Parallel input: 1.8 V/2.5 V LVCMOS Serial I/O: VML	289-ball PBGA

3.4 IEEE 1394 Cable and Backplane Applications (FireWire)

The IEEE designations for a high-performance serial bus are 1394–1995,1394a–2000 and 1394b–2002. This serial bus defines both a backplane (for example, VME, FB+) physical layer and a point-to-point, cable-connected virtual bus. The backplane version operates at 12.5, 25, 50 or 100 Mbps, whereas the cable version supports data rates of 100, 200, and 400 Mbps in 1394a–2000, 100 Mbps, 200 Mbps, 400 Mbps, 800 Mbps and 1600 Mbps in 1394b. All versions are compatible at the link layer and above. The interface standard defines the transmission method, media in the cable version, and protocol.

The primary application of the cable version is the interconnection of digital A/V equipment and integration of I/O connectivity at the back panel of personal computers using a low-cost, scalable, high-speed serial interface. The 1394 standard also provides new services such as real-time I/O and live connect/disconnect capability for external devices. Furthermore, it can be used in automotive, industrial, instrumentation, and medical applications (such as motor control, surveillance, and medical monitoring, and so forth).

3.4.1 Electrical

The 1394 standard is a packet-transaction-based technology for cable- or backplane-based environments. Both chassis and peripheral devices can use this technology. The 1394 serial bus is organized as if it were memory space interconnected between devices, or as if devices resided in slots on the main backplane. Device addressing is 64 bits wide, partitioned as 10 bits for bus ID, 6 bits for node ID, and 48 bits for memory addresses. The result is the capability to address up to 1023 buses, with each having up to 63 nodes, each with 281 terabytes of memory. Memory-based addressing, rather than channel addressing, views resources as registers or memory that can be accessed with processor-to-memory transactions. Each bus entity is termed a unit, to be individually addressed, reset, and identified. Multiple nodes may physically reside in a single module, and multiple ports may reside in a single node.

Some key features of the 1394 topology are multimaster capabilities, live connect/disconnect (hot plugging) capability, genderless cabling connectors on interconnect cabling, and dynamic node address allocation as nodes are added to the bus. Another feature is that transmission speed is scalable from approximately 100 Mbps to 800 Mbps. Future devices will support 1.6 Gbps and 3.2 Gbps, as well.

Nodes can act as a repeater, allowing them to be chained together to form a relatively unrestricted topology. 1394-1995 and 1394a-2000-based cable PHYs (physical layer devices) use cables with power wires. 1394 Equipment/Devices that are not switched on can still power the PHYs from the 1394-bus, thus acting as a repeater or hub. Equipment with low power consumption can be powered directly from the 1394 bus. By using the maximum number of 16 hops (1394a–2000 allows 24 hops) with regular 4.5-m cables, a maximum end-to end distance of 72 m is reached. 1394b–2002 defines new transmission media and modulation types. Data can now be transmitted over several types of optical cables and low-cost, twisted-pair cables. Heterogeneous networks allow optimum solutions in terms of cost (use electrical

where possible; use optical where needed). Although remote powering across optical cable sections is not possible anymore with 1394b, this standard extension is still backward compatible to 1394-1995. An optical cable cannot be connected to an electrical outlet (in this case, a simple cable converter is required). Bilingual PHYs like the TSB81BA3 are used as translators between the 1394-1995, 1394a-2000 world (that use DS coding), and the 1394b world (that use 8B10B coding).

DS coding in 1394-1995 and 1394a is a method that uses common-mode DC signals for arbitration and speed signaling; an encoded clock that can easily be recovered simplifies fast detection of data with different speeds.

8B10B coding in 1394b allows DC-free data transmission which is needed when transformers or capacitors (to separate ground domains) are used in the signal path. The bit representation is the same for electrical as for optical, it just needs an optical transceiver to go optical (LED-driver and LED on TX, photodiode and sense amplifier on RX).

It's simple! If you can connect it with cables, it is compatible back and forth (from 100 Mbps to 3.2 Gps).

Table 32. 1394 PMD Connection Matrix

SPEED	REACH	100DS	200DS	400DS	100	200	400	800	1600
STP (1394cbl)	4.5 m	1394-1995	1394-1995	1394-1995			1394b	1394b	1394b
UTP-5	100 m				1394b				
POF	50 m				1394b	1394b			
HPCF	100 m				1394b	1394b			
MMF	100 m						1394b	1394b	1394b
Remote Power	na	yes	yes	yes			On STP	On STP	On STP

3.4.2 Protocol

Both asynchronous and isochronous data transfers are supported. The asynchronous format transfers data and transaction layer information to an explicit address. The isochronous format broadcasts data based on channel numbers rather than specific addressing. Isochronous packets are issued on the average of each 125 μs in support of time-sensitive applications. Providing both asynchronous and isochronous formats on the same interface allows both real-time and nonreal-time critical applications on the same bus.

The cable environment's tree topology is resolved during a sequence of events triggered each time a new node is added or removed from the network. This sequence starts with a bus reset phase, where previous information about a topology is cleared. The tree ID sequence determines the actual tree structure, and a root node is dynamically assigned, or it is possible to force a particular node to become the root. After the tree is formed, a self-ID phase allows each node on the network to identify itself to all other nodes. During the self-ID process, each node is assigned an address. After all of the information has been gathered on each node, the bus goes into an idle state waiting for the beginning of the standard arbitration process.

An additional feature is the ability of transactions at different speeds to occur on a single device medium (for example, some devices can communicate at 100 Mbps whereas others communicate at 200 Mbps, 400 Mbps, or 800Mbps). Use of multispeed transactions on a single IEEE 1394 serial bus requires consideration of each node's maximum capabilities when laying out the connections to ensure that a device with lower-rate capabilities does not restrict the path between two higher-speed nodes.

The backplane physical layer shares some commonality with the cable physical layer. Common functions include bus state determination, bus access protocols, encoding and decoding functions, and synchronization of received data to a local clock.

3.4.3 Applicability and Typical Application for IEEE 1394

The transmission of data without burdening the host unit creates a huge market for IEEE 1394. Not only does the computer-based equipment in private households require an interface solution for the home and home office network, but also the evolving markets of digital broadcasts, interactive services, games, and home shopping require a high-speed network. The introduction of digital set top boxes enable the reception of these services and enables the capability to transmit digital data not only to consumer devices like digital TV, but also to PC and storage media. Beside the consumer, PC, and PC peripheral markets, IEEE 1394 can cover many industrial applications.

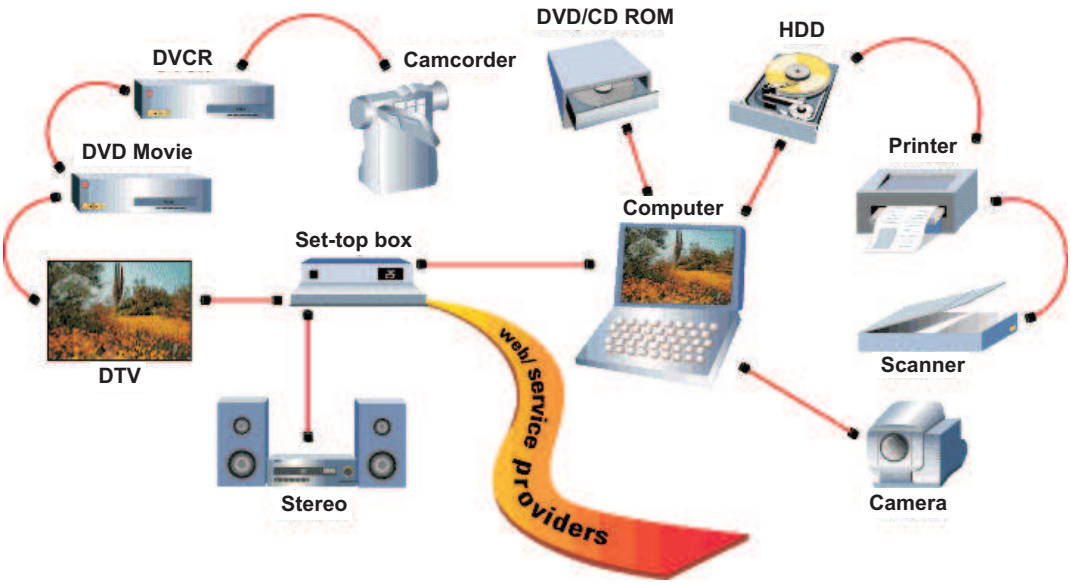


Figure 29. Possible Interconnections Using 1394 as Interface

3.4.4 Applicability and Typical Application for IEEE 1394 Backplane

The 1394 backplane serial bus (BPSB) plays a supportive role in backplane systems, specifically GTLP, Futurebus+™, VME64, and proprietary backplane bus systems. This supportive role can be grouped into three categories:

- **Diagnostics:** Alternate control path to the parallel backplane bus; test, maintenance, and troubleshooting; and software debug and support interface.
- **System enhancement:** Fault tolerance; live insertion; CSR access; and auxiliary bus to the parallel backplane bus
- **Peripheral monitoring:** Monitoring of peripherals (disk drives, fans, power supplies, and so forth, with 1394 cable serial bus)

The TSB14AA1 and SN74GTLP1394 provide a way to add high–speed 1394 connections to almost any backplane.

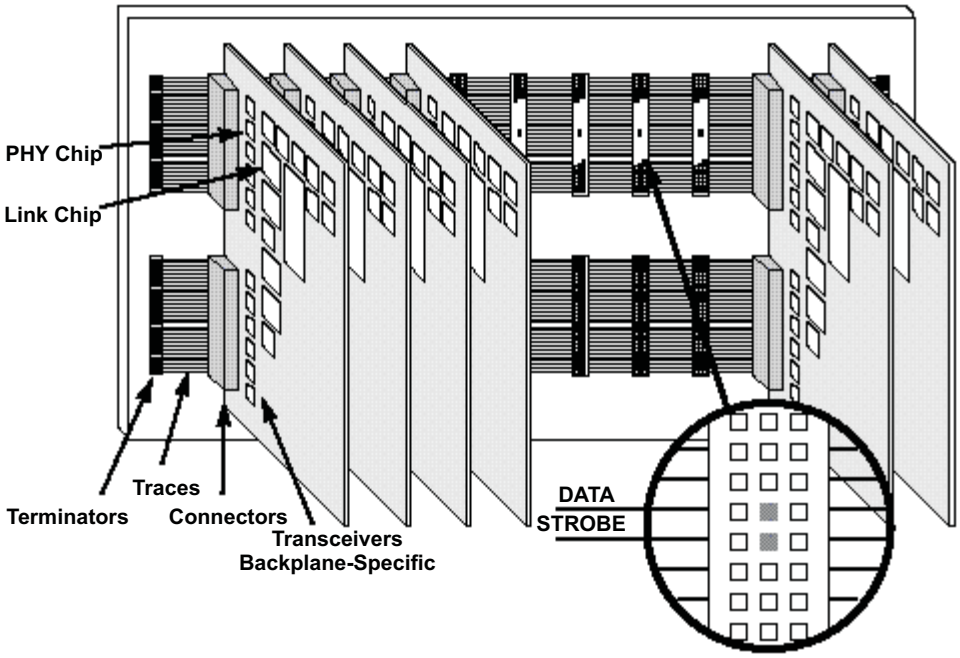


Figure 30. Principle Application Setup Using 1394 Interface

3.4.5 Features

- Real-time data transfer for multimedia applications (ensured bandwidth assignments)
- Data rates of 100, 200, and 400 Mbps for high-speed applications in cable environments in 1394a-2000 and 100, 200, and 400, 800 Mbps data rates with 1394b-2002
- 2Data rates of 5 and 50 Mbps for backplane environments
- Live connection/disconnection without data loss or interruption
- Automatic configuration supporting plug and play
- Free network topology allowing branching and daisy-chaining
- Ensured bandwidth assignments for real-time applications

Table 33. Top IEEE 1394 Link Layer Device List (PC)

DEVICE	SPEED	POWER	PACKAGE
TSB12LV26	400 Mbps	3.3 V (5-V tolerance)	100-pin TQFP
TSB12LV21B	400 Mbps	3.3 V (5-V tolerance)	176-pin TQFP
TSB42AA9A	400 Mbps	3.3 V (5-V tolerance)	100-pin TQFP
TSB82AA2	800 Mbps	3.3 V	144-pin LQFP
XIO2213A	800 Mpbs	3.3 V	167-pin PBGA

Table 34. Top IEEE 1394 Integrated Device List (PC)

DEVICE	PORTS	SPEED	POWER	PACKAGE
TSB43AB21A	1	400 Mbps	3.3 V (5-V tolerance)	128-pin TQFP
TSB43AB22A	2	400 Mbps	3.3 V (5-V tolerance)	128-pin TQFP
TSB43AB23	3	400 Mbps	3.3 V (5-V tolerance)	128-pin TQFP

Table 35. Top IEEE 1394 Integrated Device List (Non-PC)

DEVICE	PORTS	SPEED	POWER	PACKAGE
TSB43AA82A	2	400 Mbps	3.3 V (5-V tolerance)	144-pin LQFP
TSB43CA43A	3	400 Mbps	3.3 V (1.8-V core)	176-pin LQFP
TSB43CB43A	3	400 Mbps	3.3 V (1.8-V core)	176-pin LQFP

Table 36. Top IEEE 1394 Link Layer Device List (Non-PC)

DEVICE	SPEED	POWER	PACKAGE
TSB42AA4	400 Mbps	3.3 V (5-V tolerance)	128-pin TQFP
TSB42AB4	400 Mbps	3.3 V (5-V tolerance)	128-pin TQFP
TSB12LV01B	400 Mbps	3.3 V (5-V tolerance)	100-pin TQFP
TSB12LV32	400 Mbps	3.3 V (5-V tolerance)	100-pin TQFP

Table 37. Top IEEE 1394 Physical Layer Device List

DEVICE	PORTS	SPEED	POWER	PACKAGE
TSB41AB1	1	400 Mbps	3.3 V (5-V tolerance)	48-/64-pin TQFP
TSB41AB2	2	400 Mbps	3.3 V (5-V tolerance)	64-pin HTQFP
TSB41AB3	3	400 Mbps	3.3 V (5-V tolerance)	80-pin HTQFP
TSB41LV04A	4	400 Mbps	3.3 V (5-V tolerance)	80-pin HTQFP
TSB41BA3	3 (bilingual)	400 Mbps	3.3 V	80-pin TQFP
TSB41LV06	6	400 Mbps	3.3 V (5-V tolerance)	100-pin HTQFP
TSB81BA3	3 (bilingual)	800 Mbps	3.3 V (1.8-V core)	80-pin HTQFP
TSB14AA1A (Backplane)	1	100 Mbps	3.3 V	68-pin TQFP
TSB14C01A (Backplane)	1	100 Mbps	5 V	68-pin TQFP

3.5 PCI/CompactPCI

The primary goal of the PCI developers was a low-cost, flexible, high-performance industry standard local bus architecture. To enable portable systems with PCI bus, low-power dissipation also was a requirement. Personal computers have been the first area where the PCI became the standard for local buses. Meanwhile, the PCI bus has become a major player in the industrial area. For industrial applications, the form factor changed to CompactPCI and the hot-swap function has been included. The PCI Special Interest Group (PCI SIG: http://www.pcisig.com) maintains the specifications of the PCI bus and the PCI Industrial Computer Manufacturers Group (PICMG: http://www.picmg.org/) takes care of the CompactPCI specification.

3.5.1 Electrical

- Address space: 32 bit
- Data path: 32 or 64 bit
- Bus clock speed: 33 MHz and 66 MHz
- Maximum data rate: 1 Gbps for 33 MHz/32-bit bus; 4 Gbps for 66 MHz/64-bit bus
- Two major form factors:
  - Personal Computer: 62-pin connector for 32-bit systems (Figure 31) and 82-pin connector for 64-bit systems.
  - CompactPCI: Eurocard industry standard, both 3U (100 mm by 160 mm) and 6U (233.35 mm by 160 mm) board sizes (Figure 32)
- CMOS drivers; TTL voltage levels
- 5-V, 3.3-V interoperable

- Reflected wave switching, thus the bus is short. To increase the number of connected devices PCI-to-PCI bridges are necessary. Figure 33 shows a PCI system with 8 PCI buses.
- Direct drive – no external buffers

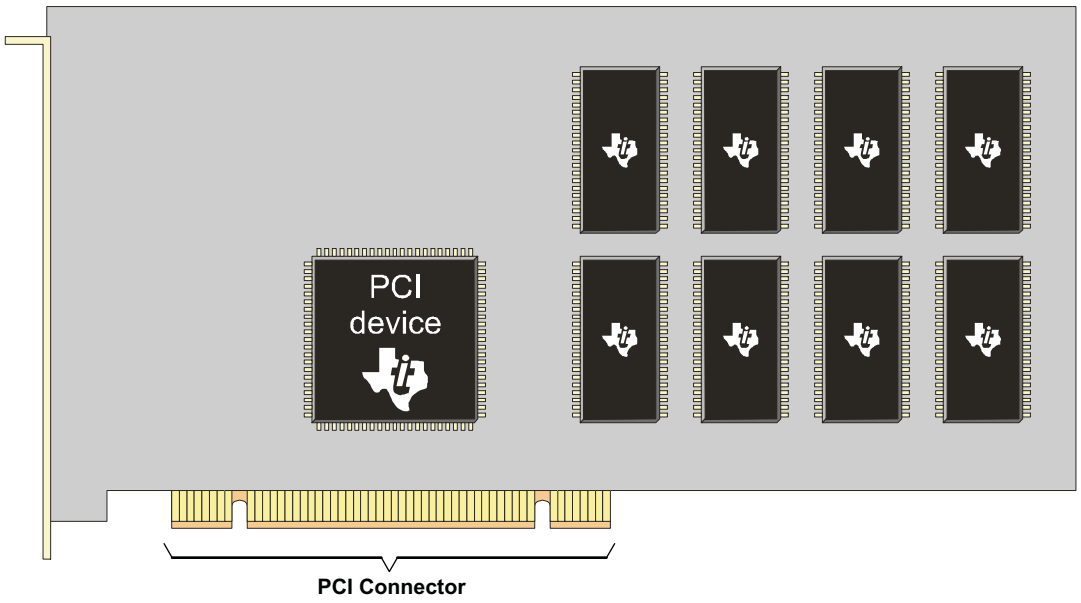


Figure 31. PCI Card for Personal Computer

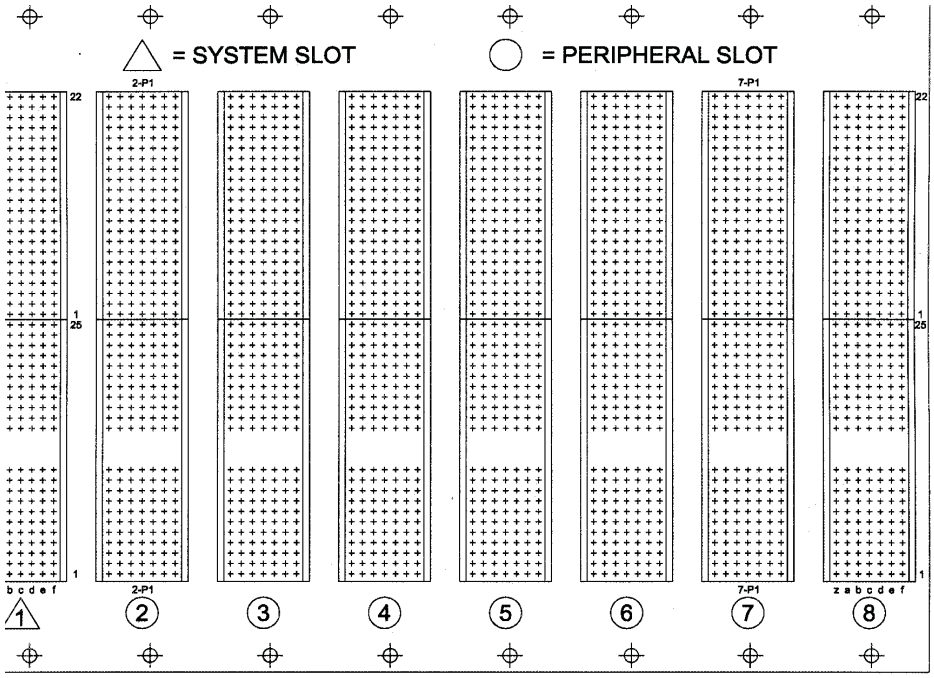


Figure 32. CompactPCI Backplane

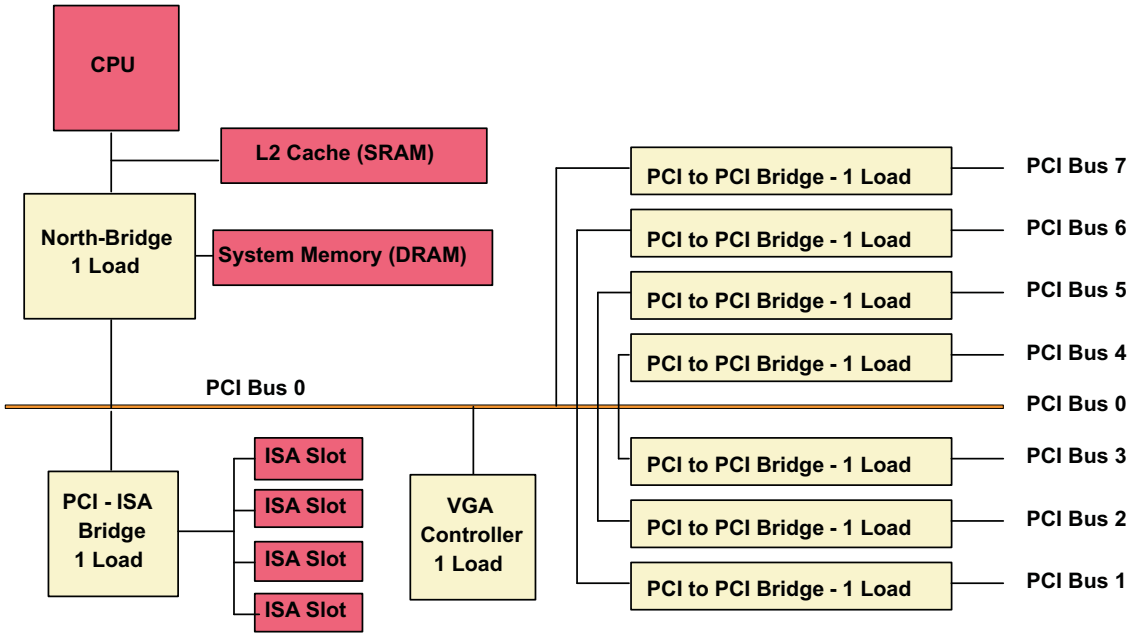


Figure 33. PCI Bus System With 8 PCI Buses

3.5.2 Protocol

PCI devices are not configured after the supply power is switched on. None of the devices have a memory or address range assigned, and no interrupts are available. To operate a PCI bus, all connected devices (master and slaves) have to be configured. Through the configuration space the controller reads the requirements of a device and is able to assign memory, I/O-space, and Interrupts. This enables plug-and-play systems.

In large systems with multiple PCI buses, the configuration software needs an enumerator to number all buses in the system and to program the PCI-to-PCI bridges accordingly.

During operation, each device on the bus can become the master and can transfer data to any other bus member. The bus design requires burst transfers to work efficiently. Single- byte transfers are still possible.

3.5.3 Applicability

The PCI bus is a computer bus system. The first and biggest success was the personal computer. Nearly every system in the world is equipped with a PCI bus system. High data rates, low cost, multimedia support, and scalability have been key features of the PCI bus that led to its success.

Notebook computers take advantage of the low-power consumption. The reflected wave switching design does not require any termination or additional bus drivers. The disadvantage is a short bus length that can be increased using PCI-to-PCI bridges. Notebook docking stations often use PCI-to-PCI bridges to generate a new PCI bus in the docking unit.

In the industrial area, CompactPCI has gained significant market share. CompactPCI comes in a Eurocard industry standard rack and supports hot swapping. According to the requirements of the industrial environment, high-quality connectors with hot-swap support are used for CompactPCI. Besides hot-swap capabilities, the electrical specifications and protocols are identical to PCI. Especially in telecommunication and server applications, 66-MHz and 64-bit systems are used.

3.5.4 Features

- Processor independent
- Multimaster; peer-to-peer

- Supports memory, I/O, and configuration space
- Data bursting as normal operation mode – both read and write – variable burst length
- Low latency assurances for real-time devices
- Initialization hooks for auto-configuration
- Arbitration: central, k access oriented, and hidden
- 64-bit extension transparently interoperable with 32-bit

Table 38. Top Device List - PCI Products

DEVICE	SPECIFICATION	DESCRIPTION	PACKAGE	STATUS
PCI1410A	PCI 2.2	PCI-to-CardBus bridge for one cardbus slot	144-pin LQFP 144-pin BGA CSP	Available
PCI1510	PCI 2.2	PCI- to-CardBus bridge for one cardbus slot (successor of PCI1410A)	208-pin LQFP 209-ball PBGA	Available
PCI1420	PCI 2.2	PCI-to-CardBus bridge for two cardbus slots	208-pin LQFP 209-pin BGA CSP	Available
PCI1520	PCI2.2	PCI-to-CardBus bridge for two cardbus slot (successor of PCI1420)	208-terminal LQFP 209-ball PBGA	Available
PCI1450	PCI 2.2	PCI-to-CardBus bridge for two cardbus slots and integrated zoom-video support	256-pin LQFP 256-pin BGA 257-pin BGA CSP	Available
PCI4410	PCI 2.2	PCI-to-CardBus/1394 bridge for one cardbus slots, integrated zoom-video support	208-pin BGA 209-pin BGAS CSP	Available
PCI4450	PCI 2.2	PCI-to-CardBus/1394 bridge for two cardbus slots, integrated zoom-video support	256-pin BGA 257-pin BGAS CSP	Available
PCI2031	PCI 2.2	PCI-to-PCI bridge, 32-bit, 33 MHz, 6 secondary master	176-pin LQFP	Available
PCI2250	PCI 2.2	PCI-to-PCI bridge, 32-bit, 33 MHz, 4 secondary master	160-pin LQFP 176-pin LQFP	Available
PCI2050/PCI2050A	PCI 2.2	PCI-to-PCI bridge, 32-bit, 33/66 MHz, 9 secondary master	208-pin LQFP 209-pin BGA CSP	Available
PCI2040	PCI 2.2	PCI-to-DSP bridge	144-pin LQFP 144-pin BGA CSP	Available

3.6 SONET/SDH Transceivers

SONET, or Synchronous Optical NETwork, and SDH, or Synchronous Digital Hierarchy, are similar standards defining the data speeds, data formats and electrical/optical performance of the link for optical networks. SONET is a US standard while SDH is the European counterpart.

3.6.1 Electrical

Several electrical interfaces are defined by ANSI and OIF groups for use in SONET/SDH systems. One of them is the SerDes-Framer Interface SFI-4 described in the OIF-SFI4-01.0 specification. This interface consists of

- 16 LVDS data bits in each direction
- Source-synchronous manner on 622.08-MHz (optional 311.04 MHz DDR) LVPECL clock
- Framer Transmit Clock signal sourced by SerDes device
- Receive Loss of Synchronization Error signal is used by OC-192 devices.

3.6.2 Protocol

SONET/SDH standards prescribe using specific protocols for controlled data transmission. Detailed description of these standards is beyond the scope of this report.

It is unnecessary, however, to provide full specification-compliant data to the transceiver device (PHY) to ensure its functionality. It is important to know, that SONET/SDH transceivers expect scrambled data (scrambling polynomial: $1 + x^6 + x^7$) on their parallel interfaces.

3.6.3 Applicability

SONET/SDH technology dominates in wide area networks (WAN). SONET/SDH links are point-to-point optical connections.

Bus speed: SONET/SDH parallel buses work at fixed speeds, such as: 38.88 MHz (OC-3/STM-1), 155.52 MHz (OC-12/STM-4), 311.04 MHz (OC-24/STM-8), and 622.08 MHz (OC-48 and 192/STM-16 & 64).

3.6.4 Features

- Data throughput up to 9.953 Gbps (OC-192/STM-64)
- Worldwide synchronous data transmission enabling adding/dropping of data within one single multiplexing process
- Forward Error Correction applicable (PHY devices often support FEC speed, which differs from the original frequencies)

Table 39. SONET/SDH Device List

DEVICE	SERDES RATIO	THROUGHPUT	VCC AND I/O	PACKAGE
SLK25x1	4:1	OC-3/12/24/48	VDD: 2.5 V Parallel input: LVDS (OIF99.102) Serial I/O: CML (PECL compliant)	100-pin PQFP
SLK27x1		OC-3/12/24/48 + FEC		

3.7 Universal Serial Bus

Flexibility, expandability, and ease of use are all important in meeting the needs of the growing numbers of PC users. The USB standard is an important tool that gives a simple way to expand a system in a virtually unlimited number of ways. Most important, this functionality is available today.

USB is designed to simplify the user's effort by combining the PC's many existing interfaces, like the TIA-232C serial ports, parallel port, game/MIDI port and more, into a single, easy-to-use connector. In itself, this capability greatly reduces the complexity of the system and gives manufacturers the ability to develop highly integrated products. The USB's true plug-and-play capability also signals an end to the often complex process of adding system peripherals.

3.7.1 Electrical

The USB physical interconnect is a tiered star topology. A hub is at the center of each star. Each wire segment is a point-to-point connection between the host and a hub or function, or a hub connected to another hub or function. The USB transfers signal and power over a four-wire cable. The signaling occurs over two wires on each point-to-point segment.

The three data rates of USB are low-speed that has a limited capability signaling mode at 1.5 Mbps, full-speed signaling bit rate at 12 Mbps, and high-speed mode at 480 Mbps. All modes can be supported in the same USB bus by automatic dynamic mode switching between transfers. The low-speed mode is defined to support a limited number of low-bandwidth devices, such as a mouse, because more general use would degrade bus utilization. The clock is transmitted, encoded along with the differential data. The clock encoding scheme is NRZI with bit stuffing to ensure adequate transitions. A SYNC field precedes each packet to allow the receiver(s) to synchronize their bit recovery clocks. The cable also carries VBUS and GND wires on each segment to deliver 5- V power to devices.

3.7.2 Protocol

The USB is a polled bus. The host controller initiates all data transfers.

All bus transactions involve the transmission of up to three packets. Each transaction begins when the host controller, on a scheduled basis, sends a USB packet describing the type and direction of transaction, the USB device address, and endpoint number. This packet is referred to as the token packet. The addressed USB device selects itself by decoding the appropriate address fields. In a given transaction, data is transferred either from the host to a device or from a device to the host. The direction of data transfer is specified in the token packet. The source of the transaction then sends a data packet or indicates it has no data to transfer. The destination, in general, responds with a handshake packet indicating whether the transfer was successful.

The USB data transfer model between a source or destination on the host and an endpoint on a device is referred to as a pipe. A pipe can be one of two types: stream or message. Stream data has no USB-defined structure, whereas message data does. Additionally, pipes have associations of data bandwidth, transfer service type, and endpoint characteristics like directionality and buffer sizes. Most pipes come into existence when a USB device is configured. One message pipe, the default control pipe, always exists once a device is powered, to provide access to the device's configuration, status, and control information.

The transaction schedule allows flow control for some stream pipes. At the hardware level, this prevents buffers from underrun or overrun situations by using a negative acknowledgment handshake to decrease the data rate. When negative acknowledged, a transaction is retried when bus time is available. The flow control mechanism permits the construction of flexible schedules that accommodate concurrent servicing of a heterogeneous mix of stream pipes. Thus, multiple stream pipes can be serviced at different intervals and with packets of different sizes.

3.7.3 Applicability and Typical Applications

USB is a PC-centric system designed to interconnect up to 127 peripherals to the PC including the ones pictured in Figure 34: keyboard, mouse, printer, modem, and so forth. Due to the tiered star topology, a hub is needed at the center of each star.

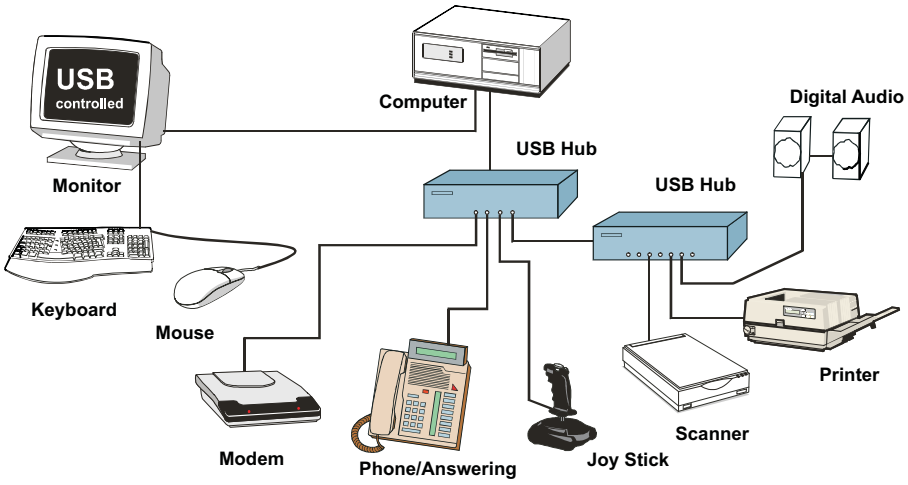


Figure 34. USB – Tiered Star Topology

3.7.4 Features

- Single PC supports up to 127 devices
- Bit transfer rates of 1.5 Mbps,12 Mbps and 480 Mbps supported
- Ends confusion of multiple add-in cards for ease of use
- Universal connectors and cables for all devices and applications
- Auto configuration on connection for real plug and play
- Ensured bandwidth for real-time applications

Table 40. Top USB Device List

DEVICE	DOWNSTREAM PORTS	SPECIAL FEATURE	POWER	PACKAGE
TUSB2036	2/3	Serial EEPROM IF	3.3 V	32-pin LQFP
TUSB2136	2	Integrated 8052 microcontroller	3.3 V	64-pin LQFP
TUSB2046B	4	Serial EEPROM IF	3.3 V	32-pin LQFP
TUSB2077A	7	Serial EEPROM IF	3.3 V	48-pin LQFP
TUSB3210	X	Full-speed USB-enabled 8052 MCU	3.3 V	64-pin LQFP
TUSB3410	X	Full-speed USB to RS-232/IrDA serial converter	3.3 V	32-pin LFQP
TUSB6250	X	High-speed USB 2.0 to IDE Bridge		80-pin TQFP
TUSB6015	X	NOR-flash host interface for seamless connectivity to OMAP™ processors	3.3, 1.8, 1.5 V	80-pin MicroStar Junior™ BGA

3.8 On-the-Go Universal Serial Bus (USB OTG)

USB On-the-Go (OTG) is an addendum to the USB 2.0 Specification that defines:

- A new type of *dual-role* device intended to extend the functionality of a peripheral product to include limited host capabilities.
  - OTG host must supply power; however, the required supply current is limited to 8 mA.
- New negotiation rules
  - HNP defines a method for dynamic switching between host and device roles.
  - SRP enables a method for bus power to be turned off/on at the discretion of the *host* device.
- New microconnectors

Target applications are portable devices with which end-users want to share data when a computer is not available.

- Sharing contact information between two PDAs or cell phones
- Sharing pictures from one DSC or camera phone with another
- Sharing music between portable audio players
- Printing directly from a DSC or PDA

Like standard USB, OTG is a point-to-point, host-centric bus and is not intended as a peer-to-peer networking connection.

3.8.1 Applicability and Typical Applications of OTG

Usage Scenario 1:

- OTG-enabled device is required to act as a standard USB peripheral.
  - Can be class device such as Media Transfer Protocol (MTP)-complaint MP3 Player or Mass Storage Class Peripheral (MSC)
  - Can require user to load a customized driver onto PC to enable functionality
- Example applications:
  - Synchronizing PDA/telephone contacts
  - Synchronizing music library for MP3 Players
  - Copying pictures from DSC to PC for editing/printing

Figure 35. Example of USB OTG Desktop-to-PDA Application

Usage Scenario 2:

- DEVICE is USB OTG host to target peripheral
- OTG-enabled device is required to implement the operating system
  - Drivers must be included in support of Target Peripheral List (TPL)
  - Messaging must be enabled to notify for nonsupported peripheral connection event
  - Must supply a minimum of 8 mA (5 V) of USB power
- Example applications:
  - Adding keyboard or mouse to a PDA
  - Updating contents of PDA/telephone from USB flash memory
  - Copying pictures from DSC to USB flash memory

Figure 36. Example USB OTG PDA-to-Memory Application

Usage Scenario 3

- Host device is required to implement the operating system – including drivers – in support of the targeted peripherals.
- Peripheral device is required to implement the desired type of USB peripheral.
- Host Negotiation Protocol can enable role reversal if cable connected backwards.
- Example applications:
  - Sharing PDA/telephone contacts
  - Sharing music between MP3 Players

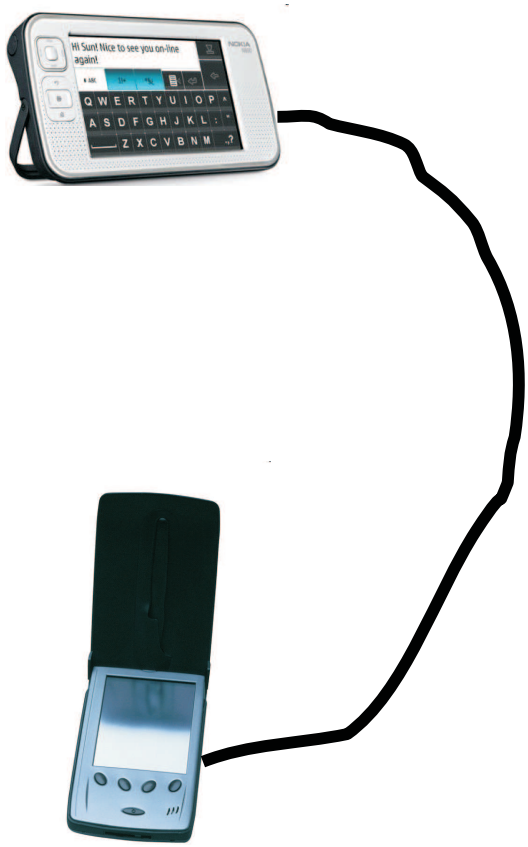


Figure 37. Example USB OTG PDA-to-PDA Application

Table 41. Top USB OTG Device List

DEVICE	DOWNSTREAM PORTS	SPECIAL FEATURE	POWER	PACKAGE
TUSB6010B	1	NOR-flash host interface	3.3, 1.8, 1.5 V	80-pin MicroStar Junior™ BGA
TUSB6020	1	VLYNQ host interface	3.3, 1.8, 1.5 V	80-pin MicroStar Junior™ BGA 80-Pin PFC

3.9 FPD-Link III

Flat panel display link III, or known as FPD-Link III, is an interface used in many automotive applications to transport video from point to point. This interface enables the transport of high-definition digital video, as well as a bidirectional control channel, over a low-cost cable, either twisted pair or coax. There are FPD-Link III serializers and deserializers (SerDes) that have been optimized either for the link between a processor and a display, or between the processor and a camera (see *FPD-Link III -- Doing More With*

Less (SLYT581) for more information). article provides an overview of these links, the advances that can be expected in the near future, and how to get even more out of the technology (see *An EMC/EMI System-Design and Testing Methodology for FPD-Link III SerDes* (SLYT719) for more information). This presents system-design guidelines that aid in EMI/EMC system design and the testing of FPD-Link III high-speed serializers and deserializers.

4 Data Signal Conditioners and Translators

These circuits are often used with data-line drivers and receivers or data links.

4.1 Clock Distribution Circuits (CDC)

Every digital system needs clock signals to synchronize the system activity. TI is developing new CDC products to meet the growing demand and high-performance expectations of the communications, wireless infrastructure, optical networks, DIMM, and consumers markets.

To meet the stringent clock-signal timing requirements of today's system, a series of single-ended and differential clock buffers, low-jitter zero-delay buffers, clock synchronizer and jitter cleaner, Rambus clock generators, and synthesizers are available.

4.1.1 Electrical

This type of circuits has no industry standard except clock circuits for DIMM (SRAM, DDR, and Rambus).

Clock Buffer/Driver: The clock distribution circuit receives one input clock and distributes the input clock to a several clock outputs with same frequency.

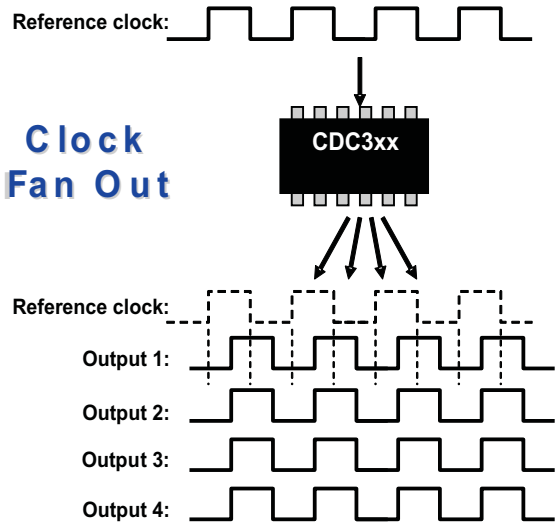


Figure 38. Clock Buffer/Driver Diagram

Zero Delay Buffer: Zero delay buffer is a PLL-based circuitry whose input clock edge is in phase with the output clock edge so that the delay between inputs to output becomes almost zero.

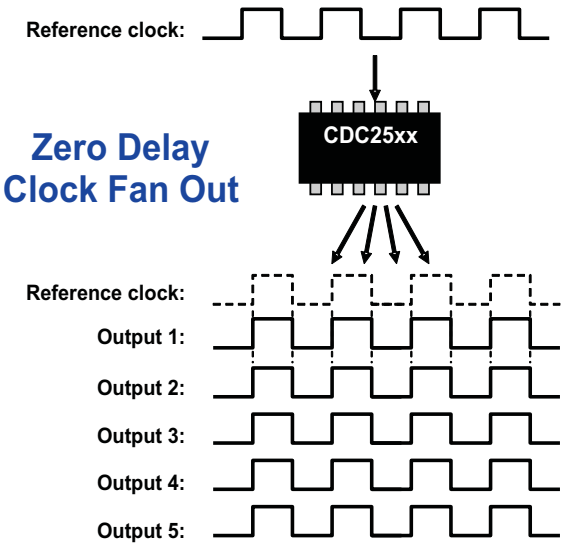


Figure 39. Zero Delay Buffer Diagram

Clock Synchronizer and Jitter Cleaner: Clock synchronizer and jitter cleaner are low phase noise and low skew clock circuits that synchronize a highly accurate VCXO clock to a reference clock. It outputs a precise and low-jitter clock.

Clock Generator/Synthesizer: The PLL-based clock circuitry receives low-frequency signal from crystal or other source and delivers different frequency output signals according to the system's need.

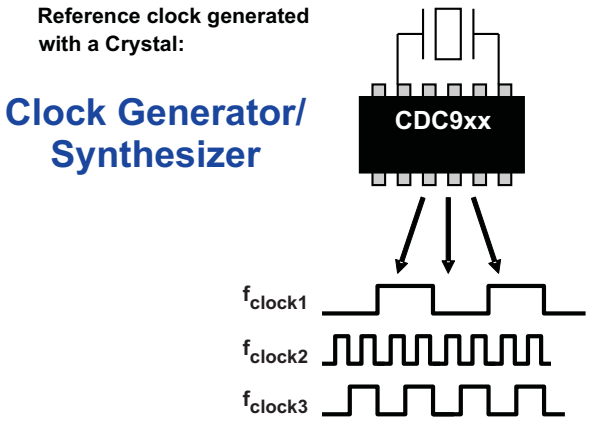


Figure 40. Clock Generator Diagram

4.1.2 Applicability

No protocol is specified for CDC devices. CDC devices depend on application. However, the following definitions of some parameters are related to clock drivers.

Propagation Delay: Propagation delay is the time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high-to-low) to the other (low-to-high) defined level.

Output Skew: Output skew is the difference between propagation delays of any two outputs of the same device at identical transitions.

Pulse skew: Pulse skew is the magnitude of the time difference between the high-to-low and the low-to-high propagation delays when a single switching input causes one or more outputs to switch.

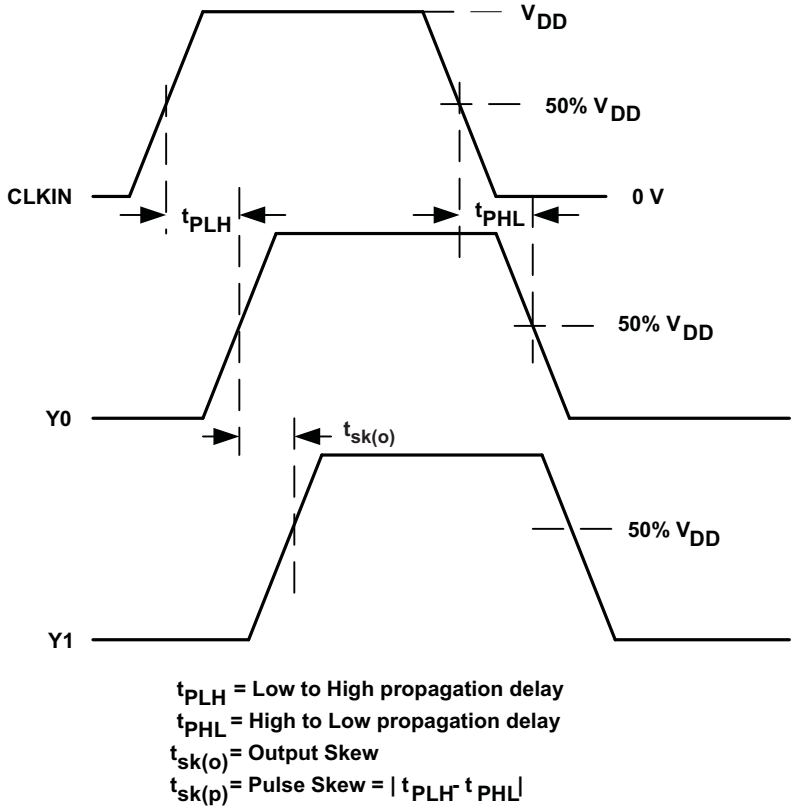


Figure 41. Input and Outputs Waveforms

Part-to-Part Skew: Part-to-part skew is defined as the magnitude of the difference in propagation delays between any specified outputs of two separate devices operating at identical conditions. The devices must have the same input signal, supply voltage, ambient temperature, package, load, environment, and so forth.

Static Phase Offset: The time difference between the averaged input reference clock and the averaged feedback input signal when the PLL is in locked mode.

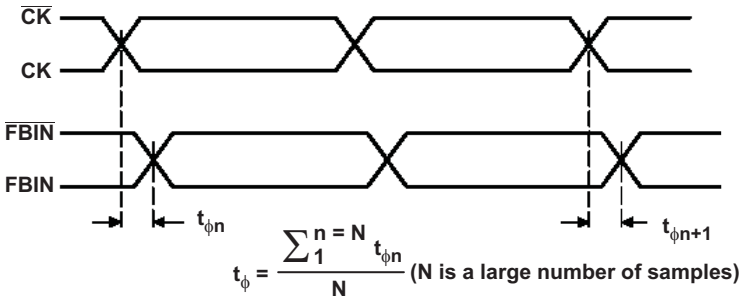


Figure 42. Static phase offset

Dynamic Phase Offset: the phase difference between input clock and feedback input clock due to the PLL's inability to instantaneously update the feedback clock when the period of the input clock changes.

Jitter: Dispersion of a time parameter of the pulse waves in a pulse train with respect to reference time, interval, or duration.

Peak-to-Peak Jitter: Peak-to-peak jitter is defined as the upper and lower bounds of a large number of samples of cycle-to-cycle period measurements from ideal.

Cycle-to-Cycle Jitter: Cycle-to-cycle jitter is the difference in the period of successive cycles of a continuous clock pulse train.

PLL Loop Bandwidth: PLL loop bandwidth is that region where the PLL is able to track for phase and frequency modulation of the reference signal as long as the modulation frequencies remain as an angular frequency band roughly between zero and PLL's natural frequency.

Spread Spectrum Clock (SSC) Compatibility: A PLL clock driver is SSC-compatible if the PLL is able to track the modulation profile and frequency is minimum tracking skew.

4.1.3 CDC Clocks With TI SerDes

All SerDes require very low jitter clock to perform its operation correctly. As the input duty cycle and jitter are critical to SerDes operation, TI clocks are readily available to meet the requirements. The peak-peak jitter requirement of TLK1201, TLK1501, TLK2201, TLK2501, TLK2701, TLK2711, and TLK3101 is less than 40 ps and CDCV304 just adds 20 ps p-p jitter on average. So, CDCV304 is an excellent clock driver for these SerDes.

The RMS jitter requirement of SLK2501 and SLK3104 is less than 3 ps and CDCVF111 and CDC111 add negligible jitter to its output. This differential clock driver has nine outputs and low output skew.

Table 42. Recommended Clock Drivers for Serial/Gigabit Transceivers

SERIAL/GIGABIT TRANSCEIVER	RECOMMENDED CLOCK DRIVER
SLK2501	CDCVF111 up to 622.08 MHz CDC111 up to 500
TLK3104SC	CDCVF111 up to 622.08 MHz CDC111 up to 500 MHz
TLK3114SA	CDC111/CDCVF111
TLK1201, TLK1501, TLK2201, TNETE2201B, TLK2501, TLK2701, TLK2711, TLK3101	CDCV304 up to 200 MHz

4.1.4 Memory Clock Driver

TI is offering the PLL clock drivers for PC100/133 and Double Data Rate (DDR) memory. These clock drivers are JEDEC standard compliant. For robust design and advanced process, these PLLs are widely used in the buffed DIMM module.

Table 43. Clock Drivers for Memory module

CLOCK DRIVER	APPLICATION SPACE
CDCVF2510, CDCVF2509	PC100/133
CDCV857, CDCV857A, CDCV857B, CDCU877	DDR

4.1.5 High-Speed LVDS/LVPECL/LVTTL Clock Buffers

The communication and ONET world need low-jitter, high-speed clock buffers. The precise clock is the backbone of their whole operation. TI is offering many high-speed differential clocks especially suitable for this space.

Table 44. Clock Buffers

DEVICE NAME	DESCRIPTIONS
CDCVF111/CDC111	1:9 Differential PECL clock buffer
CDCLVP110	2:10 PECL high-frequency clock driver
CDCLVD110	2:10 LVDS clock driver
CDCVF2310	1:10 LVTTL clock buffer

4.1.6 Adjusting Input to Output Delay

The phase-locked-loop (PLL) drivers can adjust the input-to-output delay by simply changing feedback length or feedback and load capacitance. The PLLs make the input-to-output delay zero by comparing the feedback signal with input signal, but the PLLs also can advance the output edge with respect to input edge.

Table 45. Adjustable-Delay Clock Drivers

DEVICE NAME	DESCRIPTIONS
CDCVF2505	1:5 PLL clock driver
CDCVF25081	1:8 PLL clock driver
CDCV855	1:5 Differential PLL clock driver
CDCV850	1:10 Differential PLL clock driver

4.1.7 Jitter Cleaner

In communications and many other applications, low clock jitter is the most critical requirement. An effective way is to use a PLL with low loop bandwidth to filter the noise of the reference clock. TI plans to offer the clock circuits, which can filtrate out the jitter from reference clock.

Table 46. Jitter Cleaners

DEVICE NAME	DESCRIPTIONS
CDC5801	Low-cost jitter cleaner
CDC7101	All digital PLL multiplier/divider with jitter clean up
CDC7005	High-performance clock synthesizer with jitter clean up and selectable loop bandwidth

4.1.8 Multipliers and Dividers

TI offers a number of clock multiplying and dividing circuits. The PLL-based multiplier and divider have low jitter and output skew.

Table 47. Clock Multipliers and Dividers

DEVICE NAME	DESCRIPTIONS
CDC5801	4x, 6x, 8x and 1/2x, 1/3x, 1/4x clock multiplier and divider
CDC536, CDC2536, CDC582, CDC2582, CDC586, CDC2586	1x, 1/2x and 2x options
CDC25084	4x multiplier

4.1.9 Clock Generators

The clock generators can be programmed to generate different frequencies from one crystal or LVCMOS clock input. Some of the features of these devices include are Spread Spectrum Clocking (SSC), EEPROM programming, low jitter, and 0-PPM clock generation.

Table 48. Clock Generators

DEVICE NAME	DESCRIPTIONS
CDCE906, CDC906	3-PLL, 6 outputs, 167 MHz
CDCE706, CDC706	3-PLL, 6 outputs, 300 MHz
CDCEL913, CDCE913	1-PLL, 3 outputs, 230 MHz, VCXO
CDCEL925, CDCE925	2-PLL, 5 outputs, 230 MHZ, VCXO
CDCEL937, CDCE937	3-PLL, 7 outputs, 230 MHz, VCXO
CDCEL949, CDCE949	4-PLL, 9 outputs, 230 MHz, VCXO

4.2 Digital Isolators

As today's electronics technology pushes the envelope of making things smaller, faster, and more accurate, it is inevitable that galvanic isolation technology also needs to be updated. Up until a few years ago, optically coupled isolators (opto-couplers) were the only choice available to electronics engineers to be able to effectively maintain signal integrity over the entire signal chain by isolating electrical noise arising from ground or common-mode potential differences.

With the advent of advanced digital isolators using capacitive or inductive rather than optical coupling, these engineers have been freed from the design constraints imposed by the opto-couplers. For example, the main technical advantages of a capacitively coupled isolator, such as the ISO7221 from TI, over the traditional opto-coupler are as follows:

1. Higher switching speed
2. Increased reliability and stability
3. Lower power consumption

4.2.1 Electrical

The basic electrical function of a digital isolator is to act as a filter between two subcircuits that are part of a larger electrical system. Ideally, signals (data) pass through with no distortion while noise is blocked.

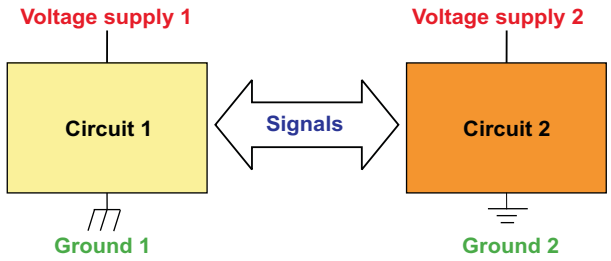


Figure 43. Digital Isolators Let Signals Pass Through Between Circuit 1 and Circuit 2

Isolators do this by allowing no electrical current to pass through while faithfully reproducing the input signal levels on the output. This galvanic isolation eliminates any noise current paths between the two subsystems that may otherwise deteriorate overall signal integrity, especially if the subsystems operate at different common-mode voltages, or ground potential differences are expected.

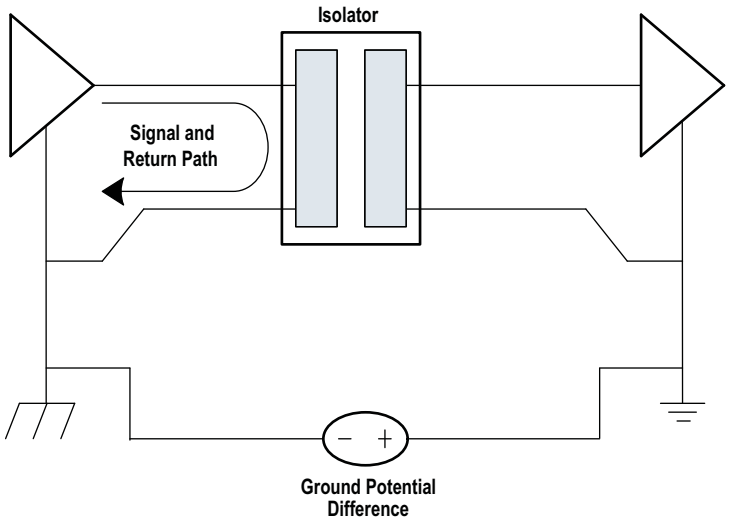


Figure 44. Isolators Break Ground Loops

Digital isolators use properties of photons (optical), capacitors, or inductors to achieve this.

Opto-couplers convert electrical energy from the input signal to photons generated by the input LED. These photons are transmitted through an optically transparent but electrically insulating material such as epoxy to the output stage that converts it back to electrical energy through the output photosensitive diode.

Capacitively coupled isolators can be explained intuitively by thinking about electrical current as water flowing in a pipe. A capacitor acts as a diaphragm across the pipe, which builds up pressure, but no steady-state current is passed through. However, an increase or decrease in water flow can be communicated across to the other side. Transitions in the input signal can thus be effectively coupled across the capacitor but with no current flow.

Inductively coupled isolators use the transformer principle – the changes in magnetic field created by the input signal transitions (primary coil) induces a voltage in the output (secondary) coil without any transfer of current.

In all cases, the input and output circuits are constructed on discrete silicon substrates separated by a dielectric of sufficient breakdown strength.

4.2.2 Applicability

Digital isolators potentially can be used in almost any electrical system where ground and/or noise isolation is needed or where protection from high voltages is desired. They are used extensively in applications ranging from industrial process control and factory automation to medical sensing and biometric data acquisition. Digital isolators are also used in consumer electronics such as plasma TVs where sensitive electronic components are electrically isolated from the high-voltage subsystem that sustains the plasma inside the plasma screen.

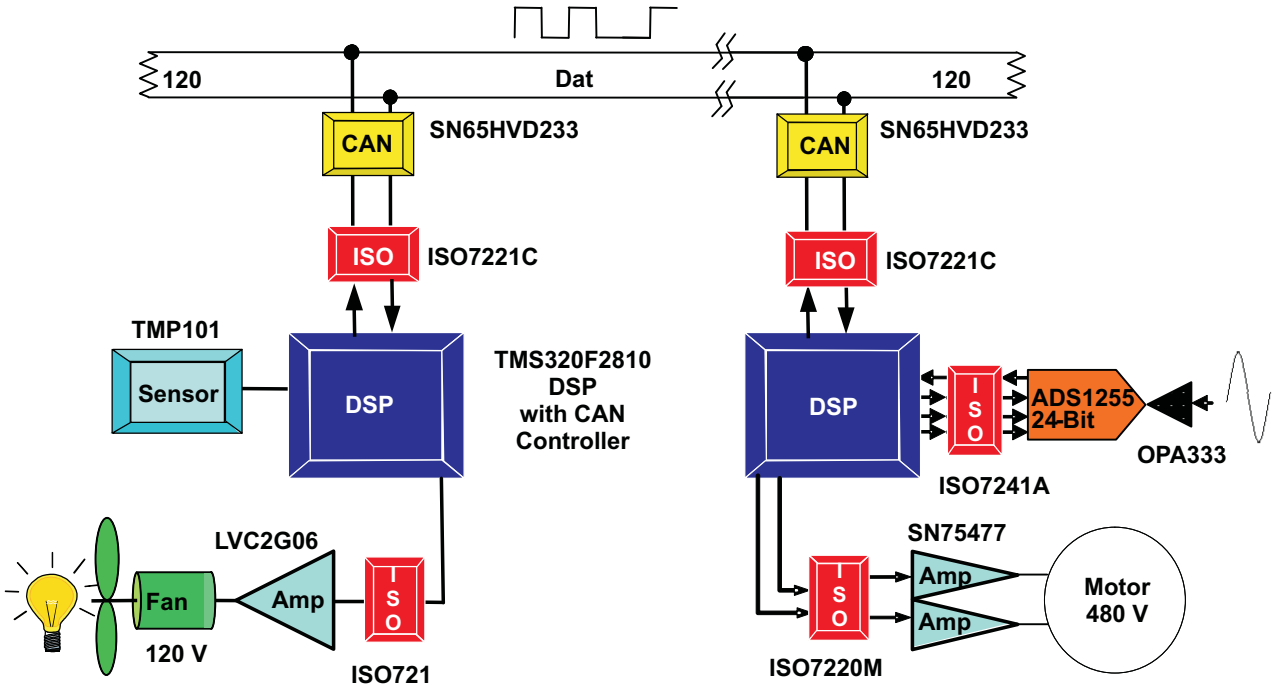


Figure 45. A Typical Industrial FieldBus Application Using Digital Isolators

4.2.3 Features

Isolation Voltage Ratings:

Momentary Withstand Voltage: This is the maximum amount of voltage that the dielectric can sustain safely for short times (de facto standard measure of time is 60 seconds) without breaking down and becoming conductive.

Continuous (Operating) Voltage: Maximum amount of voltage that can be continuously applied for the rated lifetime of the component. This is significantly lower than the momentary withstand voltage.

Creepage: Shortest distance between two conductive leads, across isolation barrier, measured along surface of insulation.

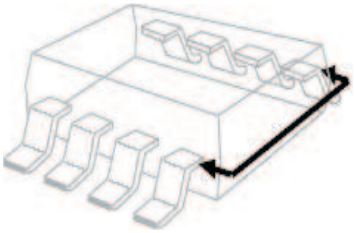


Figure 46. Measuring the Creepage Distance for a Typical Digital Isolator IC

Clearance Distances: Shortest distance between two conductive leads, across isolation barrier, measured through air (line of sight).

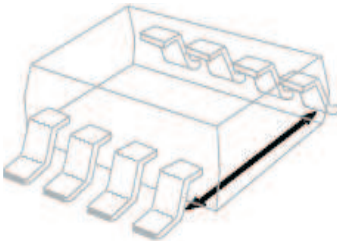


Figure 47. Figure 48. Measuring the Clearance Distance for a Typical Digital Isolator IC

Data Rate (or Input Pulse Width): Maximum input data rate in Mbps to ensure specified performance. Also can be stated as the minimum input pulse width in ns (or a measure of time)

Propagation Delay: See definitions in section 4.1 (CDC).

Pulse Width Distortion (Pulse Skew): The difference between the output and input pulse widths. Can be measured as the difference between the propagation delay from low- to-high transition (tpHL) and the high-to-low transition (tpLH)

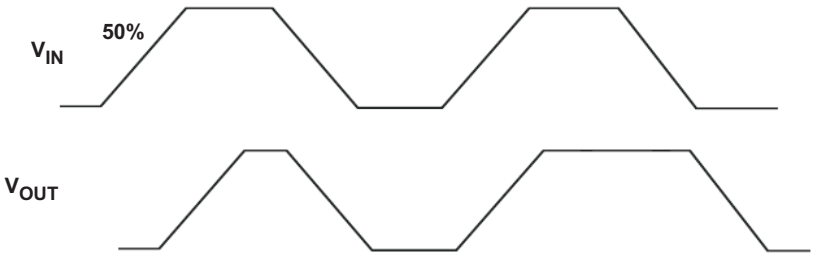


Figure 48. Pulse-Width Distortion

Output skew: See definitions in section 4.1 (CDC).

Part to part skew: See definitions in section 4.1 (CDC).

Common-Mode Transient Immunity: Maximum slew rate of ground potential shift between the input and output grounds to maintain signal integrity and/or continued device operability.

Supply Current: The amount of current drawn from the supply to operate the digital isolator. This is an indication of the power consumption and resulting heat dissipation.

Table 49. Device List – Isolation Products

DEVICE	DESCRIPTION	PACKAGE	STATUS
ISO721/ ISO722 ISO7220/ 7221	Single/dual-channel digital signal isolators, DC to 150 Mbps	8-pin SOIC	Available
ISO7230/ ISO7240 ISO7231/ ISO7241 ISO7242	Triple/quad-channel digital signal isolators, DC to 150 Mbps	16-pin SOIC (wide)	Available
AMC1203	1-bit, 10-MHz, second-order, isolated delta-sigma modulator	8-pin SOP (Gull Wing)	Available
ISO15/ ISO35 ISO3080/ ISO3082 ISO3086/ ISO3088	Isolated RS-485 transceivers. 3.3-V or 5-V, half- or full-duplex options	16-pin SOIC (wide)	Available
ISO1176	Isolated ProfiBus transceiver	16-pin SOIC (wide)	Available

5 Summary

This *Comparing Bus Solutions* application report shows that Texas Instruments provides a vast portfolio of data transmission products covering most of the commonly used communication standards. The offering ranges from typical backplane logic families like ABT, LVT, and GTLP to more advanced serial transmission families like LVDS and IEEE1394, while still providing solutions for the mature TIA (nee RS) standards such as 232 and 485.

Altogether, this shows that Texas Instruments is committed to maintaining a leadership position in the field of data transmission, and TI will continue to increase the range of advanced products available to engineers.

6 References

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2. Digital Visual Interface Revision 1.0
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4. EIA/JESD8-8, Stub Series Terminated Logic for 3.3 V (SSTL_3)
5. EIA/JESD8-9, Stub Series Terminated Logic for 2.5 V (SSTL_2)
6. EIA/TIA-232-E, ITU-T V.28
7. EIA/TIA-422-B, ITU-T V.11: Electrical characteristics for balanced double–current interchange circuits operating at data signaling rates up to 10 Mbps
8. EIA/TIA-485, ISO/IEC 8482: Information Technology – Telecommunications and information exchange between systems – Twisted pair multi–point interconnections
9. GMII Gigabit Media Independent Interface
10. High-bandwidth Digital Content Protection System Revision 1.0
11. IEEE P896.1, Futurebus+ Logic Layer Specifications
12. IEEE P896.2, Futurebus+ Physical Layer and Profile Specifications
13. IEEE1394-1995, High Performance Serial Bus
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15. ISO/IEC 9316, Information Technology, Small Computer System Interface-2
16. TIA/EIA-644, Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits
17. TIA/EIA-899, Electrical Characteristics of Multipoint-Low-Voltage-Differential Signaling (M-LVDS) Interface Circuits for Multipoint Data InterchangeEIA/JESD8-A, Interface Standard for Nominal 3-V/3.3-V Supply Digital Integrated Circuits
18. USB Universal Serial Bus Specification Revision 1.1 (Compaq, Intel, Microsoft, NEC)

7 Glossary

ABT	Advanced BiCMOS technology, 5-V logic family with TTL-compatible input and output specification
ABTE	Enhanced transceiver logic. 5-V logic with reduced noise margins to achieve higher speeds on the backplane, TTL-compatible
Arbitration	The process by which nodes compete for ownership of the bus. The cable environment uses a hierarchical point-to-point algorithm, whereas the backplane environment uses the bit–serial process of transmitting an arbitration sequence. At the completion of an arbitration contest, only one node is able to transmit a data packet.
BPS	Bits per second
BTL	Backplane transceiver logic. Typical applications are parallel backplanes
CAN	Controller area network, a Field Bus Standard (ISO 11898), intended for industrial and automotive applications.
CDC	Clock distribution circuit
DDR SDRAM	Double data rate synchronous dynamic random access memory
Downstream	The direction of data flow from the host or away from the host. A downstream port is the port on a hub electrically farthest from the host that generates downstream data traffic from the hub. Downstream ports receive upstream data traffic.
DVI	Digital visual interface
EMI	Electromagnetic interference
Endpoint	An endpoint that is capable of consuming an isochronous data stream that is sent by the host.
GTL	Gunning transceiver logic. GTL+ and GTLP are derivatives of GTL that operate at enhanced noise margin signal levels (V_{TT} = 1.5 V, V_{REF} = 1 V and V_{OL} = 0.55 V). GTLP is normally associated with optimized edge rate devices that allow high-frequency operation in heavily loaded backplane applications.
HDCP	High-bandwidth digital content protection
Hub	A USB device that provides additional connections to the USB. Typical applications are parallel backplanes
HVD	High-voltage differential
Isochronous	The term isochronous indicates the essential characteristic of a time scale or a signal such that the time intervals between consecutive significant instances either have the same duration or multiples of the shortest duration.
Life Insertion/ Removal	The ability to attach and remove devices while the system is in operation.
LIN	Local interconnect network
Link layer	The layer, in a stack of three protocol layers defined for the serial bus, that provides the service to the transaction layer of one-way data transfer with confirmation of reception. The link layer also provides addressing, data checking, and data framing. It also provides an isochronous data transfer service directly to the application.
LVD	Low-voltage differential
LVDM	Low-voltage differential signaling for multipoint applications
LVDS	Low-voltage differential signaling as defined in TIA/EIA-644-A
LVTTL	Low-voltage transistor-transistor logic
M-LVDS	Multipoint – low-voltage differential signaling, TIA/EIA-899, adding multipoint capabilities to LVDS-like signaling
Mode	An addressable device attached to the serial bus with at least the minimum set of control registers. Changing the control registers on one node does not affect the state of control registers on another node.

NRZI	Nonreturn to zero invert. A method of encoding serial data in which ones and zeroes are represented by opposite and alternating high and low voltages where there is no return to zero (reference) voltage between encoded bits and eliminates the need for clock pulses.
Packet (1394)	A serial stream of clocked data bits. A packet is normally the PDU for the link layer, although the cable physical layer can also generate and receive special short packets for management purposes.
Packet (USB)	A bundle of data organized in a group for transmission. Packets typically contain three elements: control information (e.g., source, destination, and length), the data to be transferred, and error detection and correction bits.
Physical layer	The layer, in a stack of three protocol layers defined for the serial bus, which translates the logical symbols used by the link layer into electrical signals on the different serial bus media. The physical layer ensures that only one node at a time is sending data and defines the mechanical interface for the serial bus. A different physical layer exists for the backplane and for the cable environment.
Pipe	A logical abstraction representing the association between an endpoint on a device and software on the host. A pipe has several attributes; for example, a pipe can transfer data as streams (stream pipe) or messages (message pipe).
PLL	Phase-locked loop: The PLL circuits is a feedback circuit. The purpose of this circuit is to minimize phase error between the input signal and the output signal of the PLL. In the locked state, the PLL regulates continuously the phase between the fin and fout, such a defined phase difference between both frequencies is maintained.
Port	A physical layer entity in a node that connects to either a cable or backplane and provides one end of a physical connection with another node.
Quadlet	Four bytes of data
SCSI	Small computer systems interface
SSTL	Series stub termination logic
Stubs	Short traces, branching from the backplane. Often found on memory modules.
Termination resistor	The termination resistor is used at the end of a line in order to avoid reflections of the transmitted signal. If the termination resistor is chosen equally to the line impedance the line is optimally terminated.
TMDS	Transition minimized differential signaling
Transaction	The delivery of service to an endpoint; consists of a token packet, optional data packet, and optional handshake packet. Specific packets are allowed/required based on the transaction type.
Transfer	One of the four USB transfer types. Isochronous transfers are used when working with isochronous data. Isochronous transfers provide periodic, continuous communication between host and device.
Upstream	The direction of data flow towards the host. An upstream port is the port on a device electrically closest to the host that generates upstream data traffic from the hub. Upstream ports receive downstream data traffic.
USB	Universal serial bus

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from B Revision (October 2009) to C Revision	Page
• Added *FPD-Link III* section	62

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