User's Guide

SLLU204–June 2014

SN65DSI86/SN65DSI96 EVM User's Manual

This guide describes how to use and configure the SN65DSI86 or SN65DSI96 EVM, with recommendations for system hardware implementation. These recommendations are only guidelines; the designer is responsible for all system characteristics and requirements. Refer to the datasheet for technical details such as device operation and terminal description.

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1 Overview

1.1 *What are SN65DSI86 and SN65DSI96?*

The SN65DSI86 and SN65DSI96 devices are referred to as SN65DSIX6 in this document. SN65DSIX6 is a MIPI DSI to eDP bridge device that supports video modes in forward direction. The SN65DSIX6 targets portable applications such as tablets and smart phones that utilize the MIPI DSI video format. The SN65DSIX6 can be used between a GPU with DSI output and a video panel with DisplayPort inputs.

Both devices share the same pin out and package.

Table 1 is a summary of the feature sets on these devices:

Table 1. SN65DSIX6 Features Summary

Part Name	Description
SN65DSI86	Dual channel DSI to 4 eDP lanes
SN65DSI96	Dual channel DSI to 4 eDP lane with adaptive display technology

1.2 *What is the SN65DSIX6 EVM?*

The SN65DSIX6 EVM is a PCB created to help customers evaluate the SN65DSIX6 device for video applications with the DSI and DisplayPort interface. This EVM can also be used as a hardware reference design for any implementation of the SN65DSIX6. The SN65DSIX6 EVM is designed for both the SN65DSI86 and SN65DSI96 DSI bridge devices.

NOTE: **Note**: Some portions and components in the EVM or in this document may include the references to SN65DSI86 instead of addressing both part numbers. For the purposes of this document, the SN65DSI86 is interchangeable with the SN65DSI96.

PCB design and layout files are provided upon request to aid the PCB design with a SN65DSIX6 component. The layout files are a guideline for implementing the SN65DSIX6, with illustrations of the routing and placement rules. The EVM design includes test components to evaluate the SN65DSIX6 which may not applicable for production.

1.3 *What is Included in the SN65DSIX6 EVM?*

The major components of the EVM are:

- SN65DSI86ZQE or SN65DSI96ZQE
- Samtec QSH type connectors on DSI and eDP interfaces
- Standard DisplayPort connector
- Hirose type connector on DSI Ch A interface
- I2C programming interface for an external I2C host connection

1.4 What does the EVM look like?

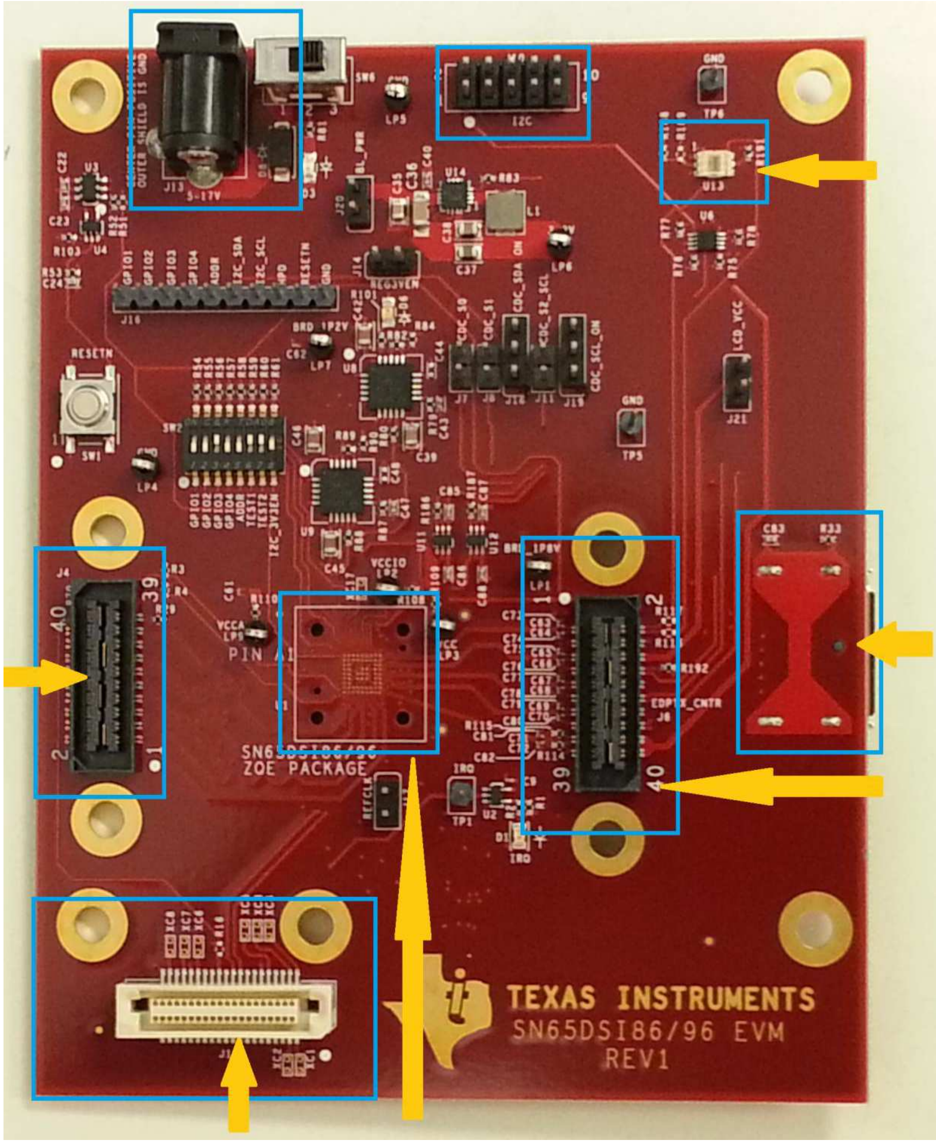

Figure 1. SN65DSIX6EVM Rev1 or Rev2

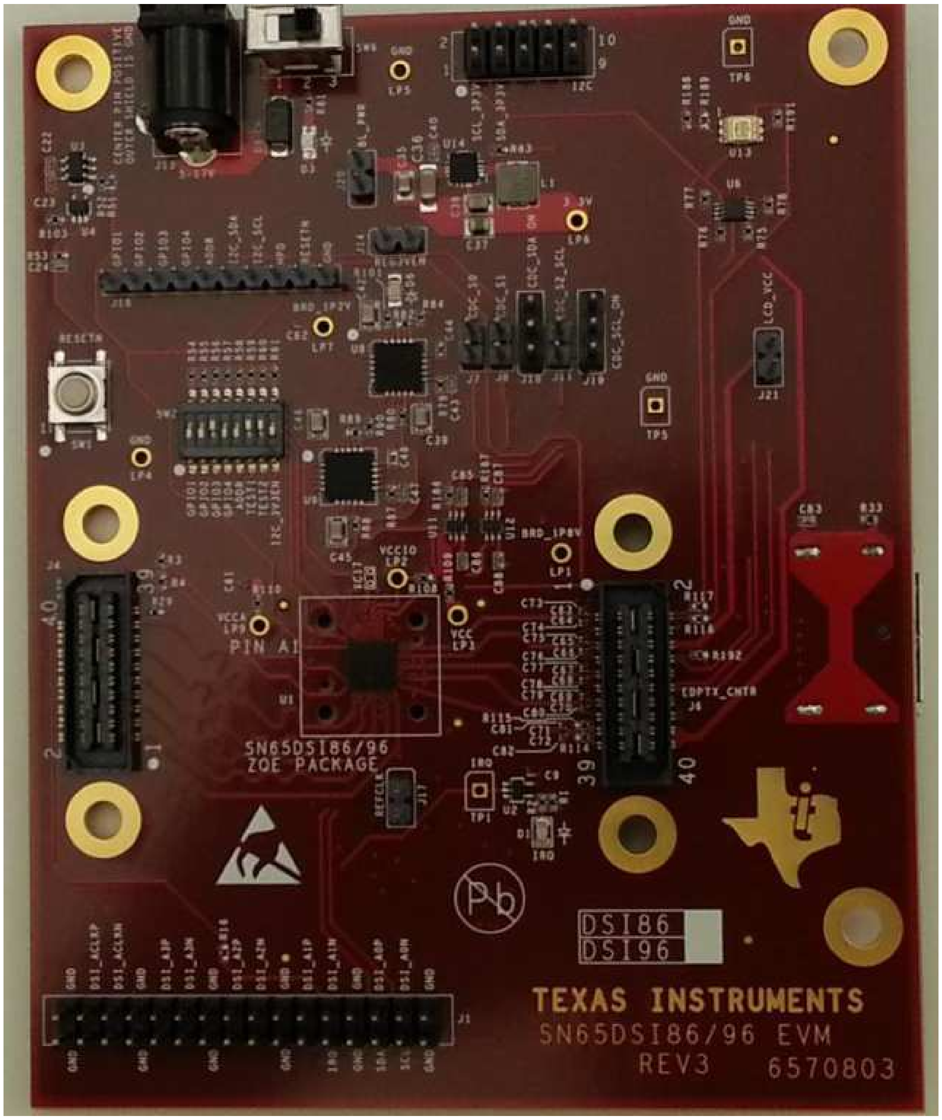

Figure 2. SN65DSI8X EVM Rev 3

2 Hardware Description

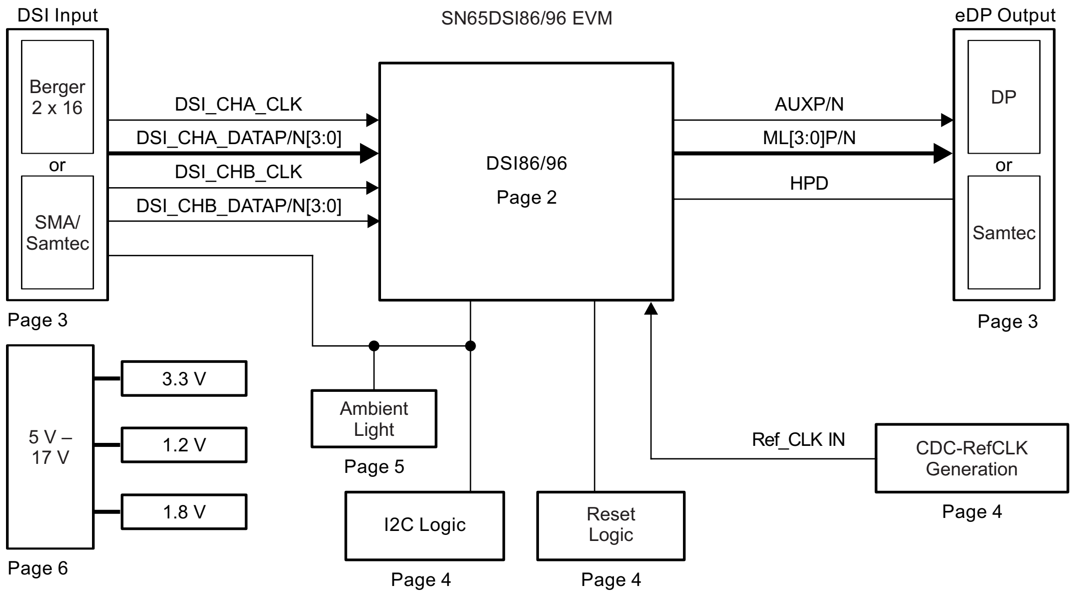

Figure 3. SN65DSIX6 EVM Block Diagram

2.1 Connectors for DSIX6 Input Ports

The EVM has two input options for DSI video. If designing a custom breakout board using these options, a schematic and an allegro PCB symbol for either connector can be provided by TI upon request.

2.1.1 J4 - Samtec QSH Type Connector (P/N QSH-020-01-H-D-DP-A)

J4 is a Samtec QSH-type connector that can be mated with a matching QTH type connector on the top. The J4 provides DSI input connections to both DSI Ch A and Ch B signals, and access to I2C and other miscellaneous signals such as IRQ. XC connections are open vias if a connection to other signals is required. The mating connector part number is QTH-020-01-H-D-DP-A. For an SMA type connection, a HDR-128291-XX breakout board from Samtec can be used. The HDR-128291-XX is a breakout board with a mating connector to J4 and standard SMA male connectors via cables. More info on this breakout board can be provided upon request.

Note: Resistors R6 thru R15 should be unpopulated when using this connector. Failure to remove these resistors will result in signal integrity issues. These resistors are located on the bottom of PCB underneath J4.

Table 2. J4 Pin-out

Pin#	Name	Pin#	Name
1	DSI_A3P	2	DSI_B3P
3	DSI_A3N	4	DSI_B3N
5	GND	6	GND
7	GND	8	GND
9	DSI_A2P	10	DSI_B2P
11	DSI_A2N	12	DSI_B2N
13	GND	14	GND
15	GND	16	GND
17	DSI_ACLKP	18	DSI_BCLKP
19	DSI_ACLKN	20	DSI_BCLKN
21	GND	22	GND

Table 2. J4 Pin-out (continued)

Pin#	Name	Pin#	Name
23	GND	24	GND
25	DSI_A1P	26	DSI_B1P
27	DSI_A1N	28	DSI_B1N
29	GND	30	GND
31	GND	32	GND
33	DSI_A0P	34	DSI_B0P
35	DSI_A0N	36	DSI_B0N
37	RESETN	38	IRQ
39	I2C_SDA	40	I2C_SCL

2.1.2 J1 – Hirose FX Type Connector (P/N FX6A-40S-0.8SV2)

J1 is a Hirose FX-type connector that can be mated with a matching FX plug on the top. The part number for the mating connector is FX6A-40P-0.8SV2. J1 provides a DSI input connection only to the DSI Ch A signals. J1 also provides access to I2C and other miscellaneous signals such as IRQ. This connector is only available in Revision 1 and 2 of the EVM.

Table 3. J1 Pin-out

Pin#	Name	Pin#	Name
1	NC	2	NC
3	NC	4	NC
5	NC	6	NC
7	NC	8	NC
9	GND	10	NC
11	DSI_ACLKP	12	GND
13	DSI_ACLKN	14	NC
15	GND	16	NC
17	DSI_A0P	18	I2C_SCL
19	DSI_A0N	20	I2C_SDA
21	GND	22	GND
23	DSI_A1P	24	IRQ
25	DSI_A1N	26	NC
27	GND	28	NC
29	DSI_A2P	30	NC
31	DSI_A2N	32	GND
33	GND	34	NC
35	DSI_A3P	36	NC
37	DSI_A3N	38	NC
39	GND	40	GND

2.1.3 J1 – 100-mil Male Header

J1 is a 2x16 100-mil male header. J1 provides DSI input connection only to the DSI Ch A signals. J1 also provides access to I2C and other miscellaneous signals such as IRQ. This connector is only available in Revision 3 of the EVM.

Table 4. J1 Pin-out

Pin#	Name	Pin#	Name
1	GND	2	GND
3	DSI_A0N	4	I2C_SCL
5	DSI_A0P	6	I2C_SDA
7	GND	8	GND
9	DSI_A1N	10	IRQ
11	DSI_A1P	12	NC
13	GND	14	GND
15	DSI_A2N	16	NC
17	DSI_A2P	18	NC
19	GND	20	GND
21	DSI_A3N	22	NC
23	DSI_A3P	24	NC
25	GND	26	GND
27	DSI_ACLKN	28	NC
29	DSI_ACLKP	30	NC
31	GND	32	GND

2.2 Connectors for DSIX6 Output Ports

There are two output port options available on the EVM for the DisplayPort output signals. By default, the DisplayPort interface signals from the SN65DSIX6 are connected to the J9 connector. To use the J6, follow these capacitor select options:

Table 5. J6 and J9 Selection Options

	Component Install Requirement
J6	C63, C64, C65, C66, C67, C68, C69, C70, C71, C72
J9 (Default)	C73, C74, C75, C76, C77, C78, C79, C80, C81, C82

2.2.1 J9 – Standard DisplayPort Male Connectors (Molex P/N 47272-0001)

J9 is a standard DisplayPort male connector widely used in notebooks and desktops for interfacing to external DisplayPort capable monitors. DisplayPort cables for connecting to this connector and a external monitor can be obtained from a third party source.

2.2.2 J6 - Samtec QSH type Connector (P/N QSH-020-01-H-D-DP-A)

J6 is a Samtec QSH-type connector that can be mated with a matching QTH-type connector on the top. The J6 provides DSI input connections to DisplayPort signals and accesses the back light power and its related signals. XC connections are open vias if a connection to other signals is required. The mating connector part number is QTH-020-01-H-D-DP-A. For an SMA-type connection, a HDR-128291-XX breakout board from Samtec can be used. The HDR-128291-XX is a breakout board with a mating connector to J6 and standard SMA male connectors via cables. More info on this breakout board can be obtained from the Samtec website.

Table 6. J6 Pin-out

Pin#	Name	Pin#	Name
1	ML3N	2	I2C_SDL (LVCMOS 3.3V Level)
3	ML3P	4	I2C_SDA (LVCMOS 3.3V Level)
5	GND	6	GND

Table 6. J6 Pin-out (continued)

Pin#	Name	Pin#	Name
7	GND	8	GND
9	ML2N	10	LCD_VCC
11	ML2P	12	LCD_VCC
13	GND	14	EDP SELF TEST
15	GND	16	HPD
17	ML1N	18	NC
19	ML1P	20	NC
21	GND	22	BL_ENABLE
23	GND	24	PWM_DIM
25	ML0N	26	NC
27	ML0P	28	NC
29	GND	30	GND
31	GND	32	GND
33	AUXP	34	BL_PWR
35	AUXN	36	BL_PWR
37	GND	38	BL_PWR
39	GND	40	BL_PWR

2.2.2.1 J6 Daughterboards

There are two daughterboards for connecting to eDP panels: DSI86 EDP_30PIN and DSI86 EDP_40PIN. These boards are not provided with the SN65DSI86/96 EVM board, but are available upon request.

2.2.2.1.1 DSI86 EDP_30PIN

The DSI86 EDP_30PIN daughterboard supports up to 2 eDP lanes. This board is intended to mate to an eDP panel that has a pin-out that matches Table 6-3 in the VESA Embedded DisplayPort Standard Version 1.3. This board has a Samtec QTH-020-01-H-D-DP-A for mating to J6 on the SN65DSI86/96 EVM board and an IPEX receptacle (part# 20455-030E-02) for interfacing to an eDP panel. The ribbon cable for connecting the eDP panel to this daughterboard should use a IPEX plug (part# 20453-030T-11S) or equivalent.

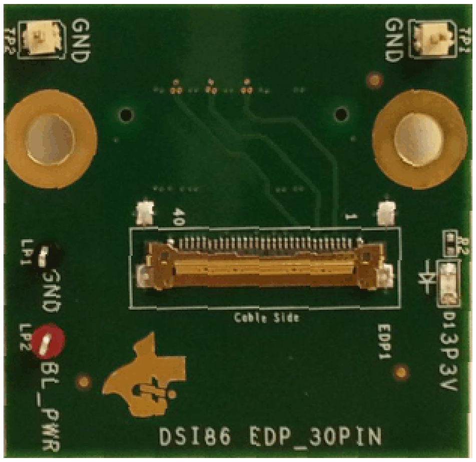

Figure 4. DSI86 EDP_30PIN

2.2.2.1.2 DSI86 EDP_40PIN

The DSI86 EDP_40PIN daughterboard supports up to 4 eDP lanes. This board is intended to mate to an eDP panel that has a pin-out that matches Table 6-4 in the VESA Embedded DisplayPort Standard Version 1.3. This board has a Samtec QTH-020-01-H-D-DP-A for mating to J6 on the SN65DSI86/96 EVM board and an IPEX receptacle (part# 20455-040E-02) for interfacing to an eDP panel. The ribbon cable for connecting the eDP panel to this daughterboard should use a IPEX plug (part# 20453-040T-11S) or equivalent.

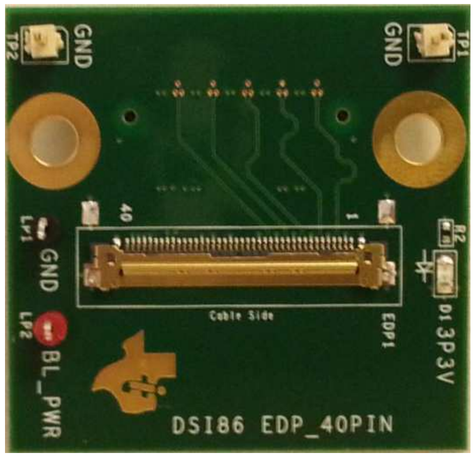

Figure 5. DSI86 EDP_40PIN

2.3 I2C

Access to I2C signals are provided via DSI input connectors J1, J4, J10, or J16. I2C signal levels should be at 1.8 V when the I2C interface is accessed through connectors J1, J4, or J16. 3.3 V to 1.8 V voltage translation is provided when an I2C host is connected through J10.

A standalone external I2C host can connect via J10 for debug purposes. An example of an external I2C host controller is the Total Phase Aardvark I2C/SPI host adapter (Total Phase Part#: TP240141). Sample scripts for this I2C Host controller are provided in Section 7.

2.4 Enable and Reset

There are three device enable and reset options for the EVM.

- **Supervisor circuitry option**: This is the default configuration. The enable (EN) signal is held low until the power good (PG) from the 1.8V voltage regulator reaches a stable high voltage level, then the EN is released high.
- **RC timing option**: The C10 external capacitor and internal resistor control the EN ramp time after the device is powered on. C10 is a DNI (Do Not Install option) by default. C10 must be installed and R52 must be uninstalled to enable this option.
- **External control option**: A push-button (SW1) or a J16 pin 9 is available for the manual control of the EN signal.

2.5 Power

The 5 V-17 V power supply can be used to operate the SN65DSIX6 EVM. A plug to accept a 5 V to 17 V wall power adapter is provided on the EVM (J13).

The EVM is designed to accommodate a maximum current of 1.5 A. The current consumption of the board without the back light driver enabled is about 75 mA + SN65DSIX6 device power. The SN65DSIX6 consumes about 23 mW at power on, and up to 320 mW depending on the system configurations. The total power consumption of the board could vary depending on the LCD panels when the on-board back light driver is used. When an LCD panel consumes more current than 1.5 A minus 75 mA + SN65DSIX6 device power, the external back light source should be used.

Important: Do not plug in any power source higher than the configured voltage (17-V).

2.6 Ambient Light Sensor

The SN65DSIX6 EVM incorporates a TAOS TSL2561T ambient light sensor. An external GPU can use this sensor with the SN65DSI96. By default, the sensor is located at the I2C slave address of 0x29 (R188 installed and R189 uninstalled). The I2C slave address can be changed to 0x49 (uninstall R188 and install R189) or 0x39 by (uninstall R188 and uninstall R189).

2.7 Reference CLK Programmability

The SN65DSIX6 EVM incorporates programmable CLK circuitry using TI-programmable device CDCEL913. The output of the CDCEL913 is connected to the reference CLK of the SN65DSIX6. The CLK can be programmed via I2C signals brought out to on-board connectors J9, J12 or J10. When J10 is used, jumpers should be placed on J9 and J12. The default frequency of the REFCLK is set to 27MHz.

2.8 DIP Switch Configuration

The DIP switch lets the user operate the device and EVM in different configurations. When the switch is in an open position, the corresponding signal is tied high. When the switch is in ON (closed) position, the corresponding signal is tied to GND.

Table 7. DIP Switch Settings

			DEFAULT CONFIG	
DIP SW No	**Signal Name**	**Description**	**Open(Off) HIGH**	**Closed(On) LOW**
SW2-1	GPIO1	General Purpose I/O. Defaults to Input. Also used to select REFCLK frequency.	X	
SW2-2	GPIO2	General Purpose I/O. Defaults to Input. Also used to select REFCLK frequency.	X	
SW2-3	GPIO3	General Purpose I/O. Defaults to Input. Also used to select REFCLK frequency.		X
SW2-4	GPIO4	General Purpose I/O. Defaults to Input. Also used to select REFCLK frequency.	X	
SW2-5	ADDR	Sets the I2C slave address of the SN65DSIX6 by controlling the ADDR pin. High = 0x2D (default) Low = 0x2C	X	
SW2-6	TEST1	Reserved. Texas Instruments use only		X
SW2-7	TEST2	Reserved. Texas Instruments use only. For DP compliance testing make dip switch position to OFF (high).		X
SW2-8	I2C_3V3EN	Enables 3.3V voltage translator for the I2C signals	X	

3 Quick Start Guide

1. Plug in a DSI source to J1 or J4. Refer to Section 2.1 for details on these connectors. All used DSI inputs should be held at LP11 state during this step.
2. Plug in a DisplayPort video sink device on J9 (Standard DisplayPort connector) or J6 (eDP breakout connector). Refer to Section 2.2 for details on these connectors.
3. Plug in an I2C host on J10 if using an external I2C host.
4. Correctly configure the DIP switch setting.
5. Apply power to the EVM. The following LEDS should light up: D3 and D6. D1 may light up depending on the configuration.
6. Configure the device for the desired mode of operation via I2C. Example Aardvark scripts are provided in Section 7.
7. Start video streaming on the DSI input.
8. Video output should be observed after the configuration is complete.

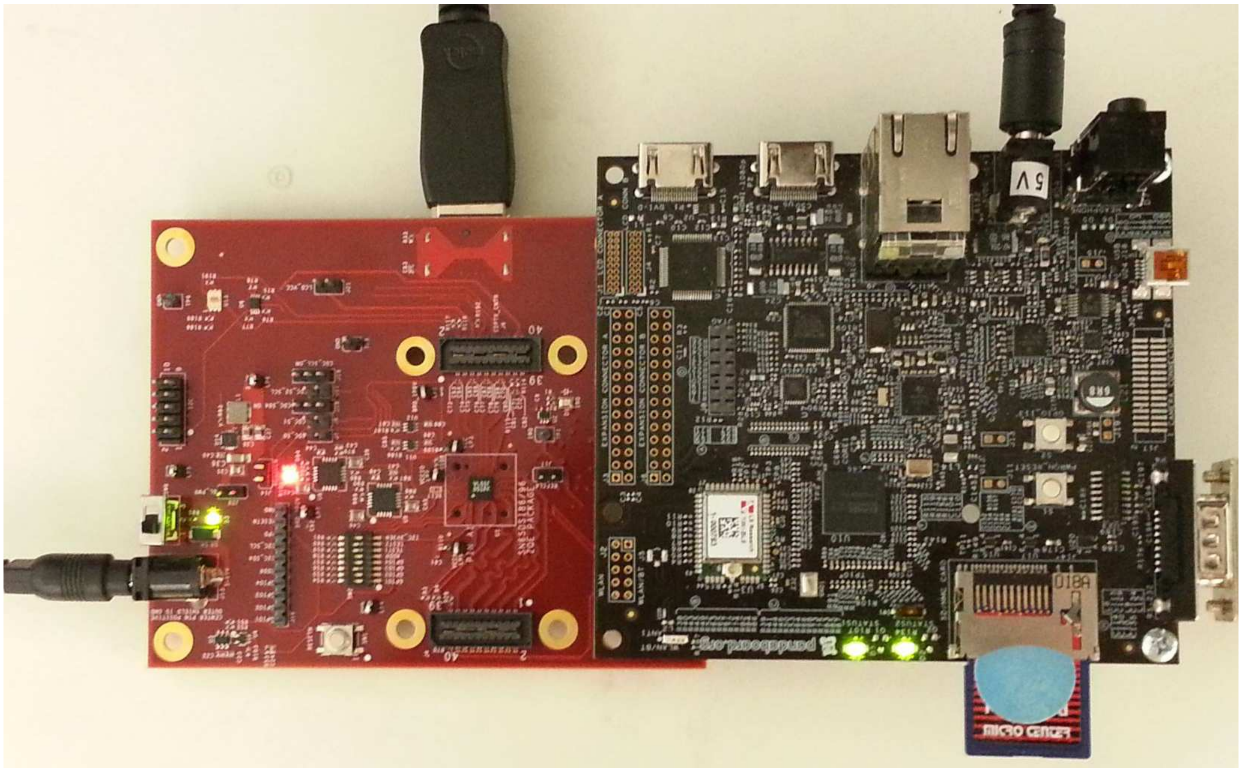

Figure 6. DSI86/96 Rev1 EVM Example Setup

4 References

SN65DSIX6 Datasheet.

5 EVM Bill of Materials

Table 8. EVM Bill of Materials

Item	Quantity	Reference	Part	Manuf	Manuf PN
1	7	C1, C38, C39, C42, C45, C46, C57	10uF		
2	5	C2, C11, C28, C83, C91	1.0uF		

Table 8. EVM Bill of Materials (continued)

Item	Quantity	Reference	Part	Manuf	Manuf PN
3	21	C3, C4, C6, C7, C9, C56, C59, C61, C62, C73, C74, C75, C76, C77, C78, C79, C80, C81, C82, C89, C90	0.1uF		
4	4	C5, C8, C58, C60	0.01uF		
5	12	C10, C63, C64, C65, C66, C67, C68, C69, C70, C71, C72, C84	DNI		
6	1	C22	220pF		
7	10	C23, C29, C30, C31, C32, C33, C85, C86, C87, C88	0.1uF		
8	1	C24	18pF		
9	5	C25, C26, C44, C48, C55	DNI		
10	2	C27, C37	22uF		
11	1	C35	10uF	Murata	GRM21BR61E106KA73L
12	1	C36	22uF	Murata	GRM31CR61E226KE15L
13	1	C40	3.3nF		
14	2	C43, C47	0.01uF		
15	1	D1	LED Orange 0805	Rohm	SML-211DTT86
16	1	D3	LED Green 0805	Arrow (Lumex)	670-1006 (SML_LX0805GC)
17	1	D6	LED RED 0805	Rohm	SML-211UT
18	1	D8	20V, 1A	Comchip	CDBA120SL-G
19	1	FB4	220 @ 100MHZ	Murata	BLM18EG221SN1D
20	1	J1	2x16 Male Header	Sullins	PBC16DAAN
21	2	J4, J6	QSH-020-01	Samtec	QSH-020-01-X-D-DP-A
22	3	J7, J8, J11	HDR2X1 M .1	AMP	103321-2
23	1	J9	Display_Port_Connector	Molex	47272-0001
24	1	J10	Header 5x2 0.1" thru-hole		
25	1	J13	2.1mm x 5.5mm	CUI STACK	PJ-202AH
26	4	J14, J17, J20, J21	HDR2X1 M .1		
27	1	J16	HEADER 1x10		
28	2	J18, J19	HDR3X1 M .1		
29	8	LP1, LP2, LP3, LP4, LP5, LP6, LP7, LP9	LP	KOBIKONN	151-103-RC
30	1	L1	2.2uH	Vishay	IHLP1616ABER2R2M11
31	2	R1, R53	1K		
32	2	R1, R53	350		
33	16	R3, R4, R54, R55, R56, R57, R58, R59, R60, R61, R77, R78, R79, R87, R188, R191	4.7K		

Table 8. EVM Bill of Materials (continued)

Item	Quantity	Reference	Part	Manuf	Manuf PN
34	1	R5	10nF		
35	11	R6, R7, R8 ,R9, R10, R11, R12, R13, R14, R15, R70	0		
36	7	R16, R51, R66, R112, R116, R117, R189	DNI		
37	5	R27, R83, R113, R114, R115	100K		
38	14	R29, R52, R75, R76, R80, R88, R104, R108, R109, R110, R111, R118, R186, R187	0		
39	2	R33, R36	1M		
40	1	R67	18		
41	5	R72, R73, R74, R86, R103	10K		
42	1	R81	500		
43	1	R82	2.49K		
44	1	R84	4.99K		
45	1	R89	3.57K		
46	1	R90	2.87K		
47	1	R105	DNI		
48	1	R192	4k		
49	1	SW1	PB_SWITCH	OMRON	B3SN-3012P
50	1	SW2	8-POS 50-MIL SMT	C&K(ITT-CANNON)	TDA08H0SK1R
51	1	SW6	TS01CQE	C&K Div.	TS01CQE
52	3	TP1, TP5, TP6	T POINT S		
53	1	U1	SN65DSI86	TI	SN65DSI86ZQER
54	1	U2	SN74LVC1G07DCK	TI	SN74LVC1G07DCK
55	1	U3	TPS3808	TI	TPS3808g18DBVT
56	1	U4	SN74LVC1G08DCK	TI	SN74LVC1G08DCK
57	1	U5	CDCEL913PW	TI	CDCEL913PW
58	1	U6	TXS0102DCUT	TI	TXS0102DCUT
59	2	U8, U9	TPS74201RGWT	TI	TPS74401RGWT
60	2	U11, U12	SN74AVC1T45DCKR	TI	SN74AVC1T45DCKR
61	1	U13	TSL2561T	TAOS	TSL2561T
62	1	U14	TPS62142RGTR	TI	TPS62142RGTR
63	1	Y1	27MHZ _crystal	ABRACON	ABM8-27.000MHZ-10-1-U-T

6 EVM Schematics

The following pages contain schematics for the SN65DSI86/96 EVM.

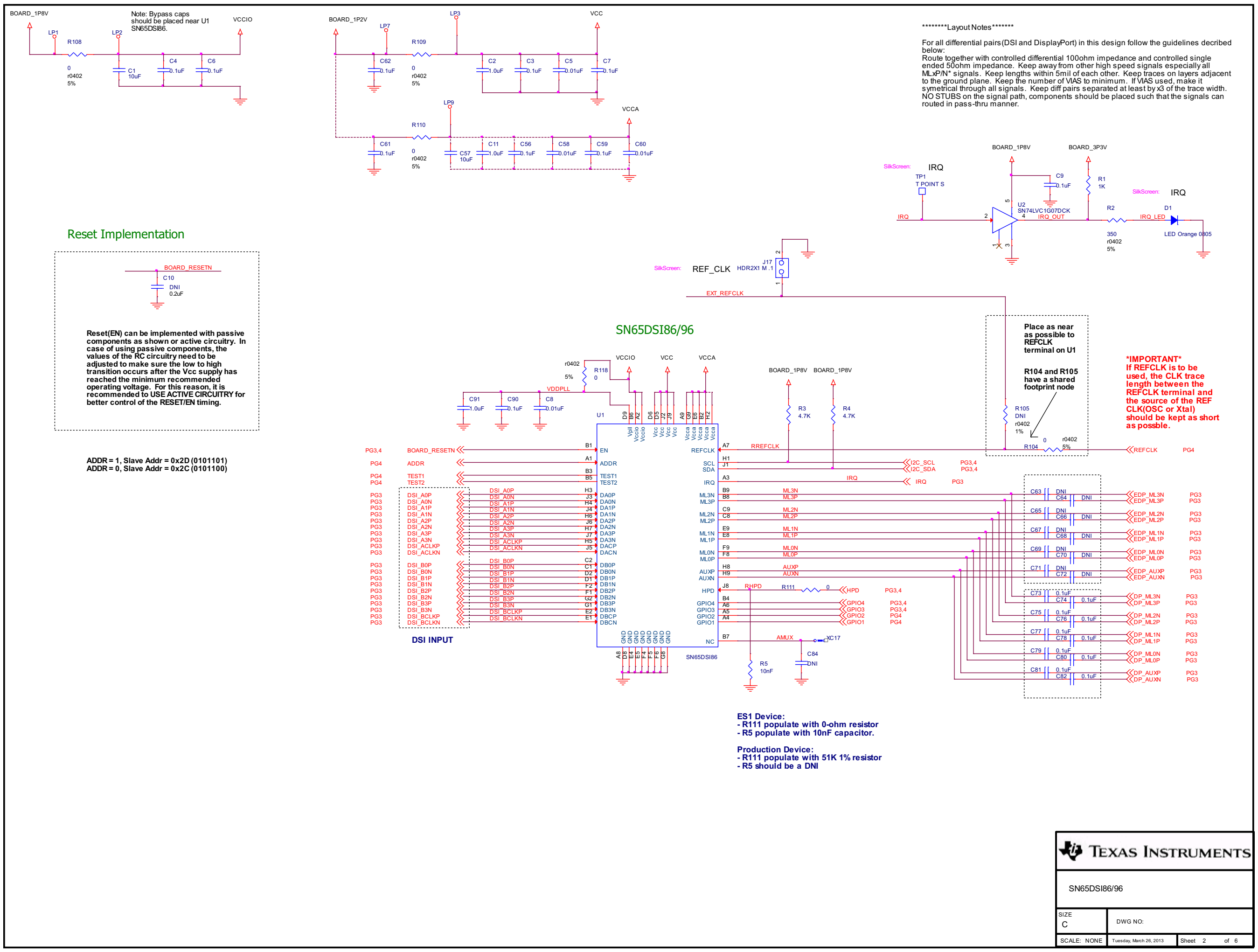

Figure 7. SN65DSI86/96 EVM

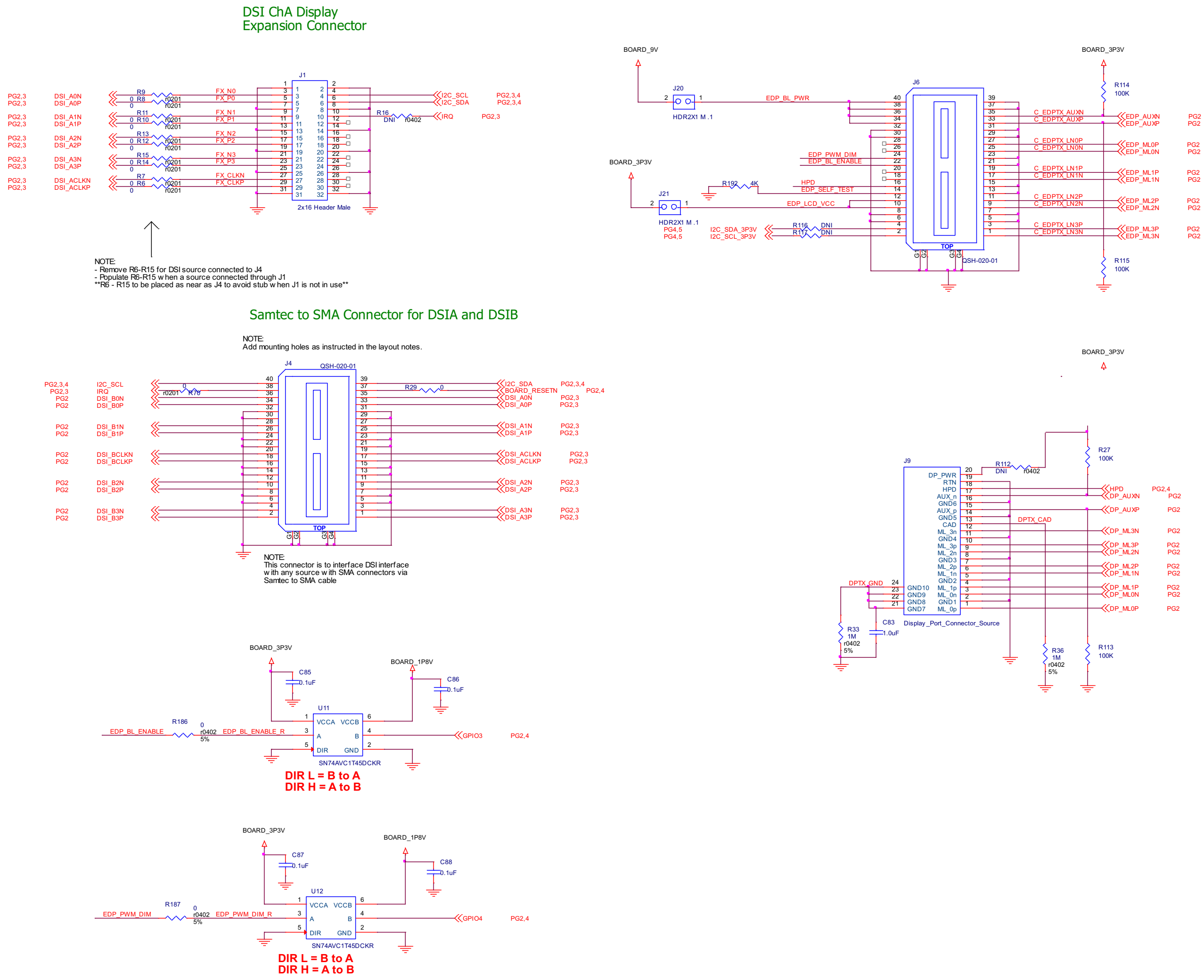

Figure 8. SN65DSI86/96 EVM

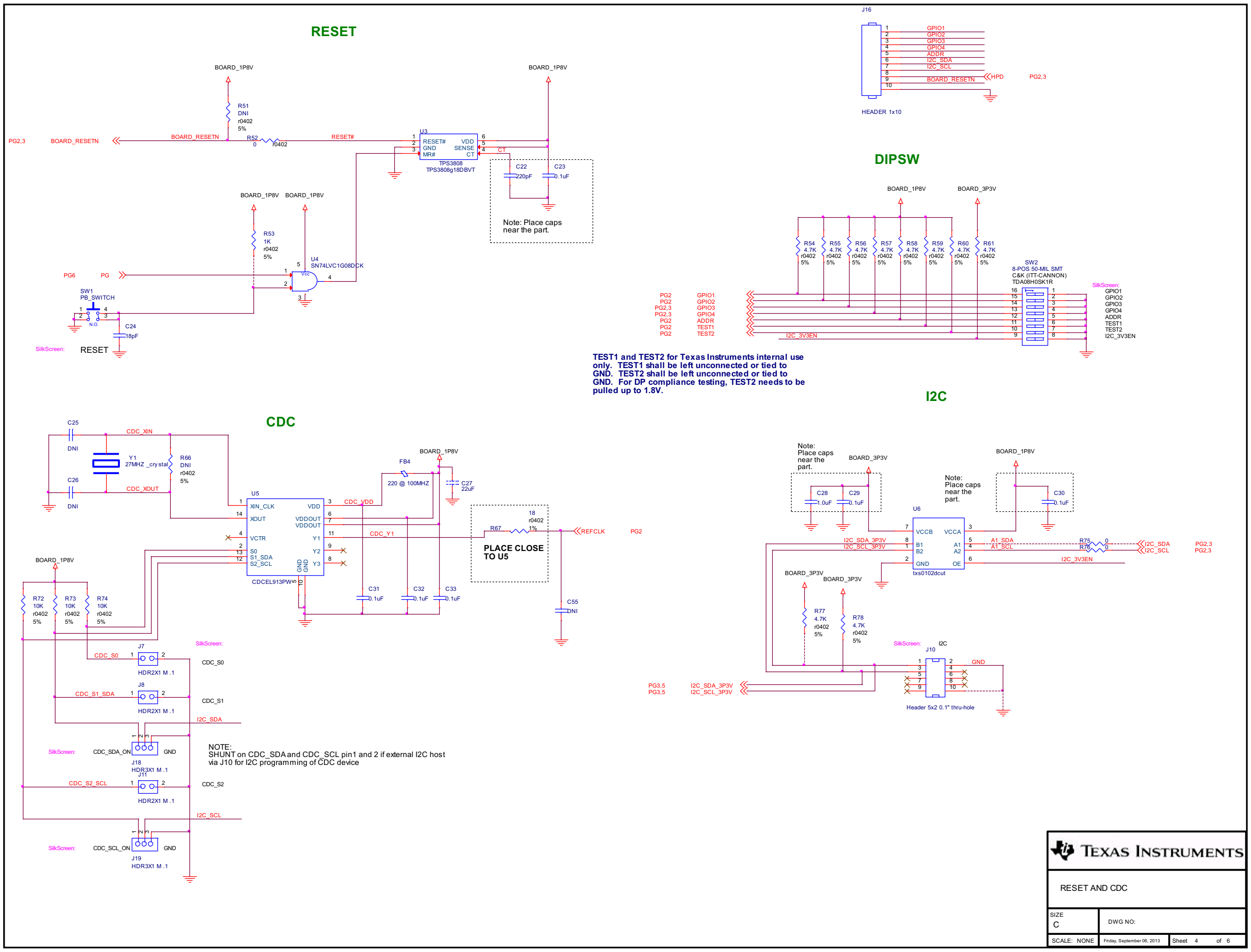

Figure 9. SN65DSI86/96 EVM

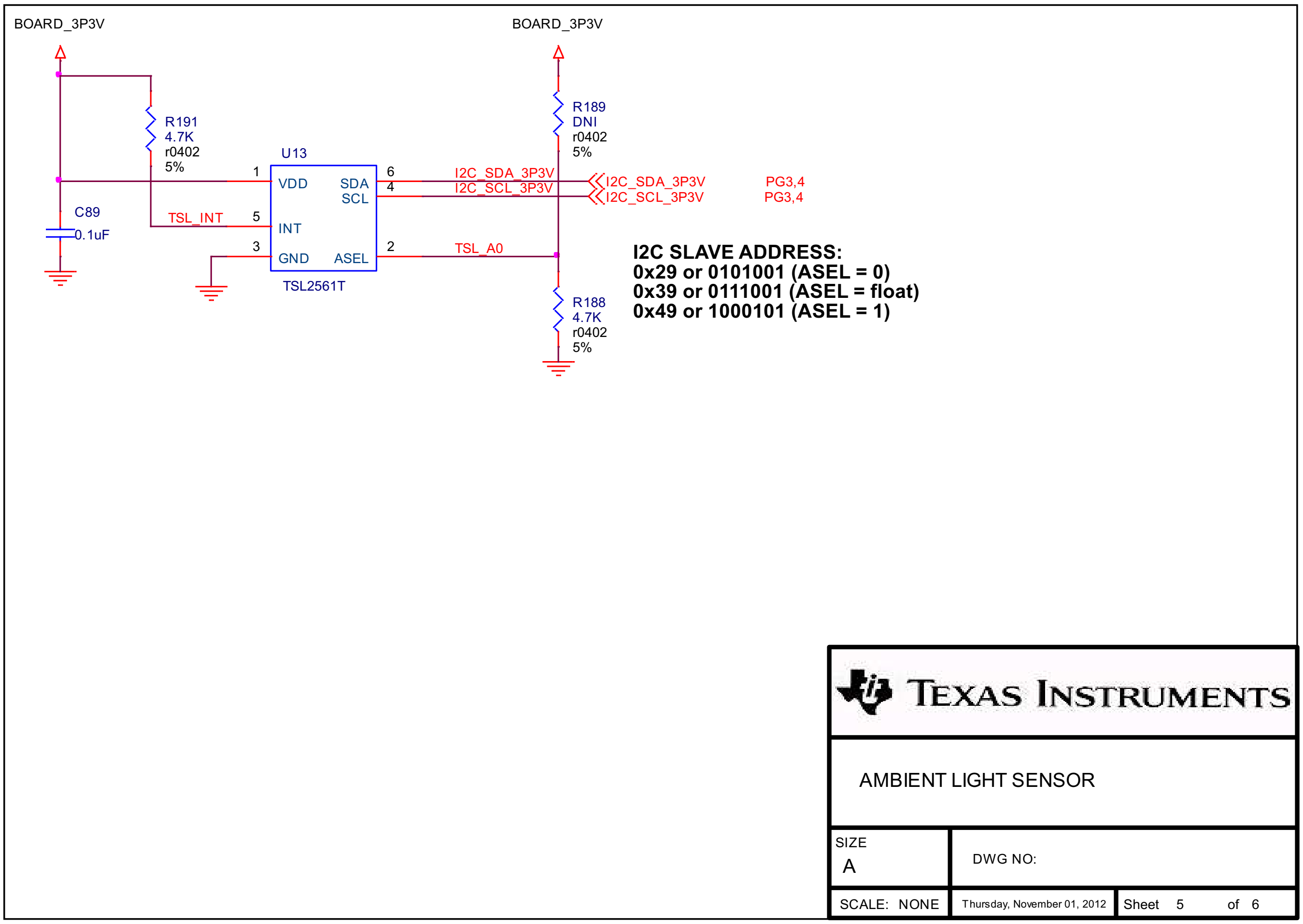

Figure 10. SN65DSI86/96 EVM

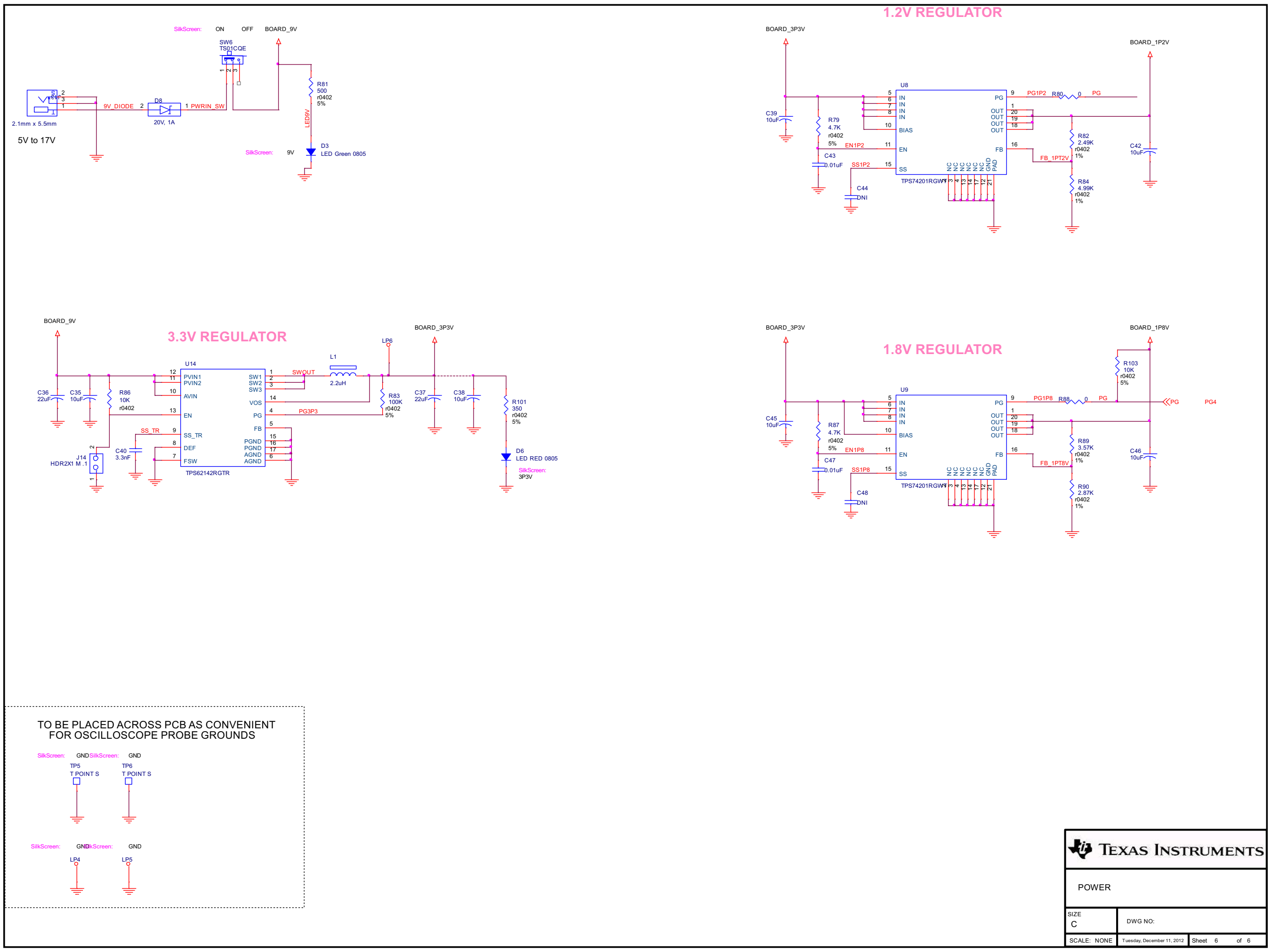

Figure 11. SN65DSI86/96 EVM

7 Sample Total Phase Aardvark I2C Host Adapter Scripts

7.1 1920x1080 @60Hz 24bpp – DSI A Channel Only and 2 DP at HBR

<aardvark>

<configure i2c="1" spi="1" gpio="0" tpower="1" pullups="0" />

<i2c_bitrate khz="100" />

======Single 4 DSI lanes======

<i2c_write addr="0x2D" count="1" radix="16">10 26</i2c_write>

<sleep ms="10" />

======enhanced framing======

<i2c_write addr="0x2D" count="1" radix="16">5A 04</i2c_write>

<sleep ms="10" />

======Pre0dB 2 lanes no SSC======

<i2c_write addr="0x2D" count="1" radix="16">93 20</i2c_write>

```
<sleep ms="10" />
======L0mV HBR======
<i2c_write addr="0x2D" count="1" radix="16">94 80</i2c_write>
<sleep ms="10" />
======PLL ENABLE======
<i2c_write addr="0x2D" count="1" radix="16">0D 01</i2c_write>
<sleep ms="10" />
======POST2 0dB ======
<i2c_write addr="0x2D" count="1" radix="16">95 00</i2c_write>
<sleep ms="10" />
======Semi-Auto TRAIN ======
<i2c_write addr="0x2D" count="1" radix="16">96 0A</i2c_write>
<sleep ms="20" />
======ADDR 0x96 CFR======
<i2c_write addr="0x2D" count="0" radix="16">96</i2c_write>
<sleep ms="20" />
======Read======
<i2c_read addr="0x2D" count="1" radix="16">00</i2c_read>
<sleep ms="10" />
=====CHA_ACTIVE_LINE_LENGTH=======
<i2c_write addr="0x2D" count="2" radix="16">20 80 07</i2c_write>
<sleep ms="10" />
=====CHA_VERTICAL_DISPLAY_SIZE=======
<i2c_write addr="0x2D" count="2" radix="16">24 38 04</i2c_write>
<sleep ms="10" />
=====CHA_HSYNC_PULSE_WIDTH=======
<i2c_write addr="0x2D" count="2" radix="16">2C 10 80</i2c_write>
<sleep ms="10" />
=====CHA_VSYNC_PULSE_WIDTH=======
<i2c_write addr="0x2D" count="2" radix="16">30 0E 80</i2c_write>
<sleep ms="10" />
=====CHA_HORIZONTAL_BACK_PORCH=======
<i2c_write addr="0x2D" count="1" radix="16">34 98</i2c_write>
<sleep ms="10" />
=====CHA_VERTICAL_BACK_PORCH=======
<i2c_write addr="0x2D" count="1" radix="16">36 13</i2c_write>
<sleep ms="10" />
=====CHA_HORIZONTAL_FRONT_PORCH=======
<i2c_write addr="0x2D" count="1" radix="16">38 10</i2c_write>
```

```
<sleep ms="10" />
=====CHA_VERTICAL_FRONT_PORCH=======
<i2c_write addr="0x2D" count="1" radix="16">3A 03</i2c_write>
<sleep ms="10" />
======DP-18BPP Enable======
<i2c_write addr="0x2D" count="1" radix="16">5B 00</i2c_write>
<sleep ms="10" />
=====COLOR BAR =======
<i2c_write addr="0x2D" count="1" radix="16">3C 00</i2c_write>
<sleep ms="10" />
======enhanced framing and Vstream enable======
<i2c_write addr="0x2D" count="1" radix="16">5A 0C</i2c_write>
<sleep ms="10" />
</aardvark>
```

7.2 2560x1440 @60Hz 24bpp – Dual DSI Channels and 2 DP at HBR2

```
<aardvark>
<configure i2c="1" spi="1" gpio="0" tpower="1" pullups="0" />
<i2c_bitrate khz="100" />
======Dual 4 DSI lanes======
<i2c_write addr="0x2D" count="1" radix="16">10 00</i2c_write>
<sleep ms="10" />
======enhanced framing======
<i2c_write addr="0x2D" count="1" radix="16">5A 04</i2c_write>
<sleep ms="10" />
======Pre0dB 2 lanes no SSC======
<i2c_write addr="0x2D" count="1" radix="16">93 20</i2c_write>
<sleep ms="10" />
======L0mV HBR2======
<i2c_write addr="0x2D" count="1" radix="16">94 E0</i2c_write>
<sleep ms="10" />
======PLL ENABLE======
<i2c_write addr="0x2D" count="1" radix="16">0D 01</i2c_write>
<sleep ms="10" />
======POST2 0dB ======
<i2c_write addr="0x2D" count="1" radix="16">95 00</i2c_write>
<sleep ms="10" />
======Semi-Auto TRAIN ======
<i2c_write addr="0x2D" count="1" radix="16">96 0A</i2c_write>
<sleep ms="20" />
```

```
======ADDR 0x96 CFR======
<i2c_write addr="0x2D" count="0" radix="16">96</i2c_write>
<sleep ms="20" />
======Read======
<i2c_read addr="0x2D" count="1" radix="16">00</i2c_read>
<sleep ms="10" />
=====CHA_ACTIVE_LINE_LENGTH=======
<i2c_write addr="0x2D" count="2" radix="16">20 00 05</i2c_write>
<sleep ms="10" />
=====CHB_ACTIVE_LINE_LENGTH=======
<i2c_write addr="0x2D" count="2" radix="16">22 00 05</i2c_write>
<sleep ms="10" />
=====CHA_VERTICAL_DISPLAY_SIZE=======
<i2c_write addr="0x2D" count="2" radix="16">24 A0 05</i2c_write>
<sleep ms="10" />
=====CHA_HSYNC_PULSE_WIDTH=======
<i2c_write addr="0x2D" count="2" radix="16">2C 20 00</i2c_write>
<sleep ms="10" />
=====CHA_VSYNC_PULSE_WIDTH=======
<i2c_write addr="0x2D" count="2" radix="16">30 05 80</i2c_write>
<sleep ms="10" />
=====CHA_HORIZONTAL_BACK_PORCH=======
<i2c_write addr="0x2D" count="1" radix="16">34 50</i2c_write>
<sleep ms="10" />
=====CHA_VERTICAL_BACK_PORCH=======
<i2c_write addr="0x2D" count="1" radix="16">36 21</i2c_write>
<sleep ms="10" />
=====CHA_HORIZONTAL_FRONT_PORCH=======
<i2c_write addr="0x2D" count="1" radix="16">3A 03</i2c_write>
<sleep ms="10" />
======DP-18BPP Enable======
<i2c_write addr="0x2D" count="1" radix="16">5B 00</i2c_write>
<sleep ms="10" />
=====COLOR BAR =======
<i2c_write addr="0x2D" count="1" radix="16">3C 00</i2c_write>
<sleep ms="10" />
======enhanced framing and Vstream enable======
<i2c_write addr="0x2D" count="1" radix="16">5A 0C</i2c_write>
<sleep ms="10" />
```

```
</aardvark>
```

7.3 Enabling ASSR in Panel

ASSR must be enabled in the panel before link training is performed.

```
<aardvark>
<configure i2c="1" spi="1" gpio="0" tpower="1" pullups="0" />
<i2c_bitrate khz="100" />
======Write DPCD Register 0x0010A to Enable ASSR======
<i2c_write addr="0x2D" count="1" radix="16">64 01</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">74 00</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">75 01</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">76 0A</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">77 01</i2c_write> />
<i2c_write addr="0x2D" count="1" radix="16">78 81</i2c_write>
<sleep ms="10" />
======enhanced framing and ASSR enable======
<i2c_write addr="0x2D" count="1" radix="16">5A 05</i2c_write>
<sleep ms="10" />
</aardvark>
```

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U.S. Federal Communications Commission Compliance

For EVMs Annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation. Changes or modifications could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at its own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Industry Canada Compliance (English)

For EVMs Annotated as IC – INDUSTRY CANADA Compliant:

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user’s authority to operate the equipment.

Concerning EVMs Including Radio Transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs Including Detachable Antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Canada Industry Canada Compliance (French)

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

Important Notice for Users of EVMs Considered “Radio Frequency Products” in Japan

EVMs entering Japan are NOT certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If user uses EVMs in Japan, user is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry’s Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after user obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after user obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless user gives the same notice above to the transferee. Please note that if user does not follow the instructions above, user will be subject to penalties of Radio Law of Japan.

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