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Driving Capacitance With the THS3001

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Driving Capacitance With the THS3001

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ABSTRACT

Operational amplifiers (op amps) are often used to drive devices that present significant capacitance such as analog-to-digital converters, cables, MOSFETs, filter networks, etc. The effect of the added capacitance is to cause extra phase shift, which tends to erode the phase margin of the amplifier and may lead to instability. At high frequency, even a very small capacitance is detrimental.

This paper outlines an effective method for stabilizing the THS3001 while driving capacitive loads.

1 Introduction

A typical technique used to compensate for capacitance on the output is to isolate it with a resistor and provide phase lead compensation using a capacitor in the feedback path. This works well for voltage feedback op amps, even though it also tends to reduce bandwidth.

In the case of the THS3001, there are problems with adding capacitance in the feedback path. The THS3001 is a current feedback op amp and so has a minimum feedback impedance requirement. Adding a capacitor in the feedback path lowers the impedance at high frequency and leads to more instability: the opposite effect from what is desired.

Therefore, isolating the capacitance from the output of the THS3001 by inserting a resistor is the most practical means of maintaining stability. This report outlines the test set up and resistor values required to stabilize the THS3001 while driving capacitance.

2 Test

Figure 1 shows the test circuits that determine the minimum value of isolation resistance required for stable operation.

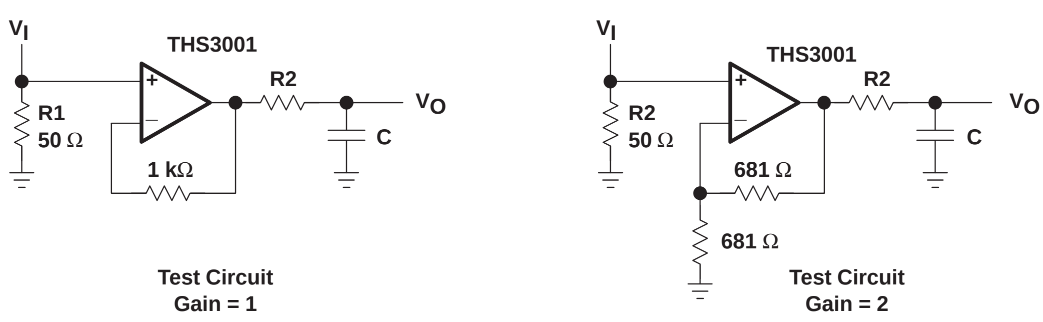

Figure 1. Test Circuits

The input signal is a square pulse with rise time and fall time of 5 ns and the amplitude adjusted for ±2 V on the output of the op amp. Gains of 1 and 2 show no significant difference. The power supply voltage is varied between ±5 V and ±15 V. The signal source is a LeCroy model 9210 pulse generator with a 9211 variable edge output module. The output signal is probed using a Tektronix P6217 4 GHz probe with input load of 0.4 pF and 100 kΩ. The signal is then displayed on a Tektronix TDS 794D oscilloscope.

The test circuit is built using the THS3001 EVM, #SLOP 130. The load capacitor is soldered across the terminal pins of output connector J2 on the solder side of the EVM. The circuit power is applied, the input signal is applied, and resistor (R2) adjusted until a square pulse with less than 1% overshoot and undershoot is obtained.

3 Data

Graph A in Figure 2 is a plot of resistor (R2) vs capacitance (C) and graph B is a plot of the rise time vs capacitance (C) (with R2). Graph A is plotted with log-log scales to show the log relationship of resistor (R2) to capacitor (C).

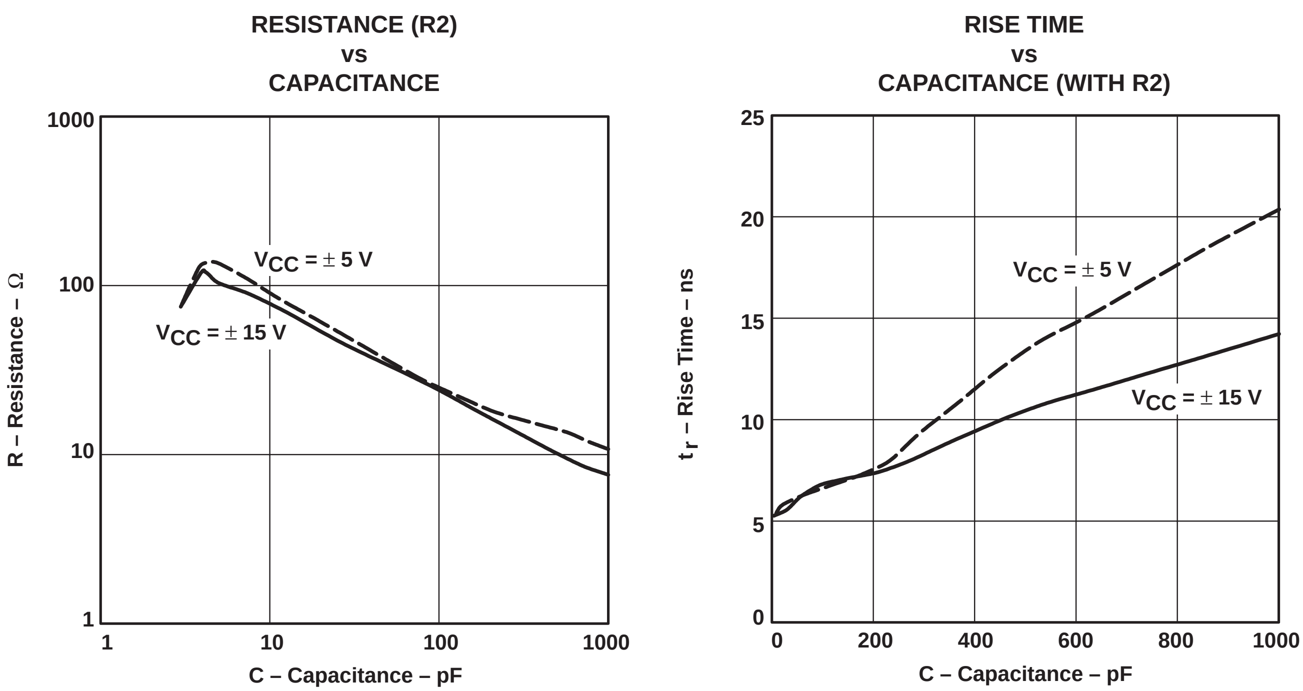

Figure 2. R2 and Rise Time vs Capacitance

With $V_{CC} = \pm5$ V, slightly higher resistor values are required than with $V_{CC} = \pm15$ V, and the rise time was significantly longer with C > 220 pF. A formula for estimating the required resistor value is found to be: $R = \frac{1}{\sqrt{C}} \times 300$, where C is in pF.

4 Summary

When driving load capacitance, insert a resistor in series with the output to isolate the load capacitance from the feedback path and maintain amplifier stability. A reasonable starting value for the isolation resistor is estimated by $R = \frac{1}{\sqrt{C}} \times 300$, where C is the load capacitance in pF. Final verification is achieved by constructing and testing the circuit.