

Intel StrataFlash Embedded Memory (P30) Power Solutions

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PMP - Portable Power DC-DC Applications

ABSTRACT

This application report provides several recommended power management solutions for the Intel™StrataFlash™ Embedded Memory (P30). Intel has migrated from its third-generation 180-nm J3 process to its fourth-generation 130-nm P30 process on flash memory and will be discontinuing the older J3 256-Mb memory. Migrating from J3 memory to the P30 Embedded Memory allows systems to operate at a lower overall current consumption because the P30 Vcc voltage requirement has dropped to 1.8 V.

From Intel application note AP812 (order number 306667), Intel recommends using LDOs (low dropout regulators) for older applications that do not have 1.8 V available for the P30 Vcc core voltage. Figure 1 shows how Intel recommends using the LDO to regulate the available 3-V Vccq voltage down to the Vcc voltage.

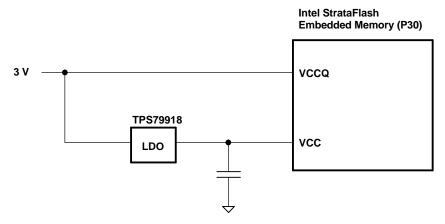


Figure 1. Typical StrataFlash Configuration With LDO

Intel specifically recommends the following LDOs for its StrataFlash P30 memory: These four LDOs meet the electrical and temperature requirements for the new P30 memory.

	ν _ο (V)	I _O (mA)	lq (μ A)	PSRR (dB)	Package	Dimensions (mm)
TPS77618D	1.8	250	35	50	SOIC	6 × 4,9 × 1,75
TPS79918DDC	1.8	200	40	70	TSOT-23	$2,9 \times 2,8 \times 1$
TPS79918DRV	1.8	200	40	70	2×2 SON	$2 \times 2 \times 0.75$
TPS79918YZU	1.8	200	40	70	WSCP	$1,36\times1\times0,62$

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Each LDO has specific advantages that recommend it for a particular application.

TPS76618D: Due to the larger package (SOIC), the TPS76618D is able to dissipate the largest amount of power. This part also accepts input voltages as high as 13.5 V. The output voltage accuracy is $\pm 3\%$.

TPS79918DDC: This SOT-23 package provides a significantly smaller solution size than the larger SOIC package. It provides a nominal accuracy of 1%. This LDO is stable with a small $2.2-\mu F$ ceramic output capacitor.

TPS79918DRV: This SON (small outline, no lead) package is also a relatively small-sized solution. It is stable with a $2.2-\mu F$ ceramic output capacitor. Due to the power pad on the bottom of the package, it dissipates significantly more power than the SOT-23 package.

TPS79918YZU: This WSCP (wafer scale chip package) provides the smallest solution size. It is also stable with a $2.2-\mu F$ ceramic output capacitor.

References

- TPS766xx, Ultra Low Quiescent Current 250-mA Low-Dropout Voltage Regulators data sheet (SLVS237)
- 2. TPS799xx, 200mA Low Quiescent Current, Ultra-Low Noise, High PSRR Low Dropout Linear Regulators data sheet (SBVS056)
- 3. Migration Guide for Intel StrataFlash Memory (J3) to Intel StrataFlash Embedded Memory (P30), Intel application note AP812, order number 306667

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